

## FEATURES

- Member of the Texas Instruments Widebus™ Family
- Optimized for 1.8-V Operation and Is 3.6-V I/O Tolerant to Support Mixed-Mode Signal Operation
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Sub-1-V Operable
- Max  $t_{pd}$  of 2.8 ns at 1.8 V
- Low Power Consumption, 20- $\mu$ A Max  $I_{CC}$
- $\pm 8$ -mA Output Drive at 1.8 V
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

## DESCRIPTION/ORDERING INFORMATION

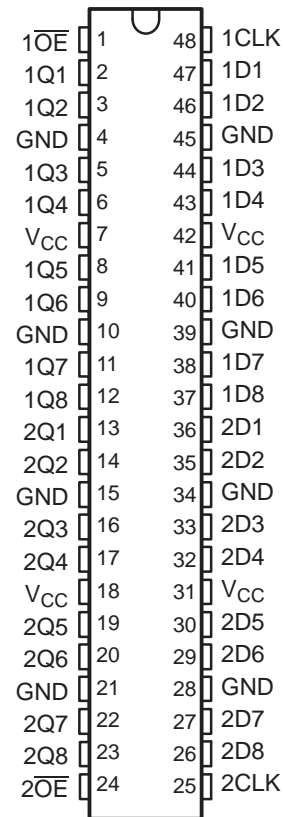
This 16-bit edge-triggered D-type flip-flop is operational at 0.8-V to 2.7-V  $V_{CC}$ , but is designed specifically for 1.65-V to 1.95-V  $V_{CC}$  operation.

The SN74AUC16374 is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers. It can be used as two 8-bit flip-flops or one 16-bit flip-flop. On the positive transition of the clock (CLK) input, the Q outputs of the flip-flop take on the logic levels set up at the data (D) inputs.

A buffered output-enable ( $\overline{OE}$ ) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

$\overline{OE}$  does not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

DGG OR DGV PACKAGE  
(TOP VIEW)



## ORDERING INFORMATION

$T_A$	PACKAGE <sup>(1)(2)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	TSSOP – DGG	Reel of 2000	SN74AUC16374DGGR	AUC16374
	TVSOP – DGV	Reel of 2000	SN74AUC16374DGVV	MH374
	VFBGA – ZQL	Reel of 1000	SN74AUC16374ZQLR	MH374

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at [www.ti.com](http://www.ti.com).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Widebus is a trademark of Texas Instruments.

# SN74AUC16374

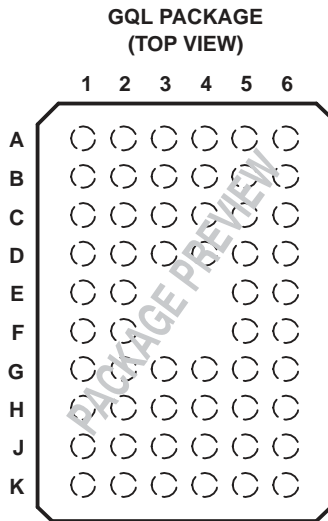
## 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

SCES403E—JULY 2002—REVISED APRIL 2007

### DESCRIPTION/ORDERING INFORMATION (CONTINUED)

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.



### TERMINAL ASSIGNMENTS<sup>(1)</sup>

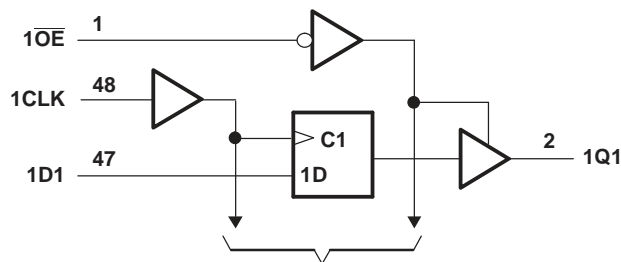
	1	2	3	4	5	6
A	$1\overline{OE}$	NC	NC	NC	NC	1CLK
B	1Q2	1Q1	GND	GND	1D1	1D2
C	1Q4	1Q3	$V_{CC}$	$V_{CC}$	1D3	1D4
D	1Q6	1Q5	GND	GND	1D5	1D6
E	1Q8	1Q7			1D7	1D8
F	2Q1	2Q2			2D2	2D1
G	2Q3	2Q4	GND	GND	2D4	2D3
H	2Q5	2Q6	$V_{CC}$	$V_{CC}$	2D6	2D5
J	2Q7	2Q8	GND	GND	2D8	2D7
K	$2\overline{OE}$	NC	NC	NC	NC	2CLK

(1) NC - No internal connection

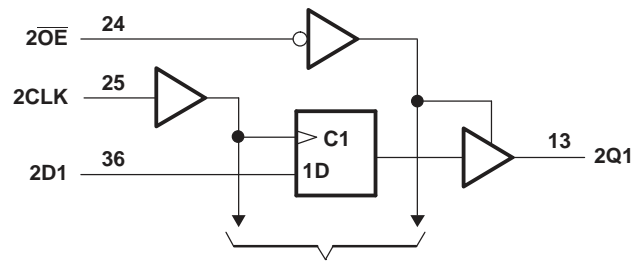
### FUNCTION TABLE (EACH FLIP-FLOP)

INPUTS			OUTPUT Q
$\overline{OE}$	CLK	D	
L	↑	H	H
L	↑	L	L
L	H or L	X	$Q_0$
H	X	X	Z

### LOGIC DIAGRAM (POSITIVE LOGIC)



To Seven Other Channels



To Seven Other Channels

Pin numbers shown are for the DGG and DGV packages.

### Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range	-0.5	3.6	V
V <sub>I</sub>	Input voltage range <sup>(2)</sup>	-0.5	3.6	V
V <sub>O</sub>	Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup>	-0.5	3.6	V
V <sub>O</sub>	Output voltage range <sup>(2)</sup>	-0.5	V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0	-50	mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0	-50	mA
I <sub>O</sub>	Continuous output current		±20	mA
	Continuous current through V <sub>CC</sub> or GND		±100	mA
θ <sub>JA</sub>	Package thermal impedance <sup>(3)</sup>	DGG package	70	°C/W
		DGV package	58	
		GQL package	42	
T <sub>stg</sub>	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The package thermal impedance is calculated in accordance with JESD 51-7.

### Recommended Operating Conditions<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	0.8	2.7	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 0.8 V	V <sub>CC</sub>	V
		V <sub>CC</sub> = 1.1 V to 1.95 V	0.65 × V <sub>CC</sub>	
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.7	
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 0.8 V	0	V
		V <sub>CC</sub> = 1.1 V to 1.95 V	0.35 × V <sub>CC</sub>	
		V <sub>CC</sub> = 2.3 V to 2.7 V	0.7	
V <sub>I</sub>	Input voltage	0	3.6	V
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 0.8 V	-0.7	mA
		V <sub>CC</sub> = 1.1 V	-3	
		V <sub>CC</sub> = 1.4 V	-5	
		V <sub>CC</sub> = 1.65 V	-8	
		V <sub>CC</sub> = 2.3 V	-9	
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 0.8 V	0.7	mA
		V <sub>CC</sub> = 1.1 V	3	
		V <sub>CC</sub> = 1.4 V	5	
		V <sub>CC</sub> = 1.65 V	8	
		V <sub>CC</sub> = 2.3 V	9	
Δt/Δv	Input transition rise or fall rate		20	ns/V
T <sub>A</sub>	Operating free-air temperature	-40	85	°C

- (1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

# SN74AUC16374

## 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

SCES403E–JULY 2002–REVISED APRIL 2007

### Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP <sup>(1)</sup>	MAX	UNIT
V <sub>OH</sub>		I <sub>OH</sub> = -100 μA	0.8 V to 2.7 V	V <sub>CC</sub> - 0.1			V
		I <sub>OH</sub> = -0.7 mA	0.8 V	0.55			
		I <sub>OH</sub> = -3 mA	1.1 V	0.8			
		I <sub>OH</sub> = -5 mA	1.4 V	1			
		I <sub>OH</sub> = -8 mA	1.65 V	1.2			
		I <sub>OH</sub> = -9 mA	2.3 V	1.8			
V <sub>OL</sub>		I <sub>OL</sub> = 100 μA	0.8 V to 2.7 V			0.2	V
		I <sub>OL</sub> = 0.7 mA	0.8 V			0.25	
		I <sub>OL</sub> = 3 mA	1.1 V			0.3	
		I <sub>OL</sub> = 5 mA	1.4 V			0.4	
		I <sub>OL</sub> = 8 mA	1.65 V			0.45	
		I <sub>OL</sub> = 9 mA	2.3 V			0.6	
I <sub>I</sub>	All inputs	V <sub>I</sub> = V <sub>CC</sub> or GND	0 to 2.7 V			±5	μA
I <sub>off</sub>		V <sub>I</sub> or V <sub>O</sub> = 2.7 V	0			±10	μA
I <sub>OZ</sub>		V <sub>O</sub> = V <sub>CC</sub> or GND	2.7 V			±10	μA
I <sub>CC</sub>		V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	0.8 V to 2.7 V			20	μA
C <sub>i</sub>		V <sub>I</sub> = V <sub>CC</sub> or GND	2.5 V			3	pF
C <sub>o</sub>		V <sub>O</sub> = V <sub>CC</sub> or GND	2.5 V			5	pF

(1) All typical values are at T<sub>A</sub> = 25°C.

### Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		V <sub>CC</sub> = 0.8 V	V <sub>CC</sub> = 1.2 V ± 0.1 V		V <sub>CC</sub> = 1.5 V ± 0.1 V		V <sub>CC</sub> = 1.8 V ± 0.15 V		V <sub>CC</sub> = 2.5 V ± 0.2 V		UNIT
		TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>clock</sub>	Clock frequency	85	250		250		250		250		MHz
t <sub>w</sub>	Pulse duration, CLK high or low	5.9	1.9		1.9		1.9		1.9		ns
t <sub>su</sub>	Setup time, data before CLK↑	1.4	1.2		0.7		0.6		0.6		ns
t <sub>h</sub>	Hold time, data after CLK↑	0.1	0.4		0.4		0.4		0.4		ns

### Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 0.8 V	V <sub>CC</sub> = 1.2 V ± 0.1 V		V <sub>CC</sub> = 1.5 V ± 0.1 V		V <sub>CC</sub> = 1.8 V ± 0.15 V			V <sub>CC</sub> = 2.5 V ± 0.2 V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	TYP	MAX	MIN	MAX	
f <sub>max</sub>			85	250		250		250			250		MHz
t <sub>pd</sub>	CLK	Q	7.3	1	4.5	0.8	2.9	0.7	1.5	2.8	0.7	2.2	ns
t <sub>en</sub>	$\overline{OE}$	Q	7	1.2	5.3	0.8	3.6	0.8	1.5	2.9	0.7	2.2	ns
t <sub>dis</sub>	$\overline{OE}$	Q	8.2	2	7.1	1	4.8	1.4	2.7	4.5	0.5	2.2	ns

## Operating Characteristics<sup>(1)</sup>

$T_A = 25^\circ\text{C}$

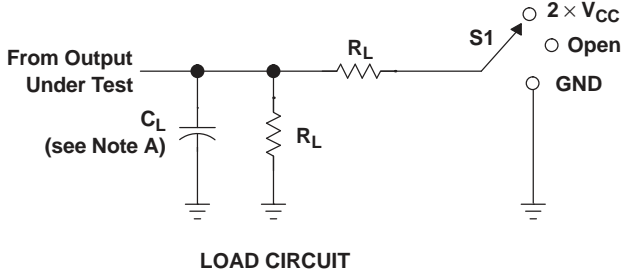
PARAMETER			TEST CONDITIONS	$V_{CC} = 0.8\text{ V}$	$V_{CC} = 1.2\text{ V}$	$V_{CC} = 1.5\text{ V}$	$V_{CC} = 1.8\text{ V}$	$V_{CC} = 2.5\text{ V}$	UNIT
				TYP	TYP	TYP	TYP	TYP	
$C_{pd}$ (each output) <sup>(2)</sup>	Power dissipation capacitance	Outputs enabled, 1 output switching	1 $f_{data} = 5\text{ MHz}$ , 1 $f_{clk} = 10\text{ MHz}$ , 1 $f_{out} = 5\text{ MHz}$ , $\overline{OE} = \text{GND}$ , $C_L = 0\text{ pF}$	24	24	24.1	26.2	31.2	pF
$C_{pd(Z)}$	Power dissipation capacitance	Outputs disabled, 1 clock and 1 data switching	1 $f_{data} = 5\text{ MHz}$ , 1 $f_{clk} = 10\text{ MHz}$ , $f_{out} = \text{not switching}$ , $\overline{OE} = V_{CC}$ , $C_L = 0\text{ pF}$	7.5	7.5	8	9.4	13.2	pF
$C_{pd}$ (each clock) <sup>(3)</sup>	Power dissipation capacitance	Outputs disabled, clock only switching	1 $f_{data} = 0\text{ MHz}$ , 1 $f_{clk} = 10\text{ MHz}$ , $f_{out} = \text{not switching}$ , $\overline{OE} = V_{CC}$ , $C_L = 0\text{ pF}$	13.8	13.8	14	14.7	17.5	pF

(1) Total device  $C_{pd}$  for multiple (n) outputs switching and (y) clocks inputs switching =  $\{n * C_{pd} \text{ (each output)}\} + \{y * C_{pd} \text{ (each clock)}\}$

(2)  $C_{pd}$  (each output) is the  $C_{pd}$  for each data bit (input and output circuitry) as it operates at 5 MHz (Note: the clock is operating at 10 MHz in this test, but its  $I_{CC}$  component has been subtracted out).

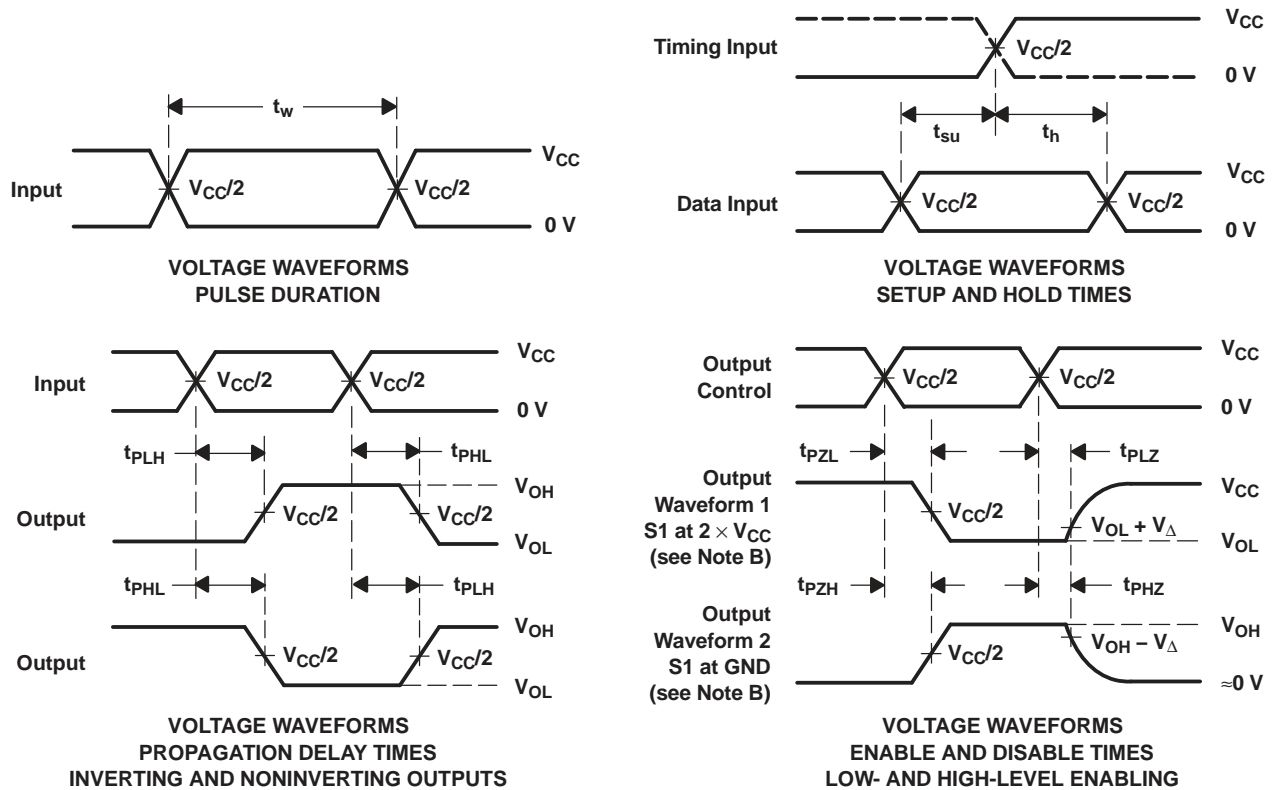
(3)  $C_{pd}$  (each clock) is the  $C_{pd}$  for the clock circuitry only as it operates at 10 MHz.

**PARAMETER MEASUREMENT INFORMATION**



TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$2 \times V_{CC}$
$t_{PHZ}/t_{PZH}$	GND

$V_{CC}$	$C_L$	$R_L$	$V_{\Delta}$
0.8 V	15 pF	2 k $\Omega$	0.1 V
1.2 V $\pm$ 0.1 V	15 pF	2 k $\Omega$	0.1 V
1.5 V $\pm$ 0.1 V	15 pF	2 k $\Omega$	0.1 V
1.8 V $\pm$ 0.15 V	30 pF	1 k $\Omega$	0.15 V
2.5 V $\pm$ 0.2 V	30 pF	500 $\Omega$	0.15 V



- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50 \Omega$ , slew rate  $\geq$  1 V/ns.
  - D. The outputs are measured one at a time, with one transition per measurement.
  - E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
  - H. All parameters and waveforms are not applicable to all devices.

**Figure 1. Load Circuit and Voltage Waveforms**

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AUC16374DGGR	ACTIVE	TSSOP	DGG	48	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AUC16374	<a href="#">Samples</a>
SN74AUC16374DGVR	ACTIVE	TVSOP	DGV	48	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MH374	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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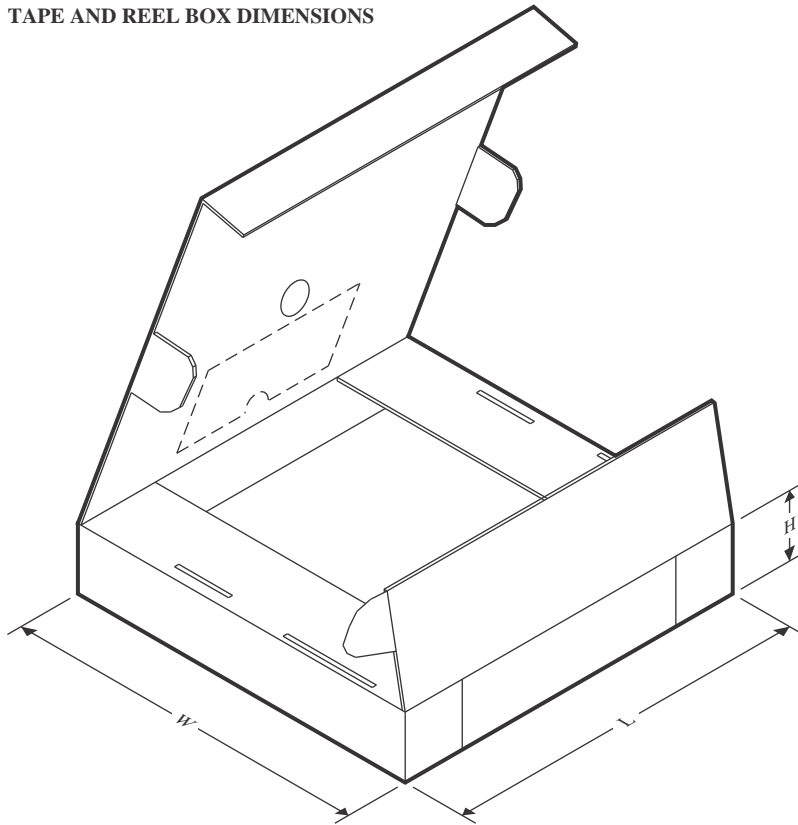


**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUC16374DGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
SN74AUC16374DGVR	TVSOP	DGV	48	2000	330.0	16.4	7.1	10.2	1.6	12.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


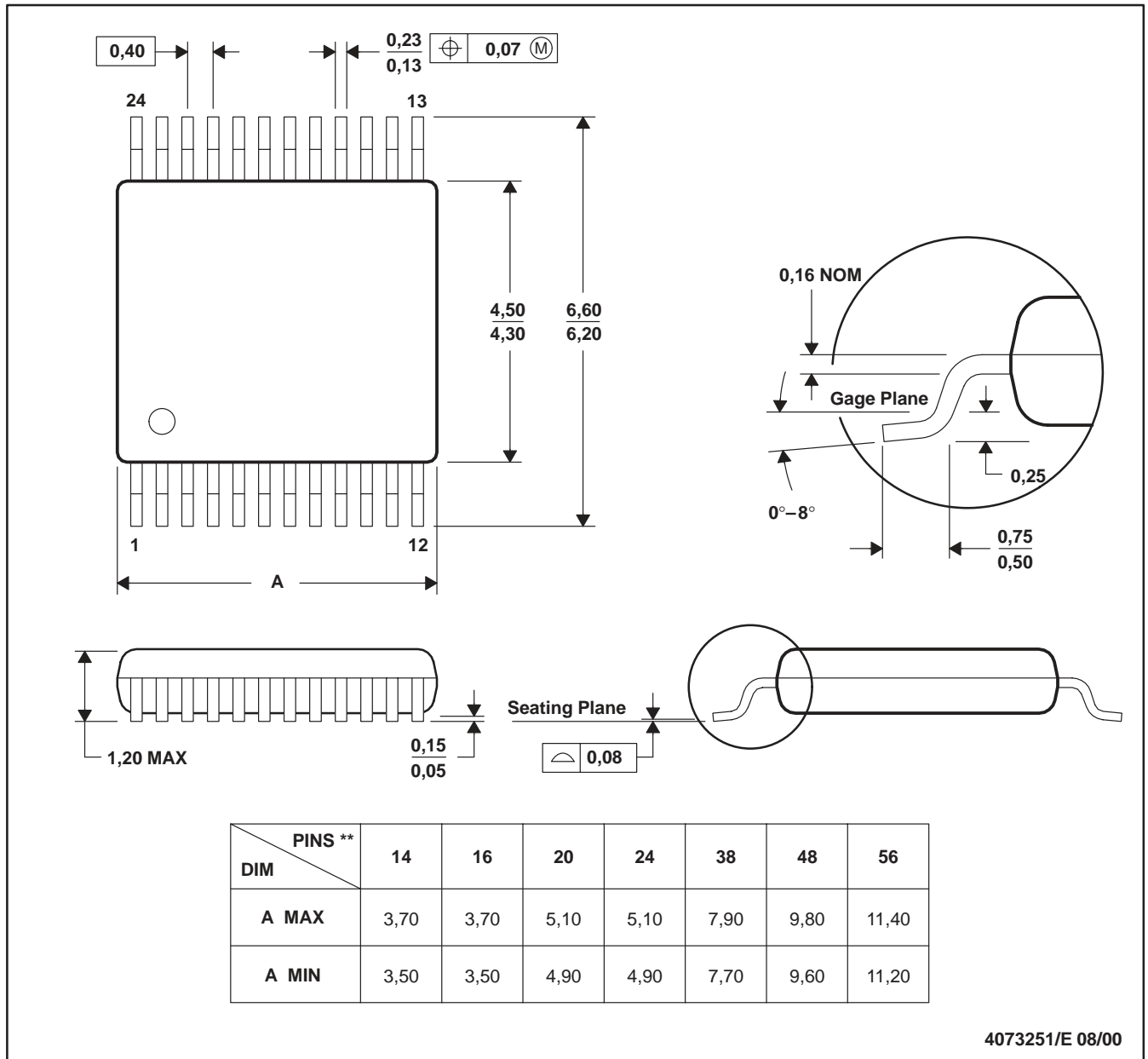
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AUC16374DGGR	TSSOP	DGG	48	2000	367.0	367.0	45.0
SN74AUC16374DGVR	TVSOP	DGV	48	2000	356.0	356.0	35.0

DGV (R-PDSO-G\*\*)

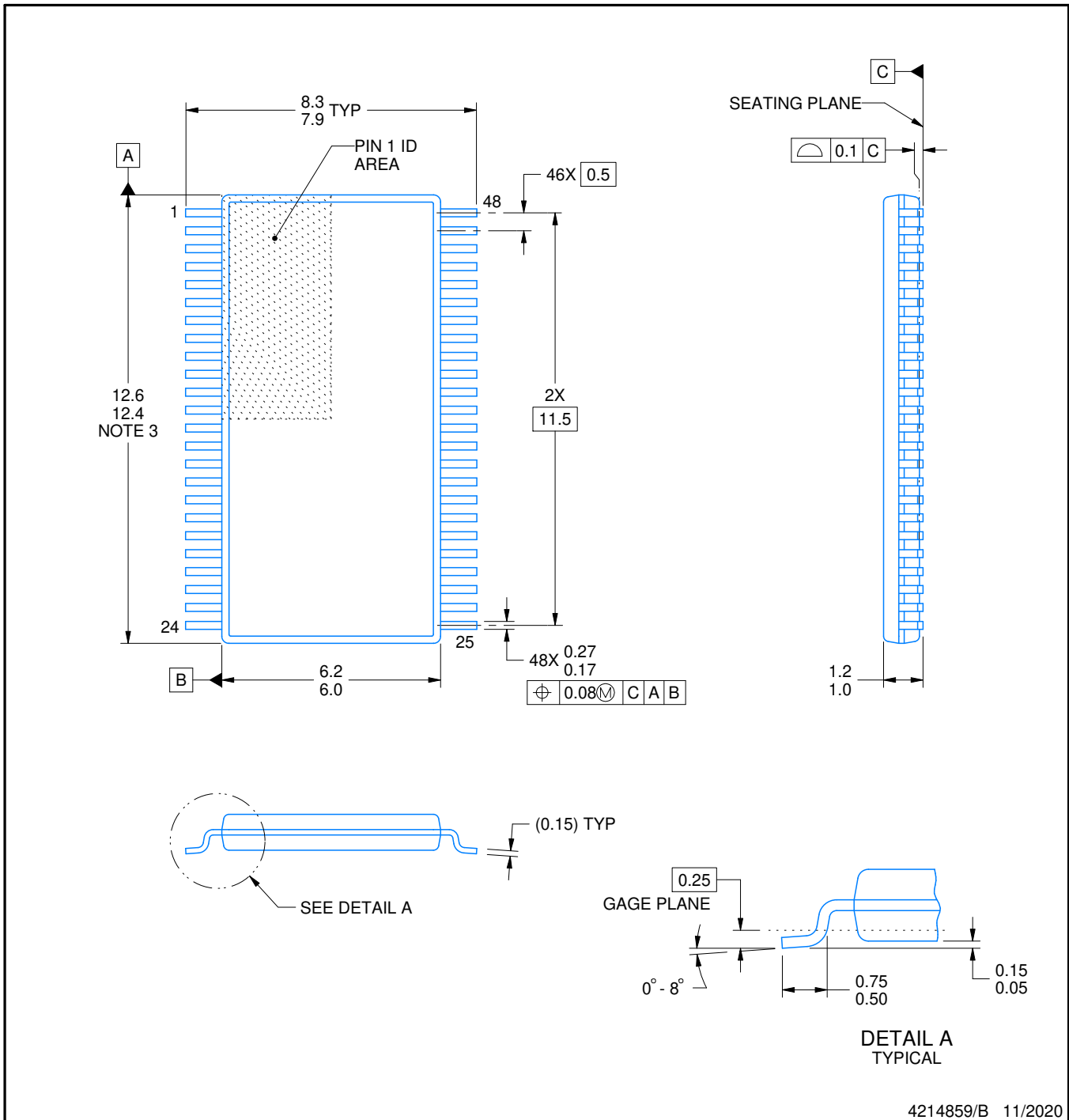
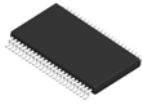
PLASTIC SMALL-OUTLINE

24 PINS SHOWN



4073251/E 08/00

- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194



4214859/B 11/2020

NOTES:

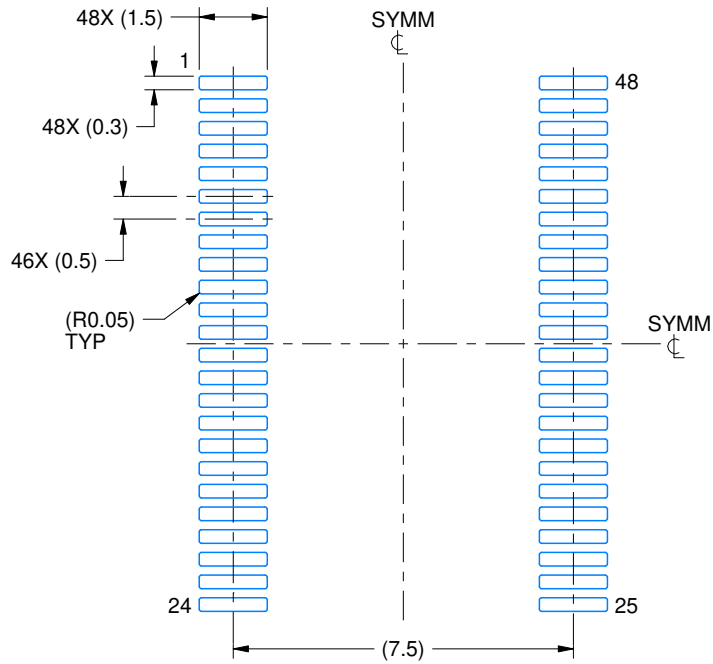
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

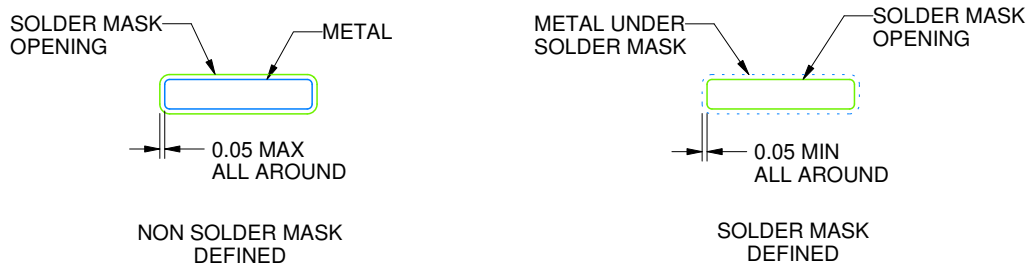
DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4214859/B 11/2020

NOTES: (continued)

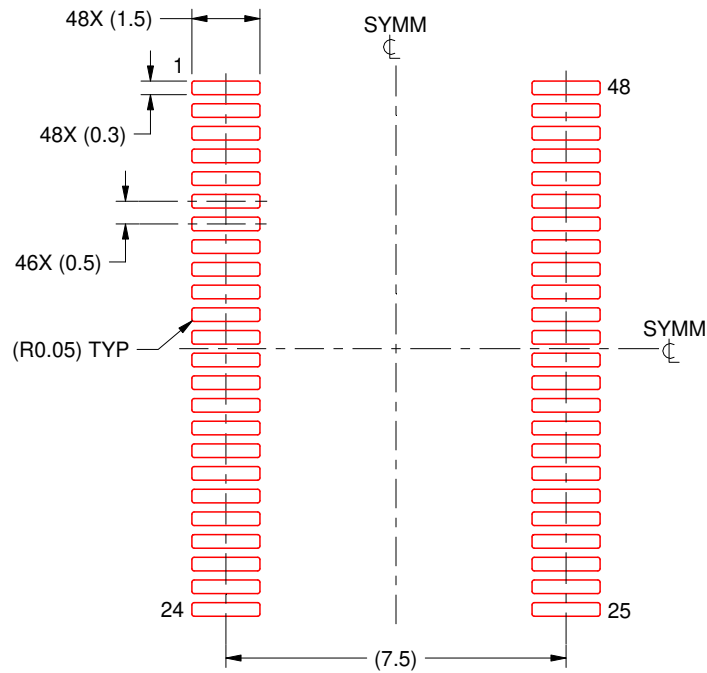
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4214859/B 11/2020

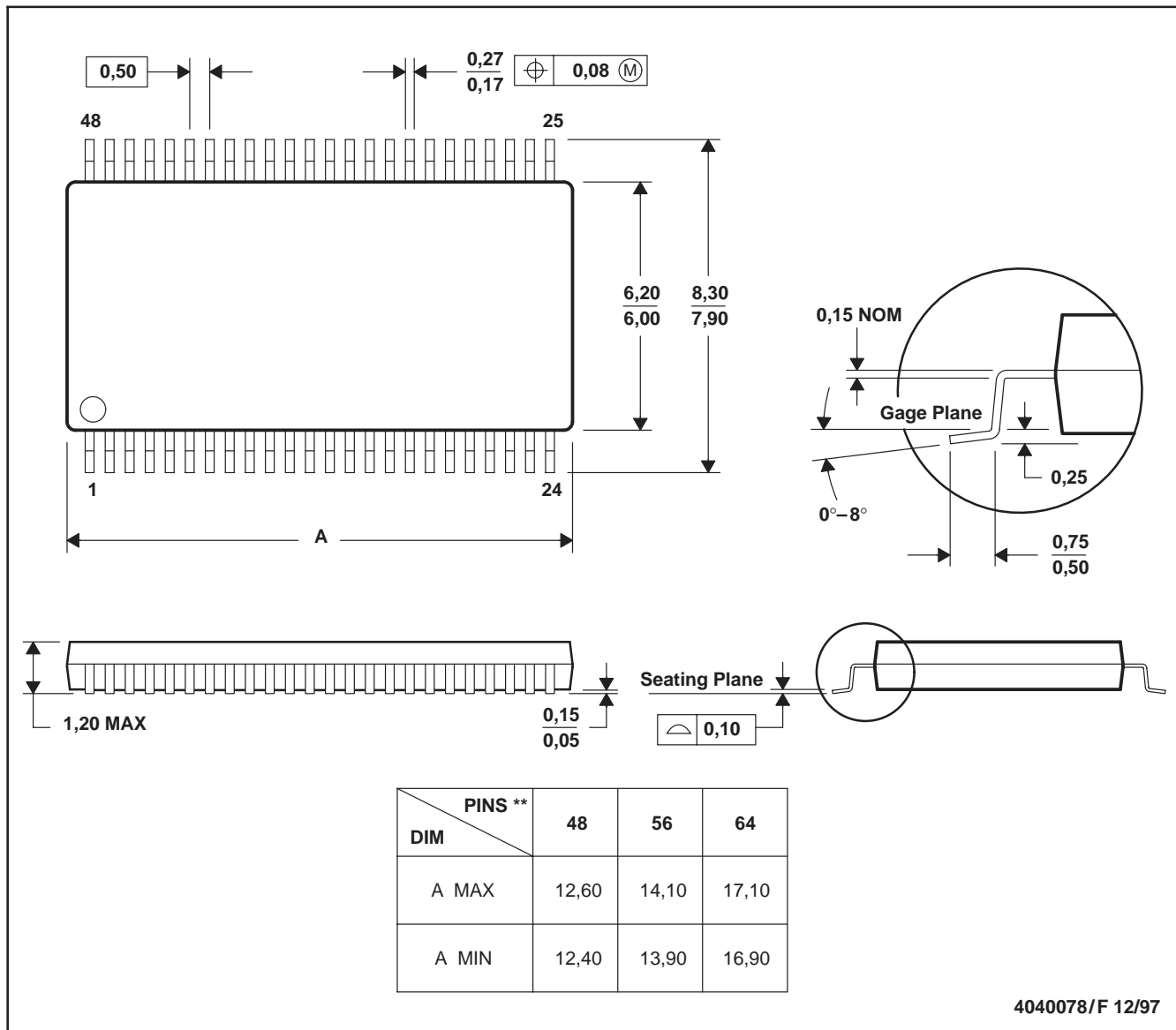
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DGG (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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