AN-1630 LM5001 Non-Isolated Flyback Evaluation Board

1 Introduction

The LM5001 non-isolated flyback evaluation board is designed to provide the design engineer with a fully functional non-isolated flyback power converter based on Current Mode Control to evaluate the LM5001 switching regulator IC. The evaluation board provides a 5V output with 1A current capability. The input voltage ranges from 16V to 42V. The design operates at 250KHz, a good compromise between conversion efficiency and solution size. The printed circuit board consists of 2 layers of 2 ounce copper on FR4 material with a thickness of 0.062 inches. This application note contains the evaluation board schematic, Bill-of-Materials (BOM) and a quick setup procedure. Refer to the LM5001 datasheet for complete circuit design information. For complete circuit design information, see *LM5001 High Voltage Switch Mode Regulator* (SNVS484).

The performance of the evaluation board is:

- Input Range: 16 to 42V
- Output Voltage: 5V, ±2%
- Output Current: 0 to 1A
- Frequency of Operation: 250 kHz
- Board Size: 2.75 × 1.75 × 0.6 inches
- Load Regulation: 0.1%
- Line Regulation: 0.1%
- Over Current Limiting

2 Evaluation Board Schematic

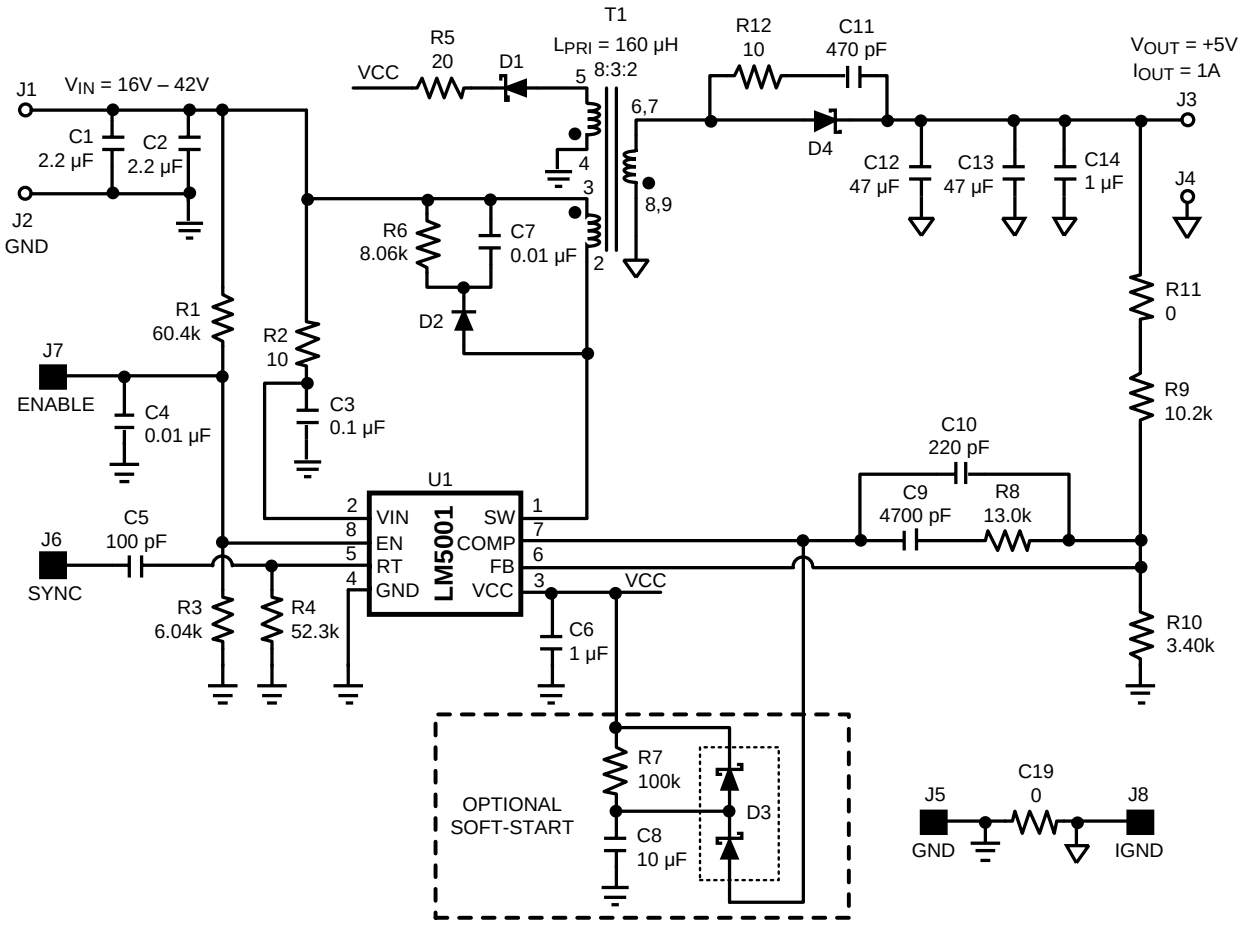


Figure 1. Evaluation Board Schematic

3 Powering and Loading Considerations

Read this entire section prior to attempting to power the evaluation board.

3.1 Quick Setup Procedure

Step 1: Set the input source current limit to 1A. Turn off the input source. Connect the positive output of the input source to J1 and the negative output to J2.

Step 2: Connect the load, with 1A capability, to J3 for the positive connection and J4 for the negative connection.

Step 3: The ENABLE pin, J7, should be left open for normal operation.

Step 4: Set the input source voltage to 28V and the load to 0.1A. The load voltage should be in regulation with a nominal 5V output.

Step 5: Slowly increase the load while monitoring the load voltage at J3 and J4. It should remain in regulation with a nominal 5V output as the load is increased up to 1 Amp.

Step 6: Slowly sweep the input source voltage from 16V to 42V. The load voltage should remain in regulation with a nominal 5V output.

Step 7: Temporally short the ENABLE pin (J7) to GND (J5) to check the shutdown function.

Step 8: Increase the load beyond the normal range to check current limiting while the input source is set to 28V. The output current should limit at approximately 1.9A. The input source current limit should be increased for this step. Fan cooling is critical during this step.

3.2 AIr Flow

Prolonged operation at full power and high ambient temperature will cause the thermal shutdown circuit within the regulator IC to activate. A fan with a minimum of 200 LFM should always be provided.

3.3 Powering Up

Using the ENABLE pin (J7) provided will allow powering up the input source with the current level set low. It is suggested that the load power be kept low during the first power up. Set the current limit of the input source to provide about 1.5 times the anticipated wattage of the load. As you remove the connection from the ENABLE pin to GND (J5), immediately check for 5 volts at the output.

A quick efficiency check is the best way to confirm that everything is operating properly. If something is amiss you can be reasonably sure that it will affect the efficiency adversely. Few parameters can be incorrect in a switching power supply without creating losses and potentially damaging heat.

3.4 Over Current Protection

The evaluation board is configured with cycle-by-cycle over-current protection. This function is completely contained in the LM5001. The Primary current is limited to approximately 1A. This equates to about 1.4A load current when the input voltage is 16V, and about 2.1A load current when the input is 42V. The thermal stress on various circuit components is quite severe while in an overloaded condition, therefore limit the duration of the overload and provide sufficient cooling (airflow).

3.5 Synchronization

A SYNC pin (J6) has been provided on the evaluation board. This pin can be used to synchronize the regulator to an external clock or multiple evaluation boards can be synchronized together by connecting their SYNC pins together. For complete information, see *LM5001 High Voltage Switch Mode Regulator* (SNVS484).

4 Flyback Topology

4.1 Flyback Transformer

Two things need to be considered when specifying a Flyback transformer to a magnetics manufacturer (Coilcraft, Pulse Engineering, Cooper-Coiltronics, and so on), the turns ratio to determine the duty cycle D (MOSFET on time compared to the switching period) and the primary inductance (L_{PRI}) to determine the current sense ramp for current mode control.

To start, the primary inductance in Continuous Current Mode (CCM) is designed to provide a ramp during the MOSFET on time, of around 30% of the full load MOSFET current. This produces a good signal-to-noise ratio for Current Mode Control.

The CCM duty cycle can be designed for 50% with nominal input voltage. The transfer function of a Flyback Powerstage is:

$$\frac{V_{OUT}}{V_{IN}} = \frac{D}{1 - D} \times \frac{N_{SEC}}{N_{PRI}} \tag{1}$$

So the duty cycle is:

$$D = \frac{V_{OUT}}{V_{OUT} + \frac{V_{IN} \times N_{SEC}}{N_{PRI}}} \tag{2}$$

And the approximate turns ratio is:

$$\frac{N_{SEC}}{N_{PRI}} = \frac{V_{OUT} \times (1-D)}{V_{IN} \times D} \tag{3}$$

The primary inductance (L_{PRI}) is then:

$$L_{PRI} = \frac{V_{IN} \times D \times \frac{1}{f_{SW}}}{30\% \times I_{OUT(MAX)} \times \frac{N_{SEC}}{N_{PRI}}} \tag{4}$$

4.2 Powerstage Analysis

In any switchmode topology that has the power MOSFET between the inductor and the output capacitor (boost, buck-boost, Flyback, SEPIC, and so on) a Right Half-Plane Zero (RHPZ) is produced by the Powerstage in the loop transfer function during Continuous Conduction Mode (CCM). If the topology is operated in Discontinuous Conduction Mode (DCM) the RHPZ does not exist. It is a function of the duty cycle, load and inductance, and causes an increase in loop gain while reducing the loop phase margin. A common practice is to determine the worst case RHPZ frequency and set the loop unity gain frequency below one-third of the RHPZ frequency.

In the Flyback topology, the equation for the RHPZ is:

$$F_{RHPZ} = \frac{\frac{V_{OUT}}{I_{OUT}} \times (1 - D)^2}{2\pi \times L_{SEC} \times D} \tag{5}$$

The worst case RHPZ frequency is at the maximum load where I_{OUT} is the highest and at minimum input voltage where the duty cycle D is the highest.

The LM5001 uses Slope Compensation to insure stability when the duty cycle exceeds 45%. This has the effect of adding some Voltage Mode control to this Current Mode IC. The effect on the Powerstage (Plant) transfer function is calculated in the following three equations:

Inductor current slope during MOSFET on time:

$$Sn = \frac{V_{IN}}{L_{PRI}} \tag{6}$$

Slope Compensation ramp:

$$Se = 450\ mV \times f_{SW} \tag{7}$$

Current Mode sampling gain:

$$F_{MOD} = V_{IN} \times \frac{N_{SEC}}{N_{PRI}} \times \frac{1}{(Sn + Se) \times \frac{1}{f_{SW}}} \tag{8}$$

The control-to-output transfer function (G_{VC}) using low ESR capacitors (ceramic, and so on) is:

$$G_{VC}(f) = \frac{V_{OUT}}{I_{OUT}} \times \frac{1 - D}{1 + D} \times \frac{1 - j2\pi f \times \frac{D \times L_{SEC}}{(1 - D)^2 \times \frac{V_{OUT}}{I_{OUT}}}}{1 + j2\pi f \times \frac{\frac{V_{OUT}}{I_{OUT}} \times C_{OUT}}{(1 + D)}} \tag{9}$$

If high ESR capacitors (aluminum electrolytic, and so on) are used for the output capacitance, an additional zero appears at frequency:

$$F_{ZERO(ESR)} = \frac{1}{2 \times \pi \times ESR \times C_{OUT}} \tag{10}$$

which increases the gain slope by +20dB per decade of frequency and boosts the phase 45° at $F_{ZERO(ESR)}$ and 90° at 10 × $F_{ZERO(ESR)}$. The output ripple voltage is also increased by:

$$V_{OUT(PEAK-PEAK)} = ESR \times \frac{I_{OUT}}{1 - D} \tag{11}$$

With these calculations, an approximate Powerstage Bode plot can be constructed with:

$$Gain = 20\log\left(F_{MOD}\sqrt{[Re(G_{VC})]^2 + [Im(G_{VC})]^2}\right) \tag{12}$$

$$Phase = \frac{180}{\pi} \times \arctan\left(\frac{Im(G_{VC})}{Re(G_{VC})}\right) \tag{13}$$

Since these equations don't take into account the various parasitic resistances and reactances present in all power converters, there will be some difference between the calculated Bode plot and the gain and phase of the prototype circuit. It is therefore important to measure the converter using a network analyzer (Venable Instruments, Ridley Engineering, Agilent, and so on) to quantify the implementation and adjust where appropriate.

4.3 Loop Compensation

The loop bandwidth and phase margin determines the response to load transients, while insuring that the output noise level meets the requirements. A common choice of loop unity gain frequency is 5% of the switching frequency. This is simple to compensate, low noise and provides sufficient transient response for most applications. The Plant Bode plot is examined for gain and phase at the desired Loop Unity Gain Frequency and the compensator is designed to adjust the loop gain and phase to meet the intended Loop Unity Gain Frequency and phase margin (typically about 55°). When gain is needed, the ratio of R8 and R9 sets the Error Amplifier to provide the correct amount.

$$A_{V(xo)} = \frac{R8}{R9} \tag{14}$$

The phase margin is boosted by a transfer function zero at frequency:

$$F_{ZERO} = \frac{1}{2 \times \pi \times R8 \times C9} \quad (15)$$

and a pole at:

$$F_{POLE(HI)} = \frac{1}{2 \times \pi \times R8 \times \frac{C9 \times C10}{C9 + C10}} \quad (16)$$

The separation between F_{ZERO} and F_{POLE} determines the amount of phase boost. If F_{ZERO} is chosen to be the Loop Unity Gain Frequency divided by a constant K, and F_{POLE} is the Loop Unity Gain Frequency times K, then the phase boost provided at the Loop Unity Gain Frequency is:

$$\theta_{BOOST} = \arctan(K) - \arctan\left(\frac{1}{K}\right) \quad (17)$$

The low frequency pole is determined by the Error Amplifier open loop gain (A_{VOL}) and R9, C9 and C10:

$$F_{POLE(LO)} = \frac{1}{2 \times \pi \times R9 \times (C9 + C10)} \times \frac{1}{A_{VOL}} \quad (18)$$

Optimal regulation is achieved by setting $F_{POLE(LO)}$ as high as possible, but still permitting F_{ZERO} to insure the desired phase margin.

4.4 MOSFET Rating

The peak MOSFET current can be determined by:

$$I_{PRI(PEAK)} = \frac{V_{IN} \times D \times \frac{1}{f_{SW}}}{2 \times L_{PRI}} + \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta \times D} \quad (19)$$

Where η is the Flyback converter efficiency.

The power MOSFET must withstand the input voltage plus the output voltage multiplied by the turns ratio during the off-time.

$$V_{SW} = V_{IN} + \left[V_{OUT} \times \frac{N_{PRI}}{N_{SEC}}\right] \quad (20)$$

In addition, any leakage inductance will cause a turn-off voltage spike above these two voltages. It will be controlled by the MOSFET drain-to-source capacitance as well as other parasitic capacitances. To further limit the spike magnitude, an RCD termination such as R6, C7 and D2 or a Diode-Zener clamp can be used.

4.5 Diode Rating

The average diode current equals the output current under normal circumstances, but the diode should be designed to handle a continuous current limit condition for the worst case:

$$I_{DIODE\ (WORST\text{-}CASE)} = I_{LIMIT\ (MOSFET)} \times \frac{N_{PRI}}{N_{SEC}} \quad (21)$$

The maximum reverse voltage applied to the diode occurs during the MOSFET on time:

$$V_{DIODE(REVERSE)} = V_{IN(MAX)} \times \frac{N_{SEC}}{N_{PRI}} \quad (22)$$

The diode's reverse capacitance will resonate with the transformer inductance (and other parasitic elements) to some degree and cause ringing that may be a problem with conducted and radiated emissions compliance. Usually an RC snubber network will eliminate the ringing.

5 Performance Characteristics

5.1 Efficiency Plots

Figure 2 shows the conversion efficiency versus output current for several input voltage conditions.

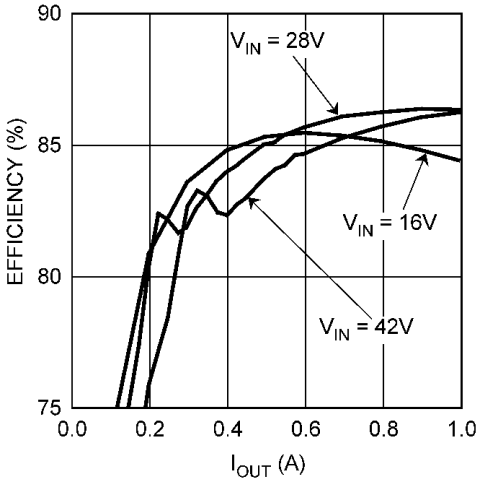
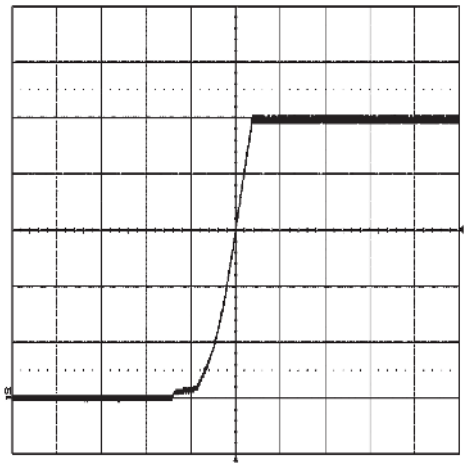


Figure 2. Efficiency Plots

5.2 Turn-on Waveform

When applying power to the LM5001 evaluation board a soft-start sequence occurs. Figure 3 shows the output voltage during a typical start-up sequence.

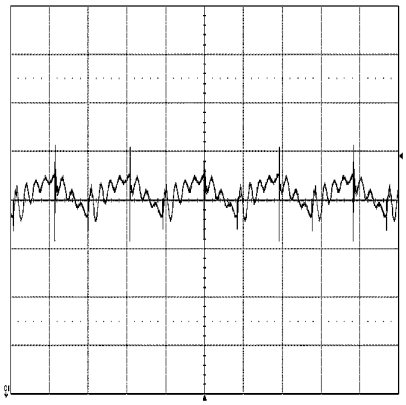


Conditions: Input Voltage = 28VDC, Output Current = 1A
Trace 1: Output Voltage Volts/div = 1V
Horizontal Resolution = 5ms/div

Figure 3. Turn-on Waveform

5.3 Output Ripple Waveform

Figure 4 shows the output voltage ripple. This measurement was taken with the scope probe tip placed on the J3 load terminal and the scope probe ground "barrel" pushed against the J4 load terminal. The scope bandwidth is set to 20 MHz.

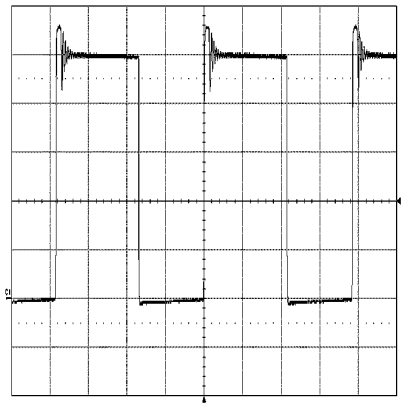


Conditions: Input Voltage = 28VDC, Output Current = 1A,
Bandwidth Limit = 20MHZ
Trace 1: Output Ripple Voltage Volts/div = 50mV
Horizontal Resolution = 2µs/div

Figure 4. Output Ripple Waveform

5.4 Primary Switch Node Waveform

Figure 5 shows the typical primary voltage during continuous conduction mode (CCM).



Conditions: Input Voltage = 28VDC, Output Current = 1A,
Bandwidth Limit = 20MHZ
Trace 1: LM5001 SW Pin Volts/div = 10V
Horizontal Resolution = 2µs/div

Figure 5. Primary Switch Node Waveform

6 Bill of Materials

Designator	Qty	Part Number	Description	Value
C1,2	2	C3225X7R1H225K	CAPACITOR, 1210 X7R CER, TDK	2.2µ, 50V
C3	1	C2012X7R2A104K	CAPACITOR, 0805 X7R CER, TDK	0.1µ, 100V
C4, 7	2	C2012X7R2A103K	CAPACITOR, 0805 X7R CER, TDK	0.01µ, 100V
C5	1	C0805C101M5RAC	CAPACITOR, 0805 COG CER, KEMET	100p, 50V
C6,14	2	C2012X7R1A105K	CAPACITOR, 0805 X7R CER, TDK	1µ, 10V
C8	1	C2012Y5V1A106Z	CAPACITOR, 0805 Y5V CER, TDK	10µ, 10V
C9	1	C2012X7R2A472K	CAPACITOR, 0805 X7R CER, TDK	4700p, 100V
C10	1	C0805C221M5RAC	CAPACITOR, 0805 COG CER, KEMET	220p, 50V
C11	1	C0805C471M5RAC	CAPACITOR, 0805 COG CER, KEMET	470p, 50V
C12,13	2	GRM32ER61A476KE20L	CAPACITOR, 1210 X5R CER, MURATA	47µ,10V
C19	1	CRCW20100000ZS	RESISTOR, 2010, VISHAY	0
D1	1	CMHSH-3	DIODE, SOD-123 SCHOTTKY, CENTRAL SEMI	200mA, 30V
D2	1	CMMR1U-2	DIODE, SOD-123F, CENTRAL SEMI	1A, 200V
D3	1	BAT54S	DIODE, SOT-23 SCHOTTKY, VISHAY	200mA, 30V
D4	1	CMSH5-40	DIODE, SMC SCHOTTKY, CENTRAL SEMI	5A, 40V
R1	1	CRCW08056042F	RESISTOR, 0805, VISHAY	60.4k
R2,12	2	CRCW080510R0F	RESISTOR, 0805, VISHAY	10
R3	1	CRCW08056041F	RESISTOR, 0805, VISHAY	6.04k
R4	1	CRCW08055232F	RESISTOR, 0805, VISHAY	52.3k
R5	1	CRCW080520R0F	RESISTOR, 0805, VISHAY	20
R6	1	CRCW08058061F	RESISTOR, 0805, VISHAY	8.06k
R7	1	CRCW08051003F	RESISTOR, 0805, VISHAY	100k
R8	1	CRCW08051302F	RESISTOR, 0805, VISHAY	13.0k
R9	1	CRCW08051022F	RESISTOR, 0805, VISHAY	10.2k
R10	1	CRCW08053401F	RESISTOR, 0805, VISHAY	3.40k
R11	1	CRCW20100000ZS	RESISTOR, 2010, VISHAY	0
T1	1	FA2636-AL	POWER XFR, COILCRAFT	160uH PRIMARY,8:3:2
U1	1	LM5001	REGULATOR, TEXAS INSTRUMENTS	
J1,2,3,4	4	7693	TERMINAL, 6-32 SCREW, 4 PIN, KEYSTONE	SNAP IN, PC MOUNT
J5,6,7,8	4	5002	TERMINAL, SINGLE PIN, KEYSTONE	TESTPOINT, LOOP

7 PCB Layout

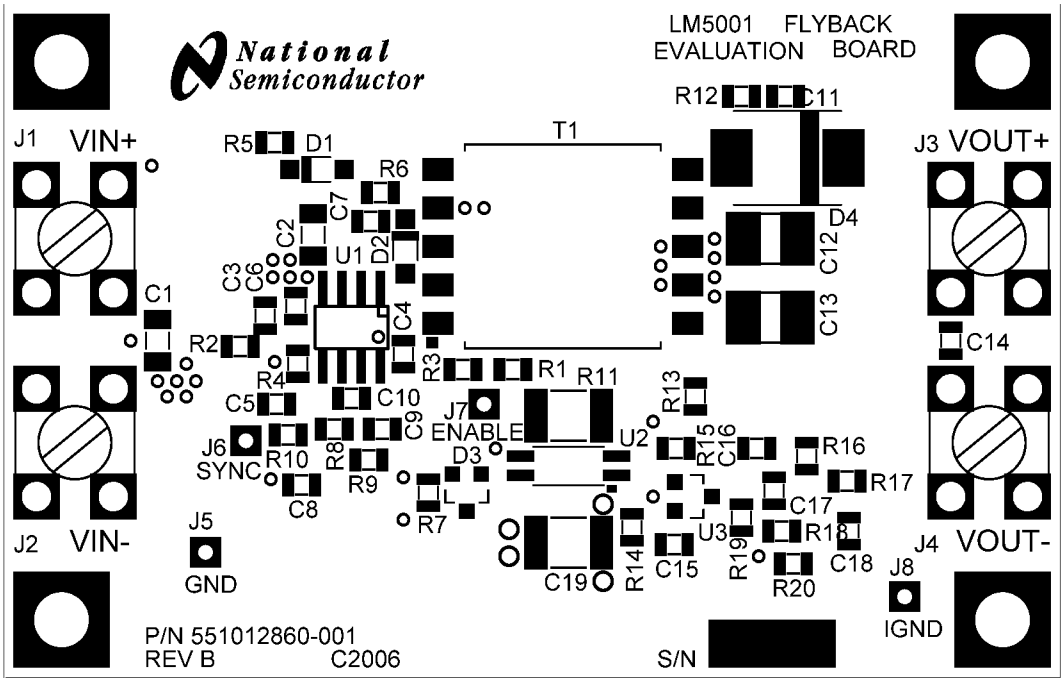


Figure 6. Silkscreen

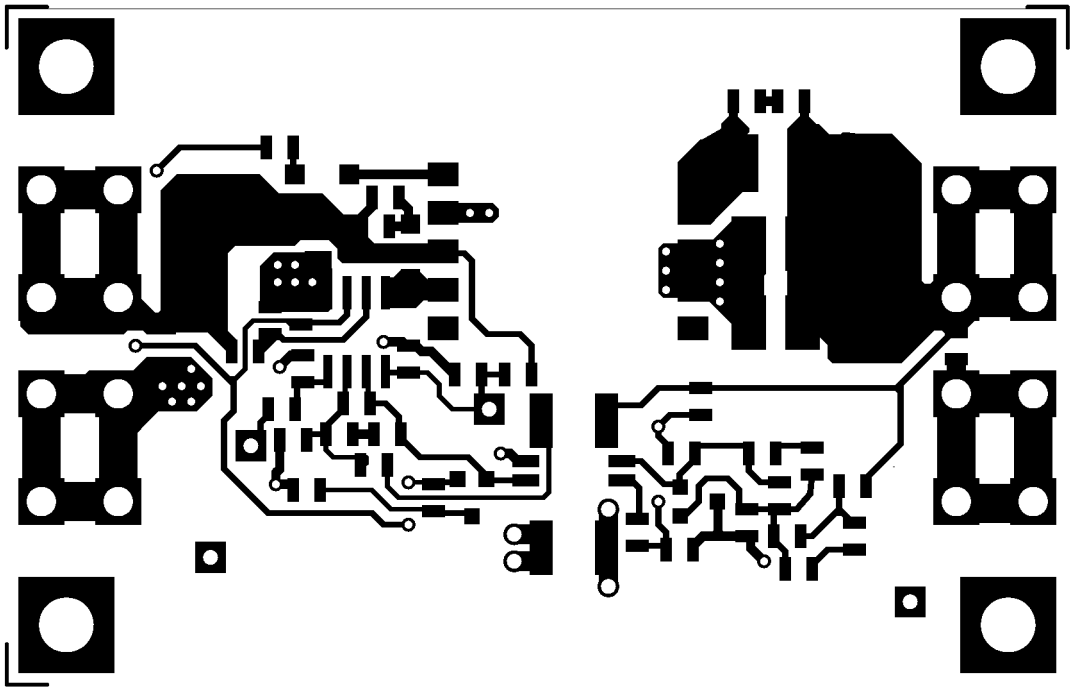


Figure 7. Component Side

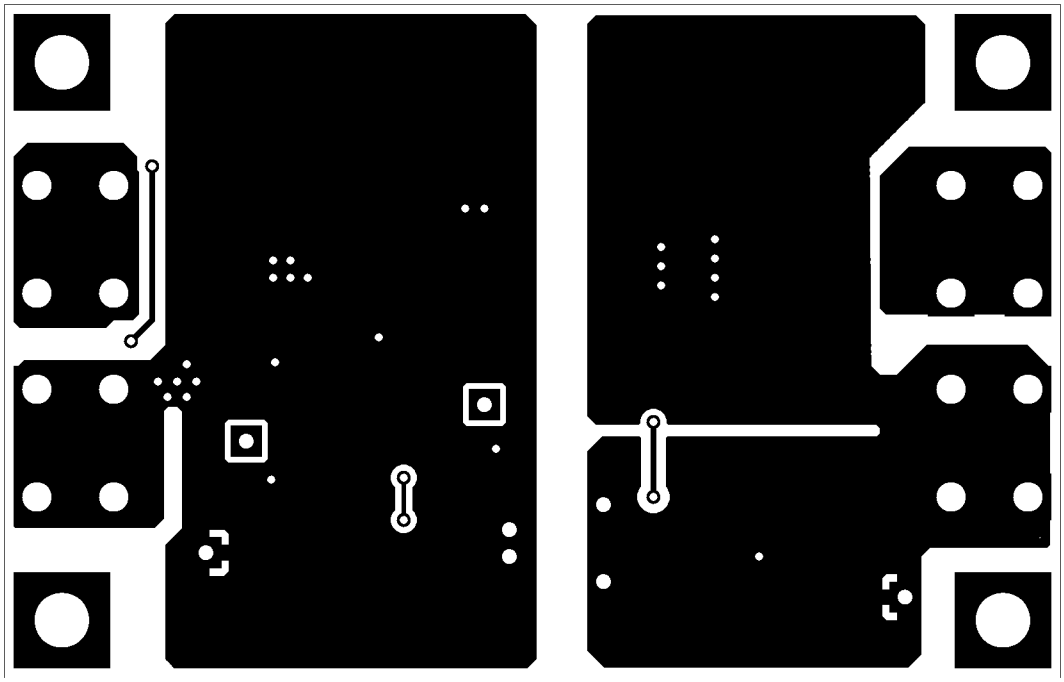


Figure 8. Solder Side

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