General Description

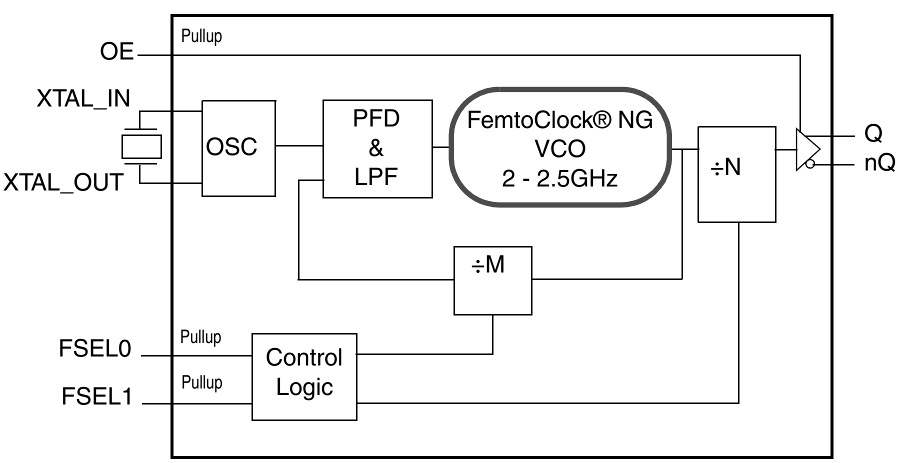
The IDT8N3PF10VA-159I is a programmable LVPECL synthesizer that is “forward” footprint compatible with standard 5mm x 7mm oscillators. The device uses IDT’s fourth generation FemtoClock® NG technology for an optimum of high clock frequency and low phase noise performance. Forward footprint compatibility means that a board designed to accommodate the crystal oscillator interface and the optional control pins is also fully compatible with a canned oscillator footprint - the canned oscillator will drop onto the 10-VFQFN footprint for second sourcing purposes. This capability provides designers with programability and lead time advantages of silicon/crystal based solutions while maintaining compatibility with industry standard 5mm x 7mm oscillator footprints for ease of supply chain management.

The IDT8N3PF10VA-159I generates four default frequencies 100MHz or 156.25MHz from a 25MHz fundamental mode crystal, or 212.5MHz or 106.25MHz from a 26.5625MHz fundamental mode crystal. The output frequency is selected by FSEL0 and FSEL1 pins.

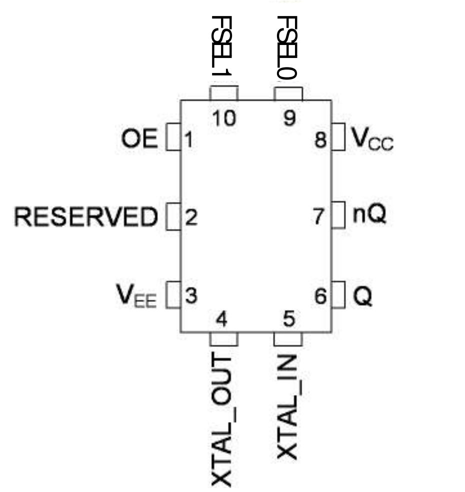
Features

- Fourth Generation FemtoClock® NG technology
- Footprint compatible with 5mm x 7mm differential oscillators
- Generates 100MHz or 156.25MHz from a 25MHz crystal, or 212.5MHz or 106.25MHz from a 26.5625MHz mode crystal
- One differential LVPECL output pair
- Crystal oscillator interface which can also be overdriven using a single-ended reference clock
- RMS phase jitter @ 156.25MHz, 10kHz – 1MHz: 0.201ps (typical)
- Full 3.3V or 2.5V operating supply
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

Block Diagram



Pin Assignment



IDT8N3PF10VA-159I

10-Lead VFQFN
5mm x 7mm x 1mm package body
ePAD size: 1.70mm x 3.70mm
NR Package
Top View

Table 1. Pin Descriptions

Number	Name	Type		Description
1	OE	Input	Pullup	Output enable. LVCMOS/LVTTL interface levels.
2	RESERVED	Reserved		Reserved pin. Do not connect.
3	V_{EE}	Power		Negative supply pin.
4, 5	XTAL_OUT XTAL_IN	Input		Crystal oscillator interface XTAL_IN is the input, XTAL_OUT is the output. Crystal oscillator interface which can also be overdriven using a single-ended reference clock.
6, 7	Q, nQ	Output		Differential output pair. LVPECL interface levels.
8	V_{CC}	Power		Power supply pin.
9	FSEL0	Input	Pullup	Output divider control inputs. Sets the output divider value to one of four values. See Table 3. LVCMOS/LVTTL interface levels.
10	FSEL1	Input	Pullup	Output divider control inputs. Sets the output divider value to one of four values. See Table 3. LVCMOS/LVTTL interface levels

NOTE: *Pullup* refers to internal input resistor. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ

Function Table

Table 3. Divider Function Table

FSEL[1:0]	Output (MHz)	Input Crystal (MHz)
0 0	100	25
0 1	156.25	25
1 0	212.5	26.5625
1 1 (default)	106.25	26.5625

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{CC}	3.63V
Inputs, V_I XTAL_IN Other Inputs	 0V to 2V -0.5V to V_{CC} + 0.5V
Outputs, I_O Continuous Current Surge Current	 50mA 100mA
Package Thermal Impedance, θ_{JA}	36.8°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, V_{CC} = 3.3V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Power Supply Voltage		3.135	3.3	3.465	V
I_{EE}	Power Supply Current			118	140	mA

Table 4B. Power Supply DC Characteristics, V_{CC} = 2.5V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Power Supply Voltage		2.375	2.5	2.625	V
I_{EE}	Power Supply Current			115	135	mA

Table 4C. LVCMOS/LVTTL DC Characteristics, V_{CC} = 3.3V ± 5% or 2.5V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{CC} = 3.465V	2		V_{CC} + 0.3	V
			V_{CC} = 2.625V	1.7		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage		V_{CC} = 3.465V	-0.3		0.8	V
			V_{CC} = 2.625V	-0.3		0.7	V
I_{IH}	Input High Current	OE, FSEL[1:0]	V_{CC} = V_{IN} = 3.465V or 2.625V			5	µA
I_{IL}	Input Low Current	OE, FSEL[1:0]	V_{CC} = 3.465V or 2.625V, V_{IN} = 0V	-150			µA

Table 4D. LVPECL DC Characteristics, V_{CC} = 3.3V ± 5% or 2.5V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CC} – 1.3		V_{CC} – 0.8	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CC} – 2.0		V_{CC} – 1.6	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs terminated with 50Ω to V_{CC} – 2V.

Table 5. Crystal Characteristics

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency			25		MHz
			26.5625		MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF

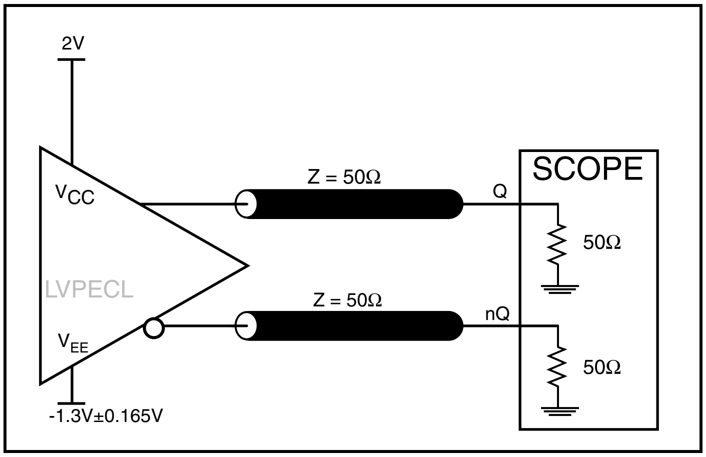
AC Electrical Characteristics

Table 6. AC Characteristics, V_{CC} = 3.3V ± 5% or 2.5V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

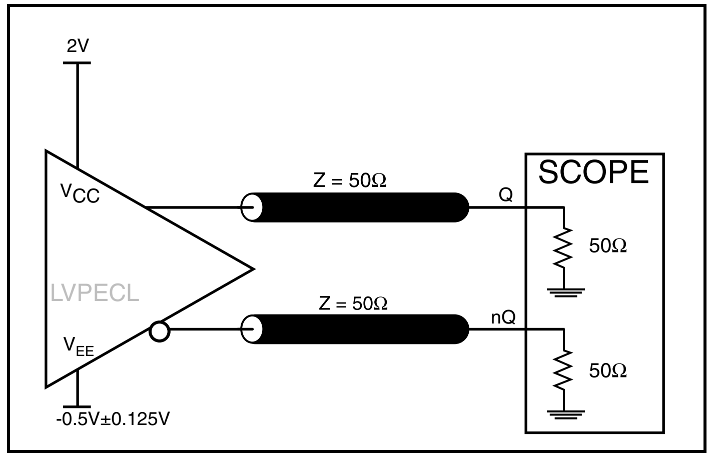
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
tjit(Ø)	RMS Phase Jitter (Random); NOTE 1	212.5MHz, Integration Range: 10kHz – 1MHz		0.197		ps
		156.25MHz, Integration Range: 10kHz – 1MHz		0.201		ps
		156.25MHz, Integration Range: 12kHz – 20MHz		0.300		ps
		106.25MHz, Integration Range: 12kHz – 20MHz		0.285		ps
		100MHz, Integration Range: 12kHz – 20MHz		0.276		ps
tjit(cc)	Cycle-to-Cycle Jitter; NOTE 2				20	ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	100		400	ps
odc	Output Duty Cycle		48		52	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE: Characterized using a 25MHz, 12pF resonant crystal.
NOTE 1: Please refer to the Phase Noise plots.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.

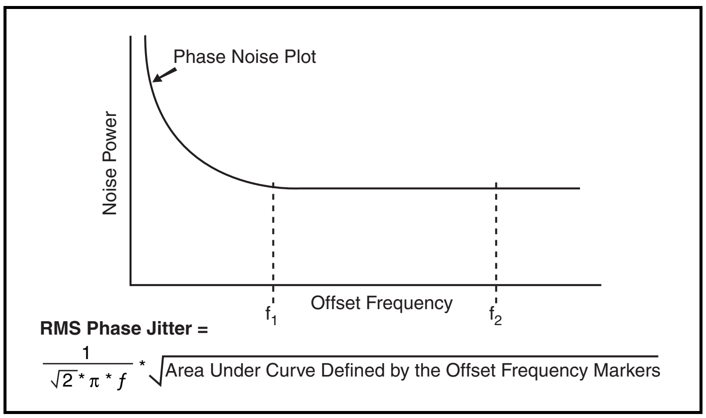
Parameter Measurement Information



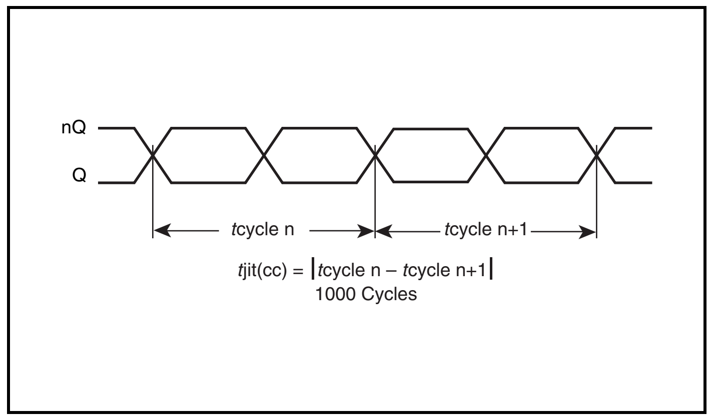
3.3V LVPECL Output Load Test Circuit



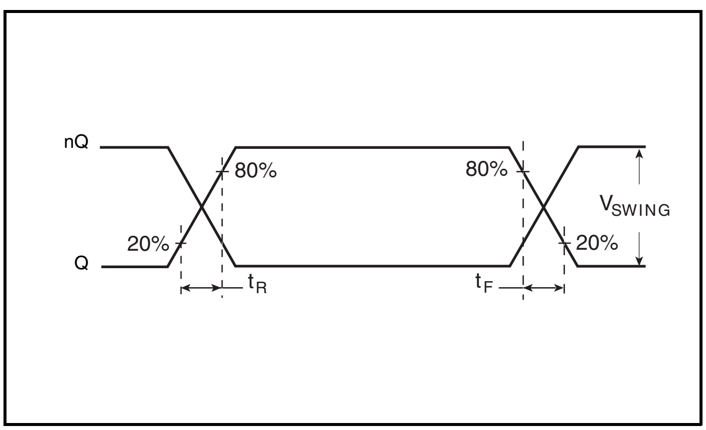
2.5V LVPECL Output Load Test Circuit



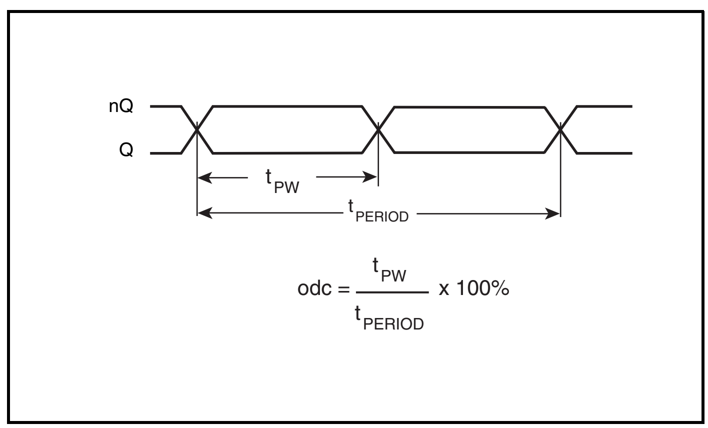
RMS Phase Jitter



Cycle-to-Cycle Jitter

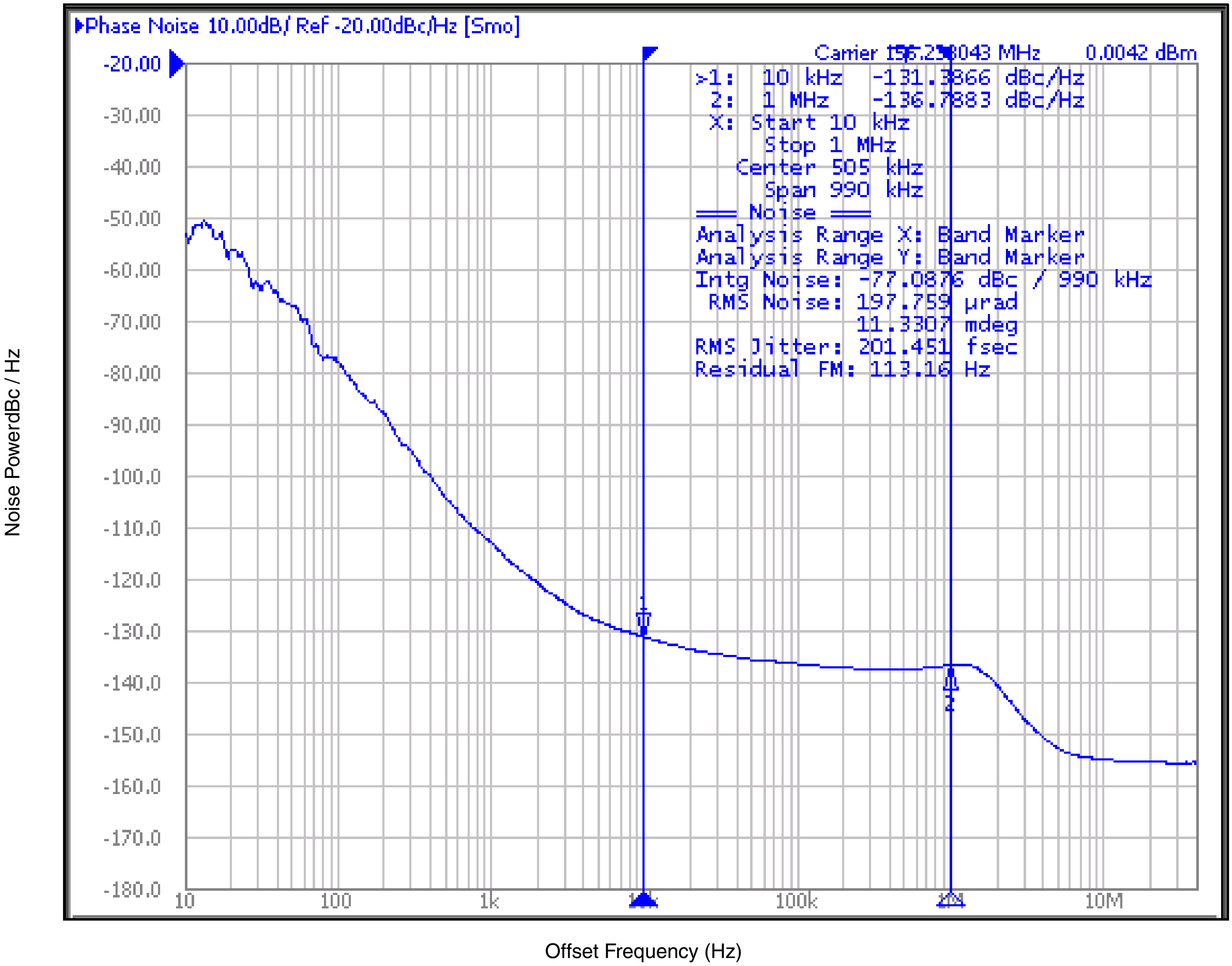


Output Rise/Fall Time



Output Duty Cycle/Pulse Width/Period

Phase Jitter Plot at 156.25MHz (3.3V)



Applications Information

Overdriving the XTAL Interface

The XTAL_IN input can be overdriven by an LVCMOS driver or by one side of a differential driver through an AC coupling capacitor. The XTAL_OUT pin can be left floating. The amplitude of the input signal should be between 500mV and 1.8V and the slew rate should not be less than 0.2V/nS. For 3.3V LVCMOS inputs, the amplitude must be reduced from full swing to at least half the swing in order to prevent signal interference with the power rail and to reduce internal noise. *Figure 1A* shows an example of the interface diagram for a high speed 3.3V LVCMOS driver. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and changing R2 to 50Ω. The values of the resistors can be increased to reduce the loading for a slower and weaker LVCMOS driver. *Figure 1B* shows an example of the interface diagram for an LVPECL driver. This is a standard LVPECL termination with one side of the driver feeding the XTAL_IN input. It is recommended that all components in the schematics be placed in the layout. Though some components might not be used, they can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a quartz crystal as the input.

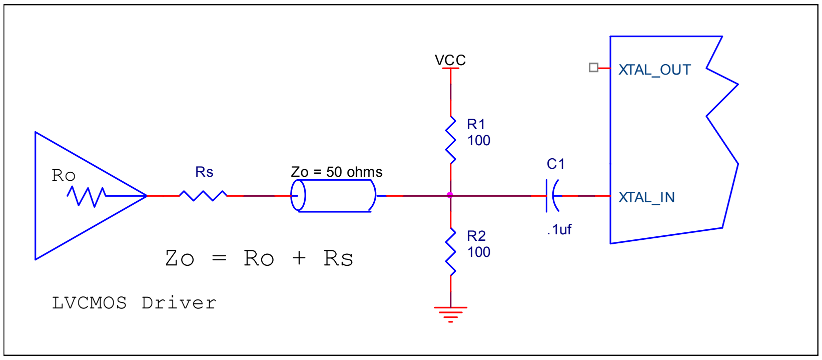


Figure 1A. General Diagram for LVCMOS Driver to XTAL Input Interface

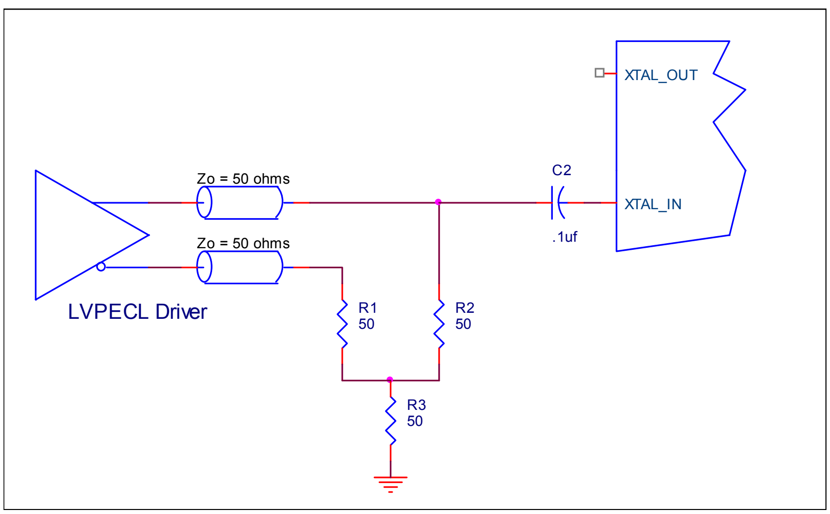


Figure 1B. General Diagram for LVPECL Driver to XTAL Input Interface

Recommendations for Unused Input Pins

Inputs:

LVCMOS Control Pins

All control pins have internal pullups; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 2A and 2B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

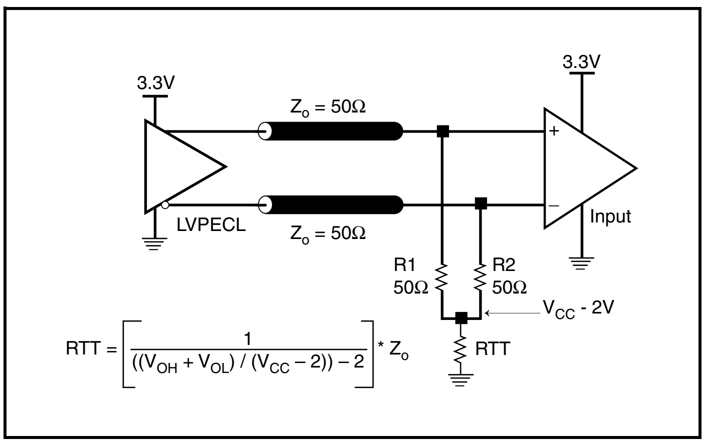


Figure 2A. 3.3V LVPECL Output Termination

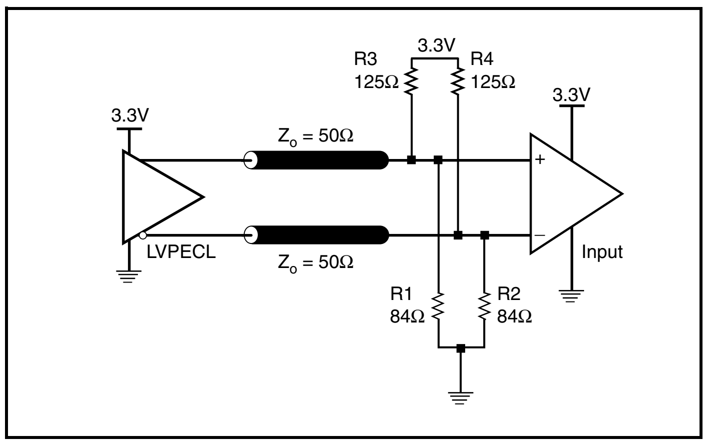


Figure 2B. 3.3V LVPECL Output Termination

Termination for 2.5V LVPECL Outputs

Figure 3A and *Figure 3B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{CC} – 2V. For V_{CC} = 2.5V, the V_{CC} – 2V is very close to ground level. The R3 in Figure 3B can be eliminated and the termination is shown in *Figure 3C.*

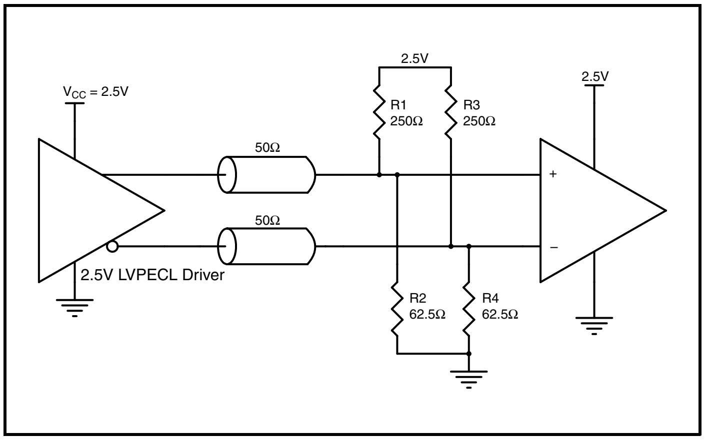


Figure 3A. 2.5V LVPECL Driver Termination Example

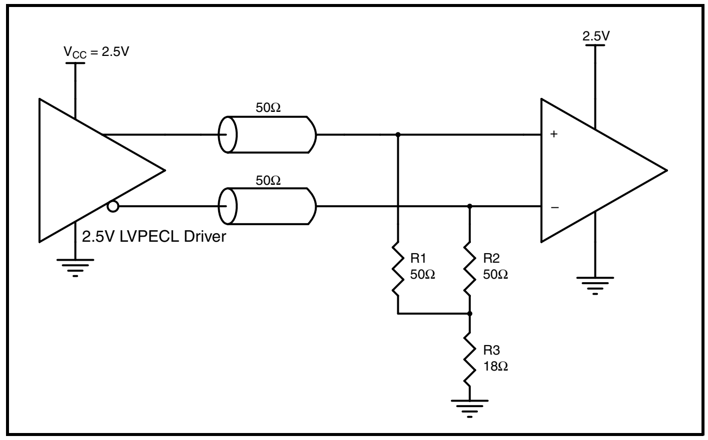


Figure 3B. 2.5V LVPECL Driver Termination Example

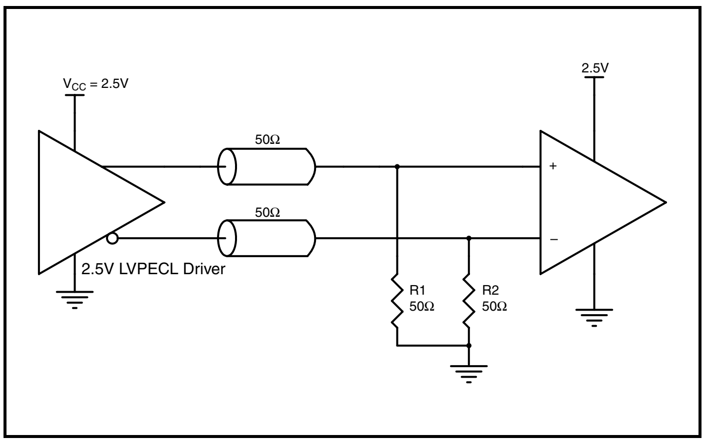


Figure 3C. 2.5V LVPECL Driver Termination Example

VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 4.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/ Electrically Enhance Leadframe Base Package, Amkor Technology.

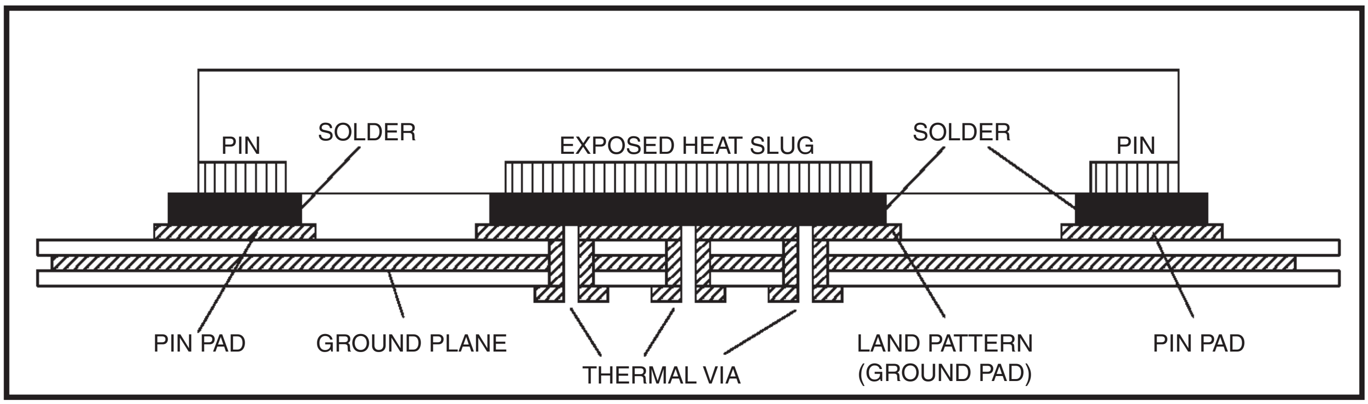


Figure 4. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)

Schematic Layout

Figure 5 (next page) shows an example of IDT8N3PF10VA-159I application schematic in which the device is operated at V_{CC} = 3.3V. The schematic example focuses on functional connections and is intended as an example only and may not represent the exact user configuration. Refer to the pin description and functional tables in the datasheet to ensure the logic control inputs are properly set. For example OE, FSET0 and FSEL1 can be configured from an FPGA instead of pull up and pull down resistors as shown.

There are two LVPECL termination options shown; the simple three resistor termination of R5, R6 and R7 and an AC termination, used when coupling the IDT8N3PF10VA-159I LVPECL output stage to a different logic family receiver. Note that the pull down resistors R8 and R9 that bias the LVPECL output stage are to be placed on the IDT8N3PF10VA-159I side of the PCB directly adjacent to pins 6 and 7 for best signal integrity. Most often each output of a 3.3V LVPECL driver will be DC terminated with a 130Ω pull up and an 82 ohm pull down resistor at the 3.3V LVPECL receiver. This is also a valid option with the IDT8N3PF10VA-159I, though the three resistor termination is simpler in regard to component count and layout as well as lower in power dissipation.

NOTE: This device package has an ePAD that is connected to ground internally. Though not necessary, the ePAD should be connected to GND on the PCB through vias in order to improve heat dissipation. If not connected, the area below the ePAD must be treated as a keep-out region.

As with any high speed analog circuitry, the power supply pins are vulnerable to random noise, so to achieve optimum jitter performance isolation of the V_{CC} pin from power supply is required. In order to achieve the best possible filtering, it is recommended that the placement of the filter components be on the device side of the PCB as close to the power pins as possible. If space is limited, the 0.1uF capacitor on the V_{CC} pin must be placed on the device side with direct return to the ground plane though vias. The remaining filter components can be on the opposite side of the PCB.

Power supply filter component recommendations are a general guideline to be used for reducing external noise from coupling into the devices. The filter performance is designed for a wide range of noise frequencies. This low-pass filter starts to attenuate noise at approximately 10kHz. If a specific frequency noise component is known, such as switching power supplies frequencies, it is recommended that component values be adjusted and if required, additional filtering be added. Additionally, good general design practices for power plane voltage stability suggests adding bulk capacitance in the local area of all devices.

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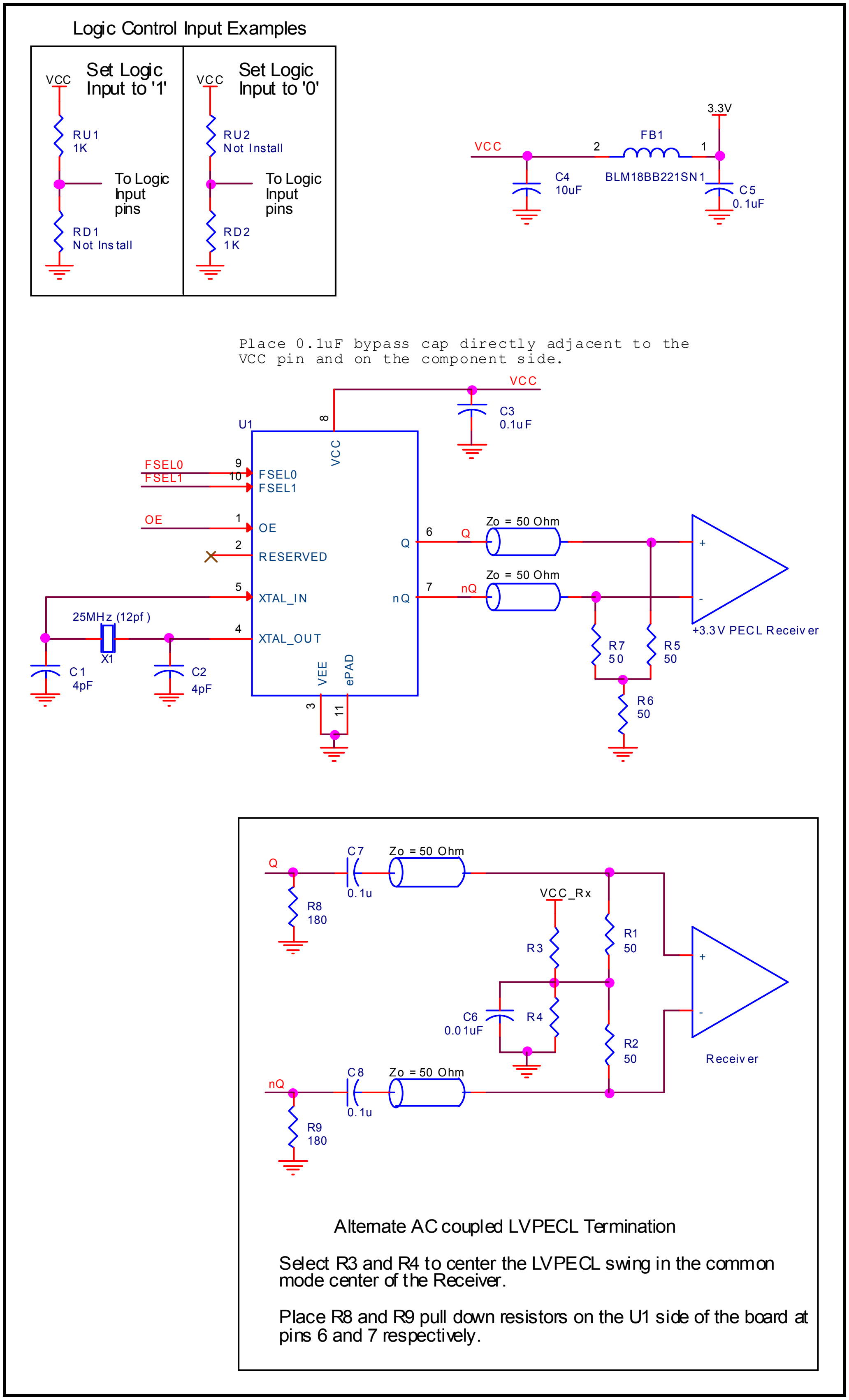


Figure 5. IDT8N3PF10VA-159I Application Schematic

Power Considerations

This section provides information on power dissipation and junction temperature for the IDT8N3PF10VA-159I.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the IDT8N3PF10VA-159I is the sum of the core power plus the power dissipation in the load(s).
The following is the power dissipation for V_{CC} = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipation in the load.

- Power $(core)_{MAX}$ = V_{CC_MAX} * I_{EE_MAX} = 3.465V * 140mA = **485.1mW**
- Power $(outputs)_{MAX}$ = **32mW/Loaded Output pair**

Total Power$_{\_MAX}$ (3.465V, with all outputs switching) = 485.1mW + 32mW = **517.1mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad, and directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 36.8°C/W per Table 7 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.517W * 36.8°C/W = 104°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 7. Thermal Resistance θ_{JA} for 10 Lead VFQFN, Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	36.8°C/W	31.7°C/W	30.1°C/W

3. Calculations and Equations.

The purpose of this section is to calculate the power dissipation for the LVPECL output pair.

The LVPECL output driver circuit and termination are shown in *Figure 6.*

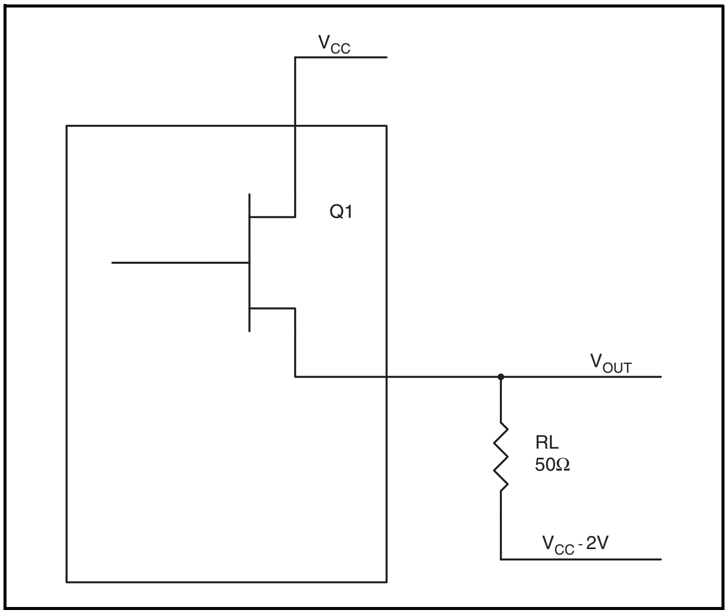


Figure 6. LVPECL Driver Circuit and Termination

To calculate power dissipation per output pair due to loading, use the following equations which assume a 50Ω load, and a termination voltage of $V_{CC} – 2V$.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CC\_MAX} – 0.8V}$
  $(V_{CC\_MAX} – V_{OH\_MAX}) = \mathbf{0.8V}$
- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CC\_MAX} – 1.6V}$
  $(V_{CC\_MAX} – V_{OL\_MAX}) = \mathbf{1.6V}$

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

Pd_H = $[(V_{OH\_MAX} – (V_{CC\_MAX} – 2V))/R_L] * (V_{CC\_MAX} – V_{OH\_MAX}) = [(2V – (V_{CC\_MAX} – V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} – V_{OH\_MAX}) =$
$[(2V – 0.8V)/50\Omega] * 0.8V =$ **19.2mW**

Pd_L = $[(V_{OL\_MAX} – (V_{CC\_MAX} – 2V))/R_L] * (V_{CC\_MAX} – V_{OL\_MAX}) = [(2V – (V_{CC\_MAX} – V_{OL\_MAX}))/R_L] * (V_{CC\_MAX} – V_{OL\_MAX}) =$
$[(2V – 1.6V)/50\Omega] * 1.6V =$ **12.8mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **32mW**

Reliability Information

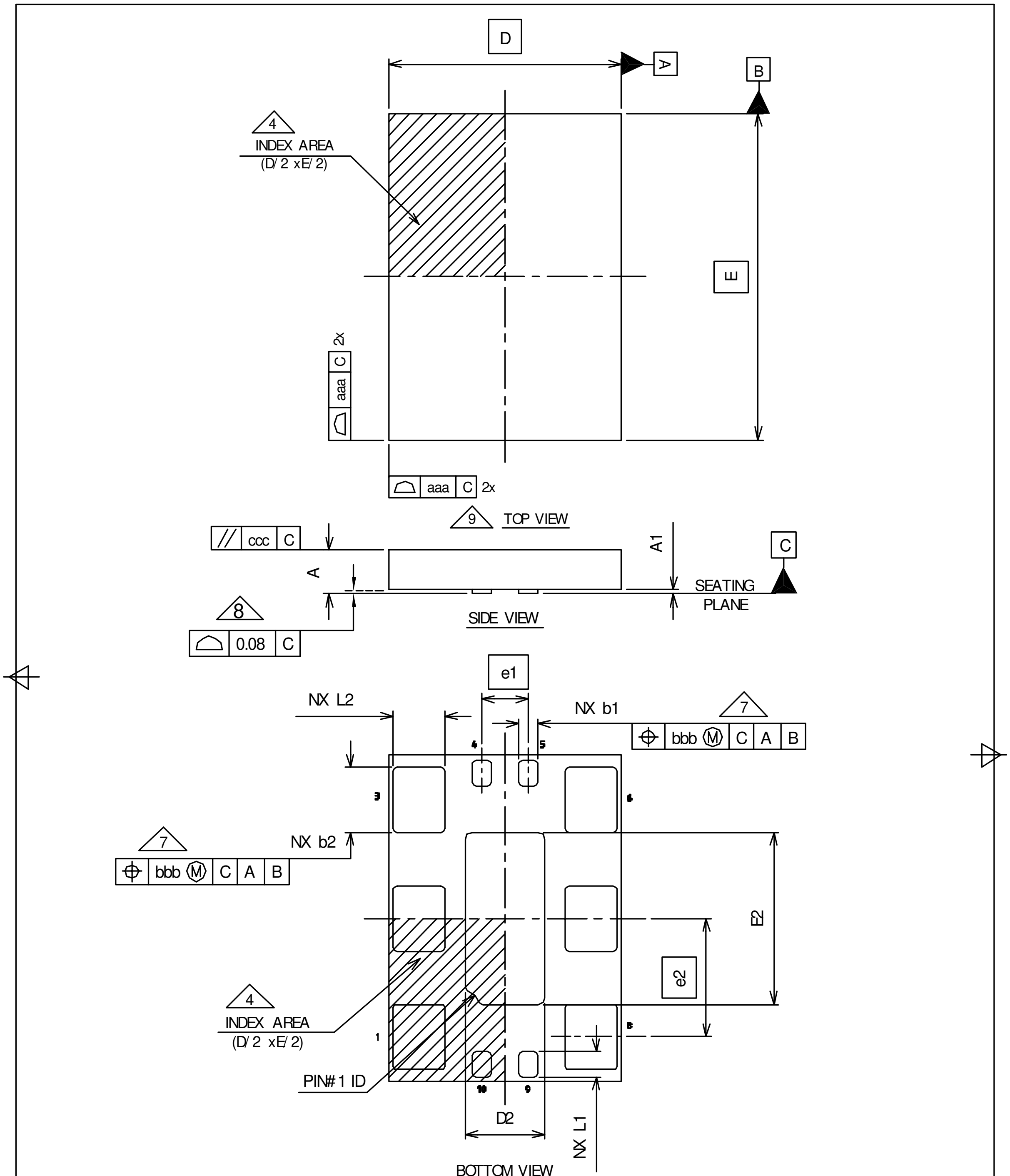
Table 8. θ_{JA} vs. Air Flow Table for a 10 Lead VFQFN

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	36.8°C/W	31.7°C/W	30.1°C/W

Transistor Count

The transistor count for IDT8N3PF10VA-159I is: 47,515

10 Lead VFQFN, NR Suffix Package Outline



FOR REVISION UPDATE PLEASE REFER TO HISTORY OF CHANGES.

DRAFT	ORIGINATOR	ZAHRUL		DWG. NO : PKGML00305
1				MLP QUAD PACKAGE OUTLINE 5.00x7.00 MLPQ 10LD 1.00/2.54 Pitch
	ENGINEERING MANAGER			
	TOOLING MANAGER	ARAVEN		
	TECH. SALES MANAGER	KANDA		
	DATE	2007-APR-18		Page 1 Of 4

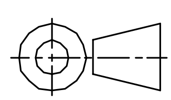
10 Lead VFQFN, NR Suffix Package Outline, continued

COMMON DIMENSION						
	TOLERANCE OF FORM AND POSITION					
aaa	0.15					
bbb	0.10					
ccc	0.10					

COMMON DIMENSION			
SYMBOL	V : Very thin		
	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
NOTES	1, 2	1, 2	1, 2

Summary Table				
Lead Pitch (e1 & e2)	Lead Count	Body Size	Very Very Thin Variation	Pin #1 ID
1.00/ 2.54	10	5.00X7.00	VNJR-1	R0.30

FOR REVISION UPDATE PLEASE REFER TO HISTORY OF CHANGES.

DRAFT 1	ORIGINATOR	ZAHRUL		DWG. NO : PKGML00305
				MLP QUAD PACKAGE OUTLINE 5.00x7.00 MLPQ 10LD 1.00/ 2.54 Pitch
	ENGINEERING MANAGER			
	TOOLING MANAGER	ARAVEN		
	TECH. SALES MANAGER	KANDA		
	DATE	2007-APR-18		PAGE: 2 of 4

10 Lead VFQFN, NR Suffix Package Outline, continued

NOTE:

1. Dimensioning and tolerancing conform to ASME Y14.5M-1994.

2. All dimensions are in millimeters, angles are in degrees(°).

3. N is the total number of terminals.

4. The location of the terminal #1 identifier and terminal numbering convention conforms to JEDEC publication 95 SPP-002.

5. ND and NE refer to the number of terminals on each D and E side respectively.

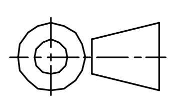
6. NJR refers to NON JEDEC REGISTERED

7. Dimension b applies to metallized terminal and is measured between 0.10mm and 0.30mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension b should not be measured in that radius area.

8. Coplanarity applies to the terminals and all other bottom surface metallization.

9. Drawing shown are for illustration only.

FOR REVISION UPDATE PLEASE REFER TO HISTORY OF CHANGES.

DRAFT 1	ORIGINATOR	ZAHRUL		DWG. NO : PKGML00305
				MLP QUAD PACKAGE OUTLINE 5.00x7.00 MLPQ 10LD 1.00/2.54 Pitch
	ENGINEERING MANAGER			
	TOOLING MANAGER	ARAVEN		
	TECH. SALES MANAGER	KANDA		
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10 Lead VFQFN, NR Suffix Package Outline, continued

Variation / Symbol		VNJR-1									Note
D BSC		5.00									
E BSC		7.00									
b1	MIN	0.35									
	NOM	0.40									
	MAX	0.45									
b2	MIN	1.35									
	NOM	1.40									
	MAX	1.45									
D2	MIN	1.55									
	NOM	1.70									
	MAX	1.80									
E2	MIN	3.55									
	NOM	3.70									
	MAX	3.80									
L1	MIN	0.45									
	NOM	0.55									
	MAX	0.65									
L2	MIN	1.00									
	NOM	1.10									
	MAX	1.20									
N		10									
ND		2									
NE		3									
NOTES		-									
PAD DESIGN		-									

FOR REVISION UPDATE PLEASE REFER TO HISTORY OF CHANGES.

DRAFT 1	ORIGINATOR	ZAHRUL	DWG. NO : PKGML00305
			MLP QUAD PACKAGE OUTLINE 5.00x7.00 MLPQ 10LD 1.00/2.54 Pitch
	ENGINEERING MANAGER		
	TOOLING MANAGER	ARAVEN	
	TECH. SALES MANAGER	KANDA	
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Ordering Information

Table 9. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8N3PF10VA-159NRGI	IDT8N3PF10VA-159NRGI	“Lead-Free” 10 Lead VFQFN	Tray	-40°C to 85°C
8N3PF10VA-159NRGI	IDT8N3PF10VA-159NRGI	“Lead-Free” 10 Lead VFQFN	Tape & Reel	-40°C to 85°C

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Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/