

# **N-Channel Power MOSFET**

 $30V, 55A, 8m\Omega$ 

#### **FEATURES**

- Fast switching
- 100% EAS Guaranteed
- Green Device Available
- G-S ESD Protection Diode Embedded

#### **APPLICATION**

- Vcore / MB
- **POL Application**
- SMPS 2<sup>nd</sup> SR

KEY PERFORMANCE PARAMETERS				
PARAMETER		VALUE	UNIT	
$V_{DS}$		30	V	
R <sub>DS(on)</sub> (max)	$V_{GS} = 10V$	8	mΩ	
	$V_{GS} = 4.5V$	12.5		
$Q_{g}$		7.5	nC	

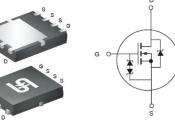






Version: B15





Notes: Moisture sensitivity level: level 3. Per J-STD-020

ABSOLUTE MAXIMUM RATINGS (T <sub>A</sub> = 25°C unless otherwise noted)				
PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-Source Voltage	V <sub>DS</sub>	30	V	
Gate-Source Voltage	$V_{GS}$	±20	V	
Continuous Drain Current (Note 1)		55	_	
T <sub>C</sub> = -	100°C	35	A	
Pulsed Drain Current (Note 2)	I <sub>DM</sub>	220	Α	
Total Power Dissipation @ T <sub>C</sub> = 25°C	P <sub>DTOT</sub>	54	W	
Single Pulsed Avalanche Energy (Note 3)	E <sub>AS</sub>	45	mJ	
Single Pulsed Avalanche Current (Note 3)	I <sub>AS</sub>	30	Α	
Operating Junction and Storage Temperature Range	e T <sub>J</sub> , T <sub>STG</sub>	- 55 to +150	°C	

THERMAL PERFORMANCE				
PARAMETER	SYMBOL	LIMIT	UNIT	
Junction to Case Thermal Resistance	R <sub>eJC</sub>	2.3	°C/W	
Junction to Ambient Thermal Resistance	$R_{\Theta JA}$	62	°C/W	

Notes: ReJA is the sum of the junction-to-case and case-to-ambient thermal resistances. The case thermal reference is defined at the solder mounting surface of the drain pins.  $R_{\Theta JA}$  is guaranteed by design while  $R_{\Theta CA}$  is determined by the user's board design.  $R_{\Theta JA}$  shown below for single device operation on FR-4 PCB in still air.





<b>ELECTRICAL SPECIFICATIONS</b> (T <sub>A</sub> = 25°C unless otherwise noted)						
PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
Static (Note 4)						
Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A$	BV <sub>DSS</sub>	30			V
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250 \mu A$	$V_{GS(TH)}$	1	1.6	2.5	V
Gate Body Leakage	$V_{GS} = \pm 20V, V_{DS} = 0V$	I <sub>GSS</sub>			±10	μΑ
Zero Gate Voltage Drain Current	$V_{DS} = 30V$ , $V_{GS} = 0V$	I <sub>DSS</sub>			1	μΑ
Drain-Source On-State Resistance	$V_{GS} = 10V, I_D = 16A$	Б		6.5	8	mΩ
	$V_{GS} = 4.5V, I_D = 8A$	$R_{DS(on)}$		9.5	12.5	mΩ
Dynamic (Note 5)						
Total Gate Charge	$V_{DS} = 15V, I_D = 20A,$ $V_{GS} = 4.5V$	$Q_g$		7.5		
Gate-Source Charge		$Q_gs$		1.3		nC
Gate-Drain Charge		$Q_{gd}$		4.5		
Input Capacitance	$V_{DS} = 25V, V_{GS} = 0V,$ f = 1.0MHz	C <sub>iss</sub>		750		
Output Capacitance		C <sub>oss</sub>		150		pF
Reverse Transfer Capacitance		C <sub>rss</sub>		110		
Gate Resistance	F = 1MHz, open drain	$R_g$		2.7		Ω
Switching (Note 6)						
Turn-On Delay Time	$V_{DD} = 15V,$ $R_{GEN} = 3.3\Omega,$ $I_{D} = 15A, V_{GS} = 10V,$	t <sub>d(on)</sub>		4.8		
Turn-On Rise Time		t <sub>r</sub>		12.5		
Turn-Off Delay Time		t <sub>d(off)</sub>		27.6		ns
Turn-Off Fall Time		t <sub>f</sub>		8.2		
Source-Drain Diode (Note 4)						
Forward On Voltage	I <sub>S</sub> = 1A, V <sub>GS</sub> = 0V	$V_{SD}$			1	V

#### Notes:

- 1. Current limited by package
- 2. Pulse width limited by the maximum junction temperature
- 3.  $L=0.1mH,\ I_{AS}=30A,\ V_{DD}=25V,\ R_G=25\Omega,\ Starting\ T_J=25^{\circ}C$
- 4. Pulse test: PW  $\leq$  300 $\mu$ s, duty cycle  $\leq$  2%
- 5. For DESIGN AID ONLY, not subject to production testing.
- 6. Switching time is essentially independent of operating temperature.



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### **ORDERING INFORMATION**

PART NO.	PACKAGE	PACKING
TSM080N03EPQ56 RLG	PDFN56	2,500pcs / 13" Reel

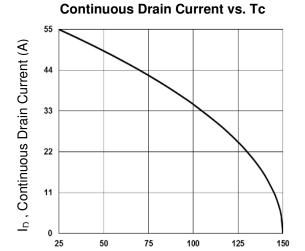
#### Note:

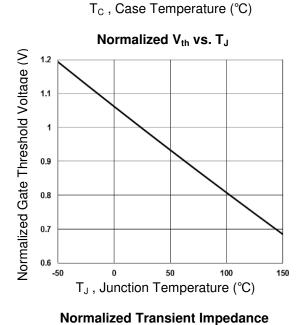
- 1. Compliant to RoHS Directive 2011/65/EU and in accordance to WEEE 2002/96/EC
- 2. Halogen-free according to IEC 61249-2-21 definition

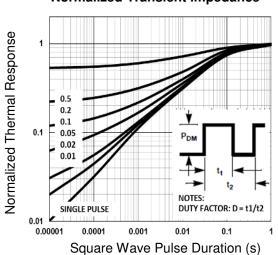


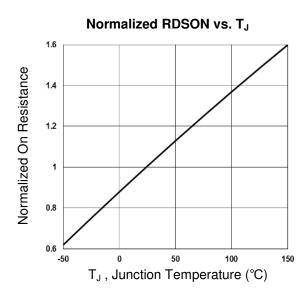
#### CHARACTERISTICS CURVES

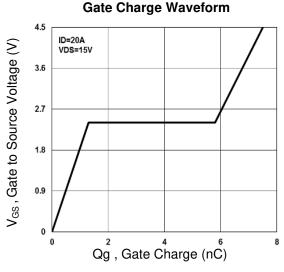
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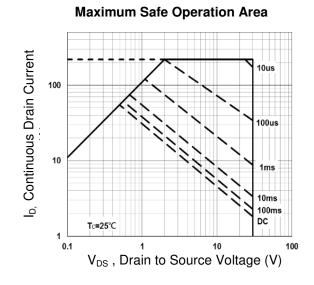






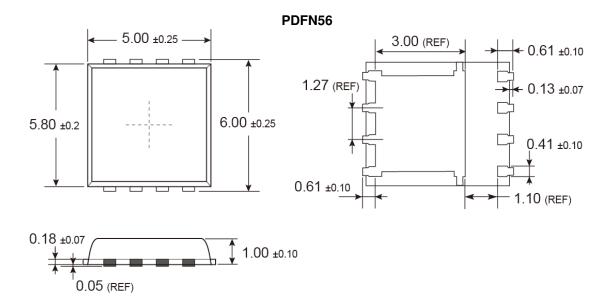




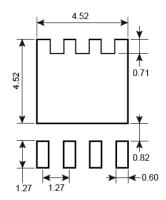




# PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)



# **SUGGESTED PAD LAYOUT (Unit: Millimeters)**



## **MARKING DIAGRAM**



Y = Year Code

M = Month Code for Halogen Free Product

O =Jan P =Feb Q =Mar R =Apr S =May T =Jun U =Jul V =Aug

W = Sep X = Oct Y = Nov Z = Dec

**L** = Lot Code  $(1 \sim 9, A \sim Z)$ 



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