CPMF-1200-S080B

Z-FET™ Silicon Carbide MOSFET

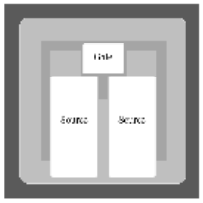
N-Channel Enhancement Mode
Bare Die

V_{DS}	= 1200 V
$R_{DS(on)}$	= 80 mΩ
Q_g	= 90.8 nC

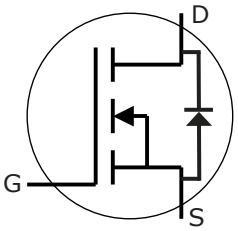
Features

- Industry Leading $R_{DS(on)}$
- High Speed Switching
- Low Capacitances
- Easy to Parallel
- Simple to Drive
- Lead-Free

Package



DIE



Part Number	Package
CPMF-1200-S080B	DIE

Benefits

- Higher System Efficiency
- Reduced Cooling Requirements
- Avalanche Ruggedness
- Increase System Switching Frequency

Applications

- Solar Inverters
- Motor Drives
- Military and Aerospace

Maximum Ratings

Symbol	Parameter	Value	Unit	Test Conditions	Note
I_D	Continuous Drain Current	50	A	V_{GS}@20V, T_J = 25°C	1
		30		V_{GS}@20V, T_J = 100°C	
I_{Dpulse}	Pulsed Drain Current	90	A	Pulse width t_P limited by T_{jmax} T_J = 25°C, tp = 1ms	1
E_{AS}	Single Pulse Avalanche Energy	2.2	J	I_D = 20A, V_{DD} = 50 V, L = 9.5 mH	
E_{AR}	Repetitive Avalanche Energy	1.5	J	t_{AR} limited by T_{jmax}	
I_{AR}	Repetitive Avalanche Current	20	A	I_D = 20A, V_{DD} = 50 V, L = 3 mH t_{AR} limited by T_{jmax}	
V_{GS}	Gate Source Voltage	-5/+25	V		
P_{tot}	Power Dissipation	313	W	T_j=25°C	1
T_J , T_{stg}	Operating Junction and Storage Temperature	-55 to +150	°C		
T_L	Solder Temperature	260	°C	1.6mm (0.063”) from case for 10s	

Note:
1. Assumes a thermal resistance junction to case of ≤ 0.4 °C/W.

Electrical Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions	Note
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	1200			V	V_{GS} = 0V, I_D = 100μA	
$V_{GS(th)}$	Gate Threshold Voltage		2.5	4	V	V_{DS} = V_{GS}, I_D = 1mA, T_J = 25ºC	2
			1.7			V_{DS} = V_{GS}, I_D = 1mA, T_J = 150ºC	
I_{DSS}	Zero Gate Voltage Drain Current		1	100	μA	V_{DS} = 1200V, V_{GS} = 0V, T_J = 25ºC	
			10	265		V_{DS} = 1200V, V_{GS} = 0V, T_J = 150ºC	
I_{GSS}	Gate-Source Leakage Current			250	nA	V_{GS} = 20V, V_{DS} = 0V	
$R_{DS(on)}$	Drain-Source On-State Resistance		80	110	mΩ	V_{GS} = 20V, I_D = 20A, T_J = 25ºC	
			110	140		V_{GS} = 20V, I_D = 20A, T_J = 150ºC	
g_{fs}	Transconductance		7.3		S	V_{DS}= 20V, I_{DS}= 20A, T_J = 25ºC	fig. 3
			6.7			V_{DS}= 20V, I_{DS}= 20A, T_J = 150ºC	
C_{iss}	Input Capacitance		1915		pF	V_{GS} = 0V V_{DS} = 800V f = 1MHz V_{AC} = 25mV	fig. 5
C_{oss}	Output Capacitance		120				
C_{rss}	Reverse Transfer Capacitance		13				
$t_{d(on)i}$	Turn-On Delay Time		17.2		ns	V_{DD} = 800V V_{GS} = -2/20V I_D = 20A R_G = 6.8Ω L = 856μH Per JEDEC24 Page 27	fig. 11
t_r	Rise Time		13.6				
$t_{d(off)i}$	Turn-Off Delay Time		62				
t_{fi}	Fall Time		35.6				
E_{ON}	Turn-On Switching Loss (25ºC) (150ºC)		530 410		μJ		
E_{Off}	Turn-Off Switching Loss (25ºC) (150ºC)		320 345		μJ		
R_G	Internal Gate Resistance		5		Ω	V_{GS} = 0V, f = 1MHz, V_{AC} = 25mV	

Note: 2. The recommended on-state VGS is +20V and the recommended off-state VGS is between 0V and -5V

Reverse Diode Characteristics

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
V_{sd}	Diode Forward Voltage	3.5		V	V_{GS} = -5V, I_F=10A, T_J = 25ºC	
		3.1			V_{GS} = -2V, I_F=10A, T_J = 25ºC	
t_{rr}	Reverse Recovery Time	220		ns	V_{GS} = -5V, I_F=20A, T_J = 25ºC V_R = 800V, di_F/dt= 100A/μs	fig. 12,13
Q_{rr}	Reverse Recovery Charge	142		nC		
I_{rrm}	Peak Reverse Recovery Current	2.3		A		

Gate Charge Characteristics

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
Q_{gs}	Gate to Source Charge	23.8		nC	V_{DD} = 800V I_D =20A V_{GS} = -2/20V Per JEDEC24-2	fig.8
Q_{gd}	Gate to Drain Charge	43.1				
Q_g	Gate Charge Total	90.8				

Typical Performance

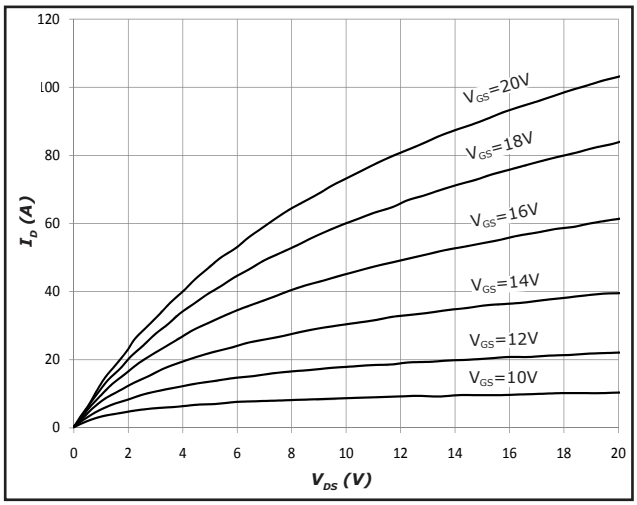


Fig 1. Typical Output Characteristics T_J = 25ºC

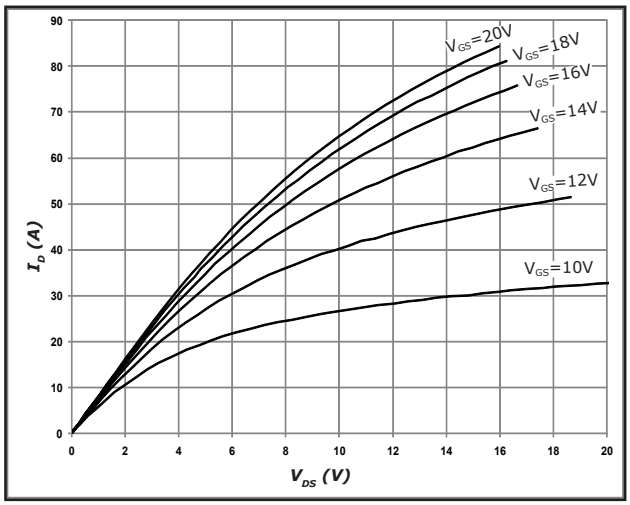


Fig 2. Typical Output Characteristics T_J = 150ºC

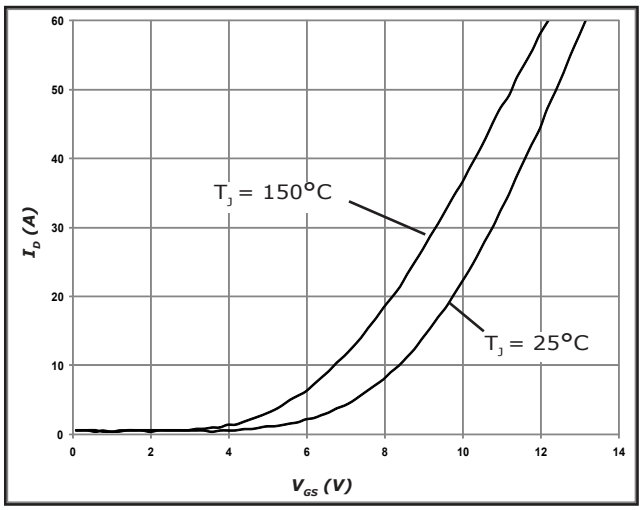


Figure 3. Typical Transfer Characteristics

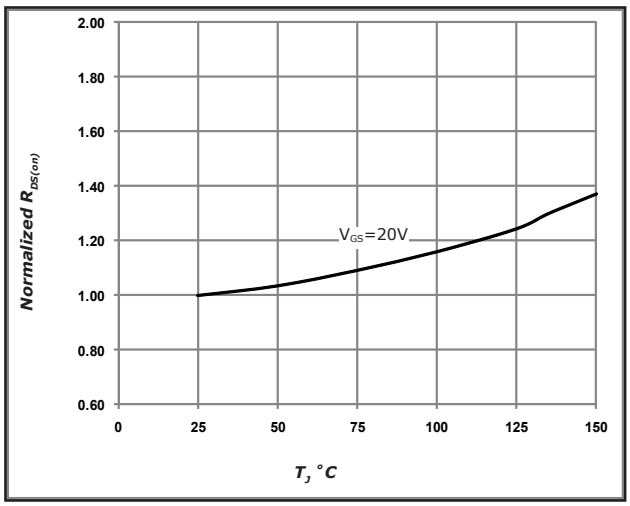
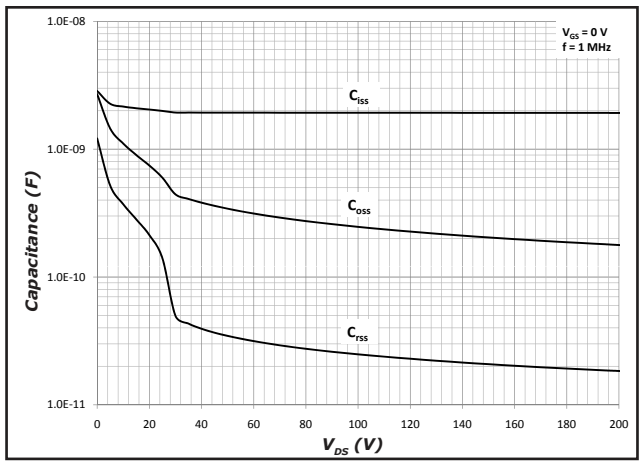


Fig 4. Normalized On-Resistance vs. Temperature



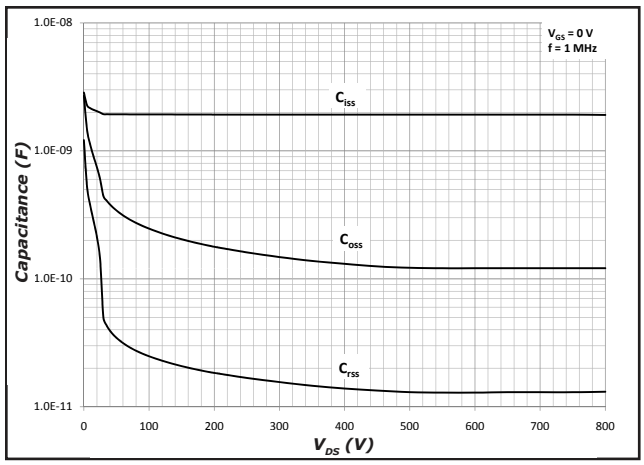


Fig 5A and 5B. Typical Capacitance vs. Drain – Source Voltage

Typical Performance

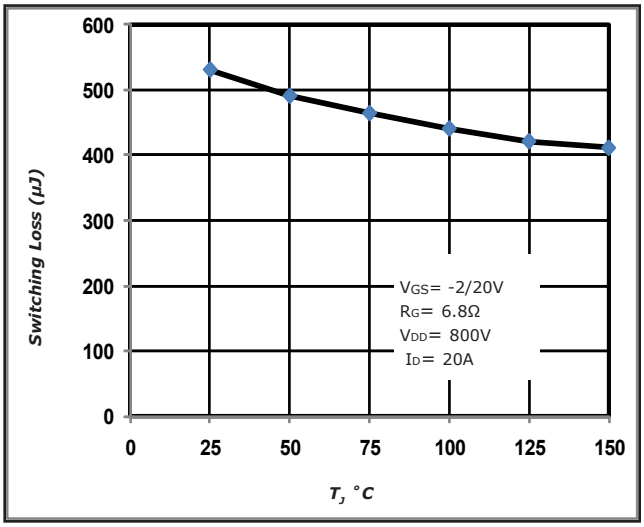


Fig 6. Inductive Switching Energy(Turn-on) vs. Temp

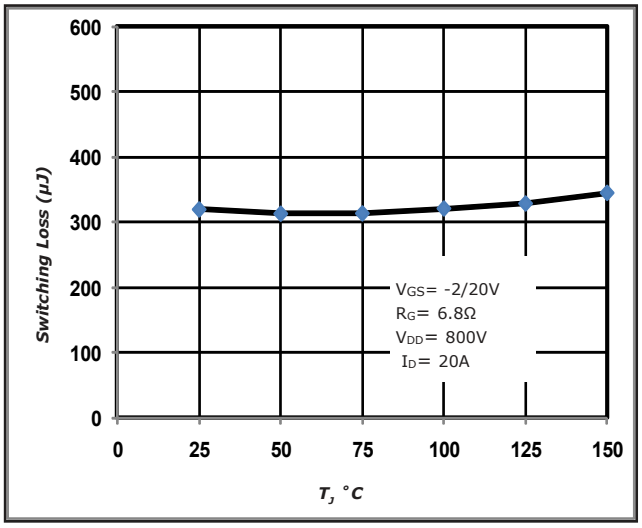


Fig 7. Inductive Switching Energy(Turn-off) vs. Temp

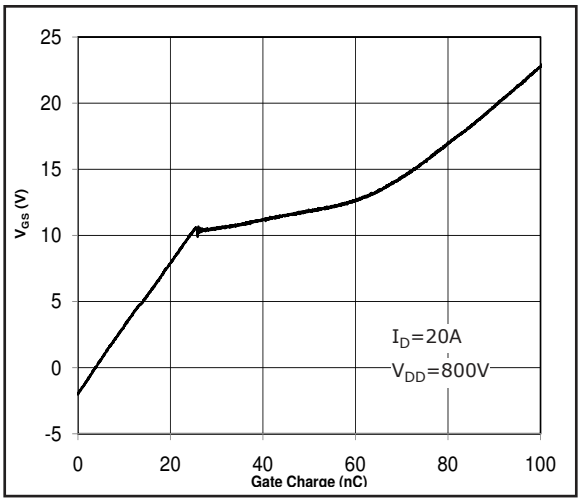


Fig 8. Typical Gate Charge Characteristics @ 25°C

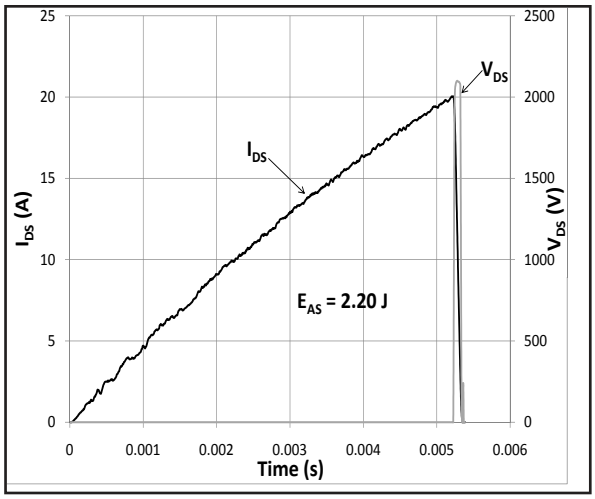


Fig 9. Typical Avalanche Waveform

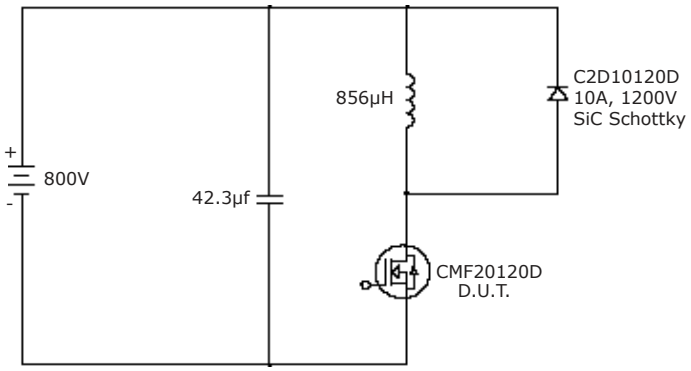


Fig 10. Switching Waveform Test Circuit

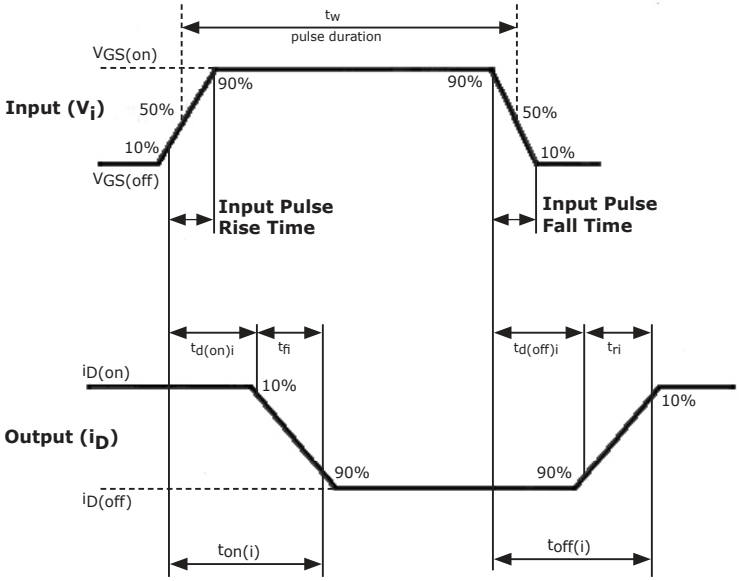


Fig 11. Switching Test Waveform Times

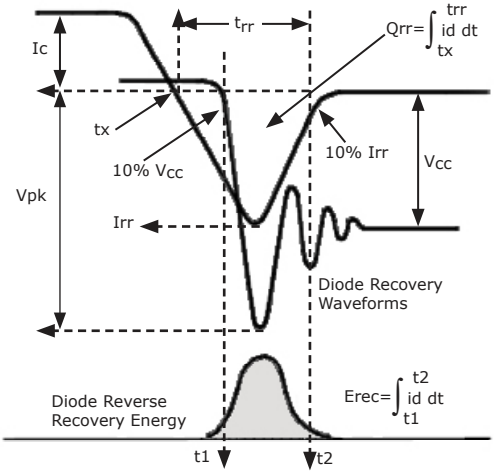


Fig 12. Body Diode Recovery Waveform

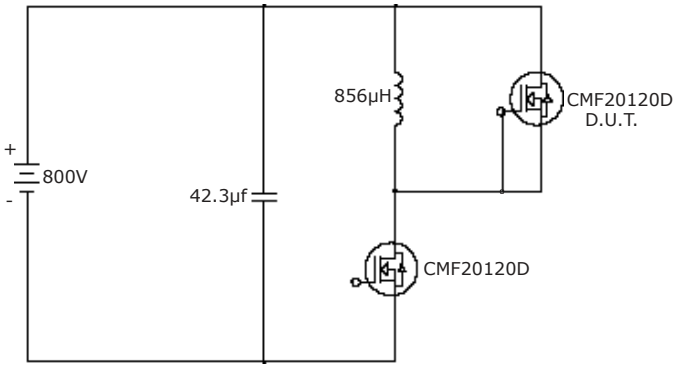


Fig 13. Body Diode Recovery Test

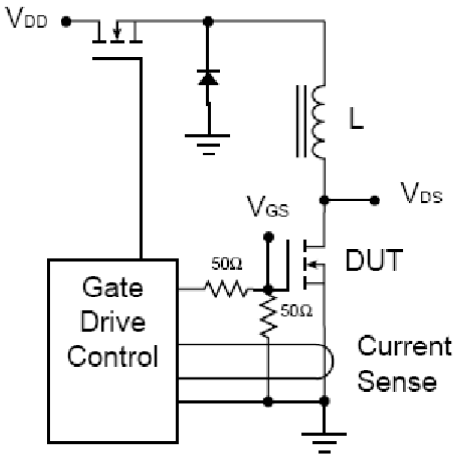
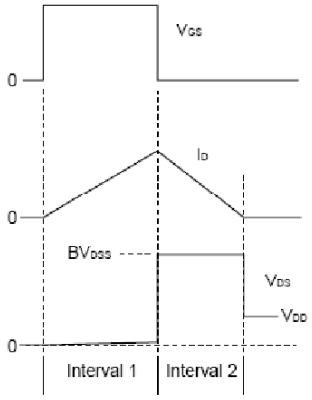


Fig 14. Avalanche Test Circuit



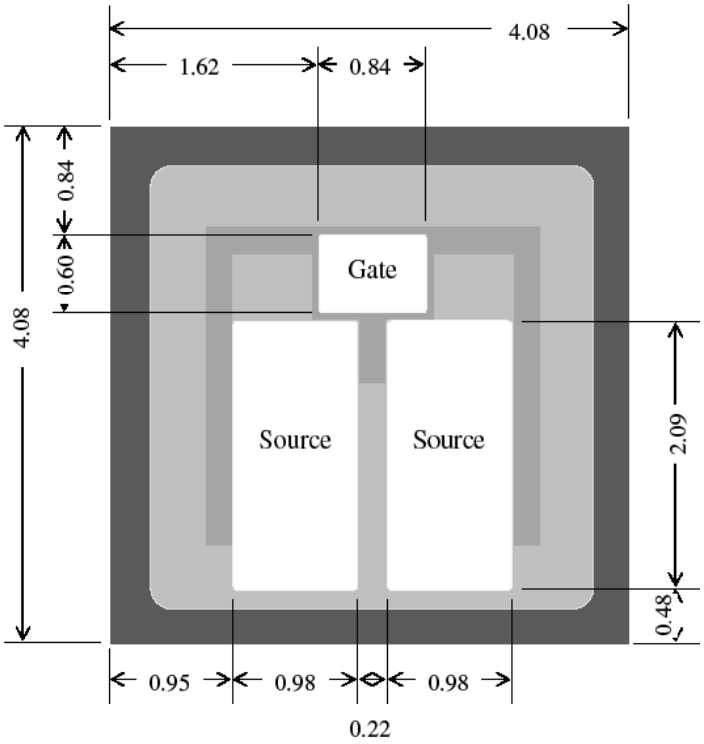
$$E_A = 1/2L \times I_D^2$$

Fig 15. Theoretical Avalanche Waveform

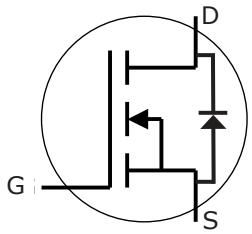
Mechanical Parameters

Parameter	Typ	Unit
Die Dimensions (L x W)	4.08 x 4.08	mm
Exposed Source Pad Metal Dimensions	0.98 x 2.09 (x 2)	mm
Gate Pad Dimensions	0.84 x 0.60	mm
Chip Thickness	365 ± 40	µm
Frontside (Source) metallization (Al)	4	µm
Frontside (Gate) metallization (Al)	4	µm
Backside (Drain) metallization (Ni/Ag)	0.8 / 0.6	µm

Chip Dimensions



Part Number	Package
CPMF-1200-S080B	DIE



* The levels of environmentally sensitive, persistent biologically toxic (PBT), persistent organic pollutants (POP), or otherwise restricted materials in this product are below the maximum concentration values (also referred to as the threshold limits) permitted for such substances, or are used in an exempted application, in accordance with EU Directive 2002/95/EC on the restriction of the use of certain hazardous substances in electrical and electronic equipment (RoHS), as amended through April 21, 2006.

* The die-on-tape method of delivering these SiC die may be considered a means of temporary storage only. Due to an increase in adhesion over time, die stored for an extended period may affix too strongly to the tape. These die should be stored in a temperature-controlled nitrogen dry box soon after receipt. Cree will further recommend that all die be removed from tape to a waffle pack, to a similar storage medium, or used in production within 2 – 3 weeks of delivery to assure 100% release of all die without issues.

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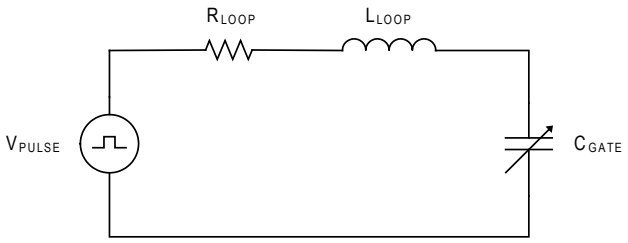
Applications Information:

The Cree SiC DMOSFET has removed the upper voltage limit of silicon MOSFETs. However, there are some differences in characteristics when compared to what is usually expected with high voltage silicon MOSFETs. These differences need to be carefully addressed to get maximum benefit from the SiC DMOSFET. In general, although the SiC DMOSFET is a superior switch compared to its silicon counterparts, it should not be considered as a direct drop-in replacement in existing applications.

There are two key characteristics that need to be kept in mind when applying the SiC DMOSFETs; modest transconductance and no turn-off tail. The modest transconductance requires that V_{GS} needs to be 20V to optimize performance. This can be seen the Output and Transfer Characteristics shown in Figures 1-3. The modest transconductance also affects the transition where the device behaves as a voltage controlled resistance to where it behaves as a voltage controlled current source as a function of V_{DS}. The result is that the transition occurs over higher values of V_{DS} than is usually experienced with Si MOSFETs and IGBTs. This might affect the operation anti-desaturation circuits, especially if the circuit takes advantage of the device entering the constant current region at low values of forward voltage.

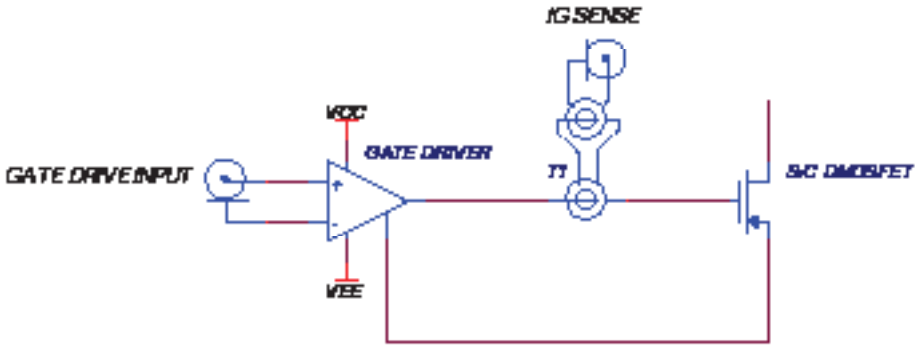
The modest transconductance needs to be carefully considered in the design of the gate drive circuit. The first obvious requirement is that the gate driver be capable of a 22V (or higher) swing. The recommended on state V_{GS} is +20V and the recommended off state V_{GS} is between 0V to -5V. Please carefully note that although the gate voltage swing is higher than typical silicon MOSFETs and IGBTs, the total gate charge of the SiC DMOSFET is considerably lower. In fact, the product of gate voltage swing and gate charge for the SiC DMOSFET is lower than comparable silicon devices. The gate voltage must have a fast dV/dt to achieve fast switching times which indicates that a very low impedance driver is necessary. Lastly, the fidelity of the gate drive pulse must be carefully controlled. The nominal threshold voltage is 2.3V and the device is not fully on ($dV_{DS}/dt \approx 0$) until the V_{GS} is above 16V. This is a noticeably wider range than what is typically experienced with silicon MOSFETs and IGBTs. The net result of this is that the SiC DMOSFET has a somewhat lower 'noise margin'. Any excessive ringing that is present on the gate drive signal could cause unintentional turn-on or partial turn-off of the device. The gate resistance should be carefully selected to insure that the gate drive pulse is adequately dampened. To first order, the gate circuit can be approximated as a



$$\zeta = \frac{R_{LOOP}}{2}\sqrt{\frac{C_{GATE}}{L_{LOOP}}} \geq 1$$

$$\therefore\ R_{LOOP} \geqslant 2\sqrt{\frac{L_{LOOP}}{C_{GATE}}}$$

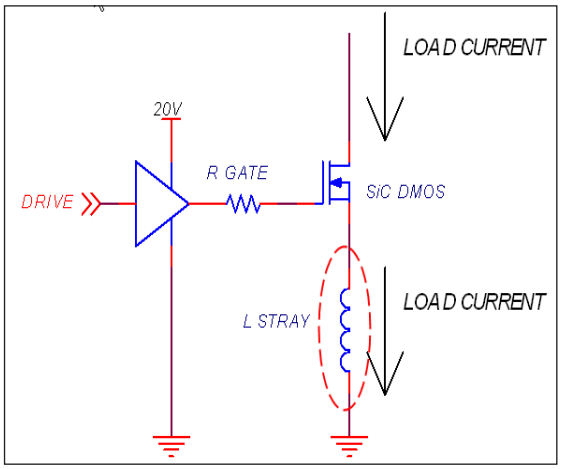
As shown, minimizing L_{LOOP} minimizes the value of R_{LOOP} needed for critical dampening. Minimizing L_{LOOP} also minimizes the rise/fall time. Therefore, it is strongly recommended that the gate drive be located as close to the SiC DMOSFET as possible to minimize L_{LOOP}. An external resistance of 6.8 Ω was used to characterize this device. Lower values of external gate resistance can be used so long as the gate pulse fidelity is maintained. In the event that no external gate resistance is used, it is suggested that the gate current be checked to indirectly verify that there is no ringing present in the gate circuit. This can be accomplished with a very small current transformer. A recommended setup is a two-stage current transformer as shown below:



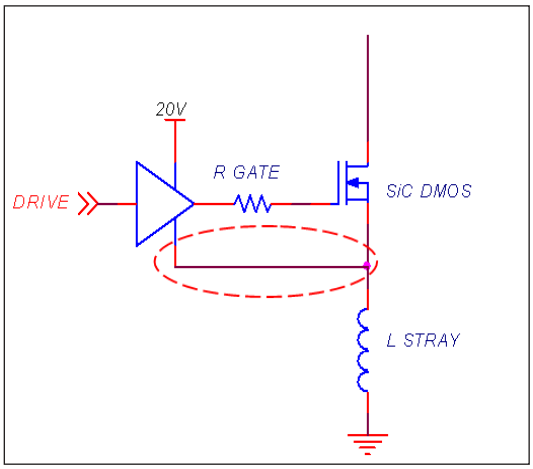
The two stage current transformer first stage consists of 10 turns of AWG 30 wire on a small high permeability core. A Ferroxcube 3E27 material is recommended. The second stage is a small wide bandwidth current transformer, such as the Tektronix CT-2. Lastly, a separate source return should be used for the gate drive as shown below:

Stray inductance on source lead causes load di/dt to be fed back into gate drive which causes the following:

- *Switch di/dt is limited*
- *Could cause oscillation*



Kelvin gate connection with separate source return is highly recommended



A significant benefit of the SiC DMOSFET is the elimination of the tail current observed in silicon IGBTs. However, it is very important to note that the current tail does provide a certain degree of parasitic dampening during turn-off. Additional ringing and overshoot is typically observed when silicon IGBTs is replaced with SiC DMOSFETs. The additional voltage overshoot can be high enough to destroy the device. Therefore, it is critical to manage the output interconnection parasitics (and snubbers) to keep the ringing and overshoot from becoming problematic.

ESD RATINGS

ESD Test	Total Devices Sampled	Resulting Classification
ESD-HBM	All Devices Passed 1000V	2 (>2000V)
ESD-MM	All Devices Passed 400V	C (>400V)
ESD-CDM	All Devices Passed 1000V	IV (>1000V)