Unipolar 2-Phase Stepper Motor Driver ICs

STA7130MC Series

Datasheet

June, 2016 Rev.4.1

This document describes the STA7130MC series, which are unipolar 2-phase stepping motor driver ICs.

This document contains preliminary information on the products under development. If you have any questions, including information on options, please contact your nearest sales or representative office.

Table of Contents

1. General Description

Thank you for your long years of patronage for each series of our unipolar 2-phase stepping motor driver ICs. **The STA7130MC series** is our latest release.

This document describes summaries of our latest products.

2. Features and Benefits

(1) Load (motor supply) voltages, V_M: 35 V (max.), 0 to 33 V normal operating range
(2) Main power supply voltages, V_{BB}: 46 V (max.), 10 to 44 V normal operating range
(3) Maximum output currents, $I_{O(max)}$: 2.0 A, 3.0 A
(4) Clock-in stepping control that allows full-, half-, quarter-, eighth-, and sixteenth-step excitation driving
(5) Built-in "sense resistor" detects motor current
(6) All variants are pin-compatible for enhanced design flexibility
(7) ZIP type 18-pin molded package (STA package)
(8) Self-excitation PWM current control with fixed OFF-time
    → OFF-time adjusted automatically by step reference current ratio (3 levels)
(9) Built-in synchronous rectifying circuit reduces power dissipation at PWM-OFF
(10) Synchronous PWM chopping function prevents motor noise in the Hold mode
(11) The Standby mode to reduce IC input current in stand-by state
(12) Built-in protection circuitry against motor coil opens/shorts and thermal shutdown protection
(13) The following functional options are available:
    ● Blanking Time
        • Standard type: 1.5 μs (typ.)
        • Optional type B: 3.0 μs (typ.)

NOTE: "Optional type B" is abbreviated and referred to as "B" as the letter used for product branding codes. This term and abbreviation are also used throughout this document. See also Section 6 for more details.

3. Part Numbers and Rated Currents

Table 3-1 provides product part numbers and rated currents available in the STA7130MC series.

Table 3-1. Part Numbers and Rated Currents

Part Number	Rated Current (Maximum Setting Value)
STA7132MC	2.0 A
STA7133MC	3.0 A

4. Specifications

Table 4-1. Absolute Maximum Ratings

Unless specifically noted, T_A = 25 °C

Characteristic	Symbol	Rating	Unit	Remarks	
Load (Motor Supply) Voltage	V_M	35	V		
Main Power Supply Voltage	V_{BB}	46	V		
Output Current	I_O	2.0	A	STA7132MC	Control current value
		3.0	A	STA7133MC	
Logic Input Voltage	V_{LI}	−0.3 to 5.5	V		
Logic Output Voltage	V_{LO}	5.5	V	FLAG, MO pins	
REF Input Voltage	V_{REF}	−0.3 to 5.5	V		
Detection Voltage	V_{RS}	±1	V		
Power Dissipation	P_D	3.5	W	Without heatsink	
Junction Temperature	T_J	150	°C		
Ambient Temperature	T_A	−20 to 80	°C		
Storage Temperature	T_{stg}	−30 to 150	°C		

NOTE: Output current ratings may be limited by duty cycles, ambient temperatures, and heat sinking conditions. Do not exceed the maximum output current and the maximum junction temperature (T_J) given above, under any conditions of use.

Table 4-2. Recommended Operating Conditions

Unless specifically noted, T_A = 25 °C

Characteristic	Symbol	Standard Value		Unit	Remarks
		Min.	Max.		
Load (Motor Supply) Voltage	V_M		33	V	
Main Power Supply Voltage	V_{BB}	10	44	V	
Logic Input Voltage	$V_{IN(Logic)}$	0	5.5	V	
REF Input Voltage	V_{REF}	0.1	0.9	V	Control current accuracy degrades at a voltage of 0.1 V or less
Case Temperature	T_C		85	°C	Measured at Pin 10 (lead portion), without heatsink

NOTE: As the motor supply voltage, V_M, becomes higher, it also approaches the breakdown voltage of the OUTx pins (75 V min.); and breakdown will be more likely to happen. Even if one of the OUTx pins breaks down (due to surge noise or other factors), the STA7130MC series will recognize it as abnormality (coil open) and will run appropriate protection functions. Therefore, a thorough evaluation is recommended.

Table 4-3. Electrical Characteristics

Unless specifically noted, T_A = 25 °C, V_{BB} = 24 V

Characteristic	Symbol	Rating			Unit	Conditions
		Min.	Typ.	Max.		
Main Power Supply Current	I_{BB}			15	mA	Normal mode
	I_{BBS}			3	mA	Standby mode
MOSFET Breakdown Voltage	V_{DSS}	75			V	I_D = 1 mA
MOSFET On-Resistance	$R_{DS(on)}$		0.18	0.24	Ω	STA7132MC
			0.12	0.18		STA7133MC
MOSFET Body Diode Forward Voltage	V_F		0.85	1.2	V	STA7132MC
			0.9	1.3		STA7133MC
Maximum Response Frequency	f_{CLK}	250			kHz	Clock duty cycle = 50%
Logic Input Voltage	V_{LIL}	0		0.7	V	
	V_{LIH}	2.3		5.5	V	
Logic Input Current	I_{LIL}		±1		μA	V_{LIL} = 0 V
	I_{LIH}		±1		μA	V_{LIH} = 5 V
Logic Output Voltage	V_{LOL}			0.5	V	I_{LOL} = 3 mA
Logic Output Current	I_{LOL}			3	mA	V_{LOL} = 0.5 V
REF Input Voltage	V_{REF}	0.1		0.9	V	
	V_{REFS}	2.0		5.5	V	Standby1[1]
REF Input Current	I_{REF}		±10		μA	V_{REF} = 0.1 to 5 V
Step Reference Current Ratio	Mode F		100		%	V_{REF} = 0.1 to 0.9 V
	Mode E		98.1			
	Mode D		95.7			
	Mode C		92.4			
	Mode B		88.2			
	Mode A		83.1			
	Mode 9		77.3			
	Mode 8		70.7			
	Mode 7		63.4			
	Mode 6		55.5			
	Mode 5		47.1			
	Mode 4		38.2			
	Mode 3		29			
	Mode 2		19.5			
	Mode 1		9.8			
SENSE Detection Voltage	V_{SENSE}	V_{REF} × 1/3 – 0.03	V_{REF} × 1/3	V_{REF} × 1/3 + 0.03	V	V_{REF} = 0.6 V, Mode F

NOTE: Unless specifically noted, negative current is defined as output current flow from a specified pin.

[1] In a state of: I_{BBS}, output OFF, and sequencer enabled.

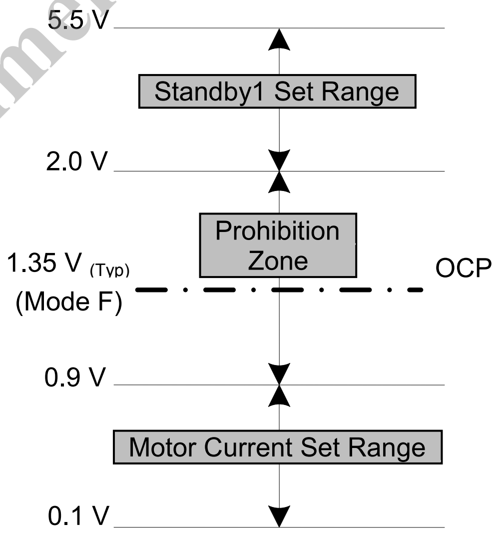
Table 4-3. Electrical Characteristics (continued)

Unless specifically noted, T_A = 25 °C, V_{BB} = 24 V

Characteristic	Symbol	Rating			Unit	Conditions
		Min.	Typ.	Max.		
Sense Resistor[1]	R_S		0.15		Ω	STA7132MC
			0.1			STA7133MC
Minimum PWM ON-Time	$t_{ON(min)}$		1.5		μs	Standard type
			3.0		μs	Optional type B
PWM OFF-Time	t_{OFF1}		12		μs	Mode 8 to Mode F
	t_{OFF2}		9		μs	Mode 4 to Mode 7
	t_{OFF3}		7		μs	Mode 1 = Mode 3
Standby-Enable Recovery Time	t_{SE}	100			μs	Standby1, Standby2
Switching Time	t_{CON}		1.6		μs	Clock → Output ON
	t_{COFF}		0.9		μs	Clock → Output OFF
Overcurrent Detection Voltage[2]	V_{SOC}		0.45		V	SENSE Terminal Voltage
Overcurrent Detection Current (V_{SOC} / R_S)	I_{OCP}		3		A	STA7132MC
			4.5		A	STA7133MC
Load Disconnection Undetected Time	t_{OPP}		2		μs	From PWM-OFF
Overheat Protection Temperature	T_{TSD}		125		°C	Measured at back of device case (after heat has saturated)

[1] Protection circuit operates when $V_{SENSE} > V_{SOC}$.

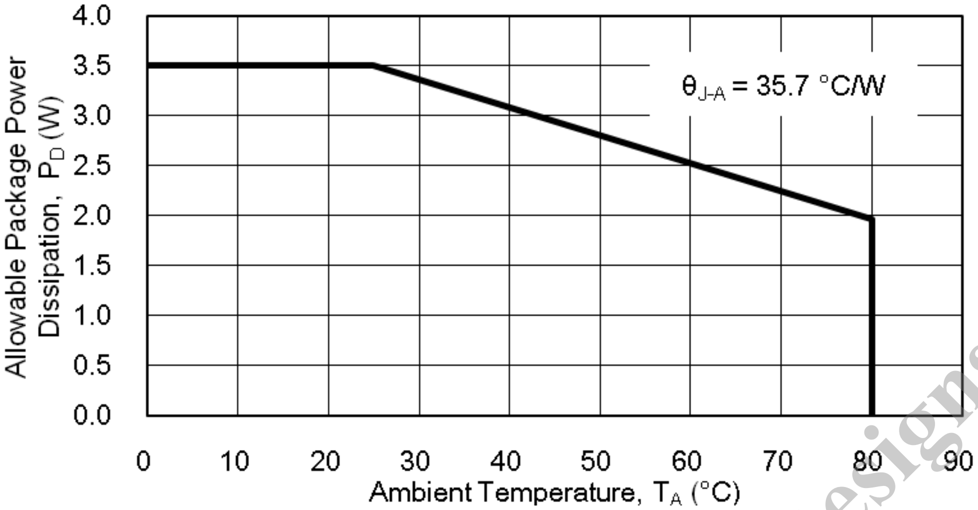
Figure 4-1. Setting Range of Reference Voltage, V_{REF}



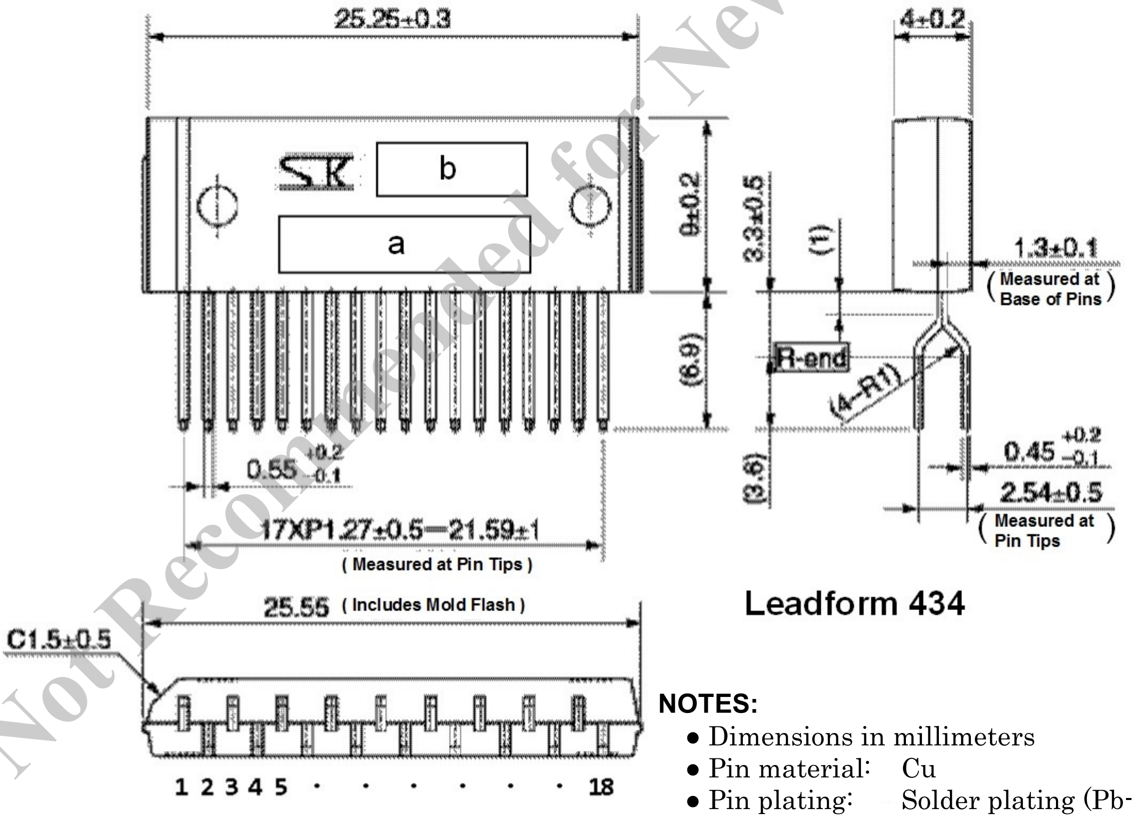
NOTE: Extra attentions should be paid to the changeover between the motor current setting range and the Standby1 set range. If the changeover takes too long, OCP operation will start when $V_{SENSE} > V_{SOC}$, depending on the step reference current ratio (Mode) selected.

5. Power Derating Chart

Figure 5-1. Power Derating Chart



6. Package Outline Drawing



Leadform 434

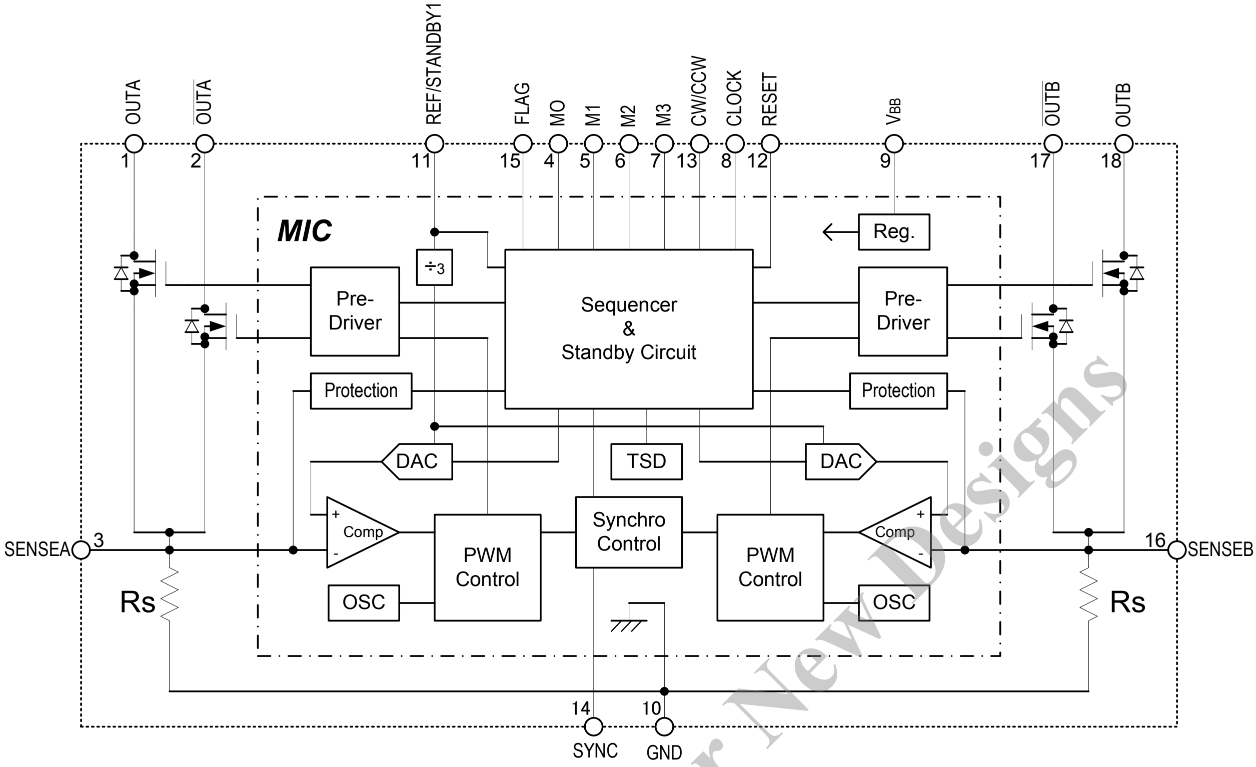
NOTES:

- Dimensions in millimeters
- Pin material: Cu
- Pin plating: Solder plating (Pb-free)

- Branding codes:
  - a Part number: *STA713xMC*
    - The lowercase letter *x* represents a number of either of *2* or *3*, according to current ratings. See also Table 3-1, which lists the part numbers and corresponding current ratings.
    - Optional type B has the suffix letter *B* at the end of its part number.
  - b Lot number: *YMDD*
    - *Y* is the last digit of the year of manufacture
    - *M* is the month of the year (1 to 9, O, N, or D)
    - *DD* is the day of the month (01 to 31)

7. Functional Block Diagram and Pin Assignment

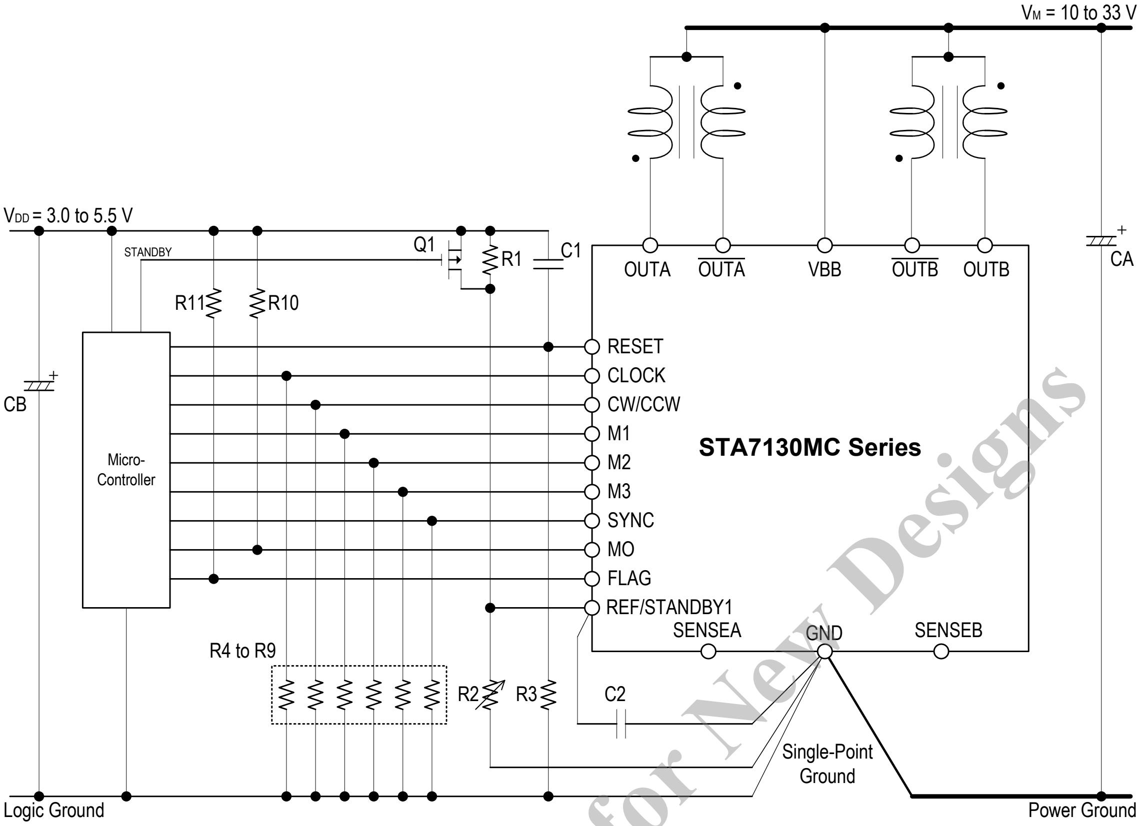
Figure 7-1. Functional Block Diagram



Pin No.	Symbol	Function
1	OUTA	Phase A output
2	$\overline{\text{OUTA}}$	Phase $\overline{\text{A}}$ output
3	SENSEA	Phase A current sensing
4	MO	Output from 2-phase excitation status monitor
5	M1	Input for excitation mode & Standby2 setting
6	M2	
7	M3	
8	CLOCK	Step clock input
9	V_{BB}	Main power supply voltage
10	GND	Ground
11	REF/STANDBY1	Input for control current / Standby1 setting
12	RESET	Reset input for internal logic
13	CW/CCW	Forward / reverse input
14	SYNC	Synchronous PMW control switch input
15	FLAG	Output from protection circuits monitor
16	SENSEB	Phase B current sensing
17	$\overline{\text{OUTB}}$	Phase $\overline{\text{B}}$ output
18	OUTB	Phase B output

8. Application Example

Figure 8-1. Application Example



Constants, for reference use only:

R1 = 10 kΩ
R2 = 1 kΩ (VR)
R3 = 10 kΩ
R4 to R9 = 1 to 10 kΩ (Not required if input state does not reach indefinite.)
R10 to R11 = 5.1 to 10 kΩ

NOTES:

- Take precautions to avoid noise on the V_{DD} line; noise levels greater than 0.5 V on the V_{DD} line may cause device malfunction. Noise can be reduced by separating the logic ground and the power ground on a PCB from the GND pin (Pin 10).
- Unused logic input pins (CW/CCW, M1, M2, M3, RESET, and SYNC) **must be pulled up or down to VDD or ground**. If those unused pins are left open, the device may malfunction.
- Unused logic output pins (MO, FLAG) **must be kept open**.

9. Truth Tables

(1) Input Pins

Table 9-1. Truth Table for Common Input Pins

Pin Name	Low Level	High Level	Clock
RESET	Normal operation	Logic reset	—
CW/CCW	Forward (CW)	Reverse (CCW)	↑
M1	Excitation mode setting & Standby2 (Protection Release)1)		
M2			
M3			
REF/STANDBY1	Enable	Standby1	—
SYNC	Non-sync PWM control	Sync PWM control	—

1) See Table 9-2 below.

Voltage across the REF/STANDBY1 pin controls PWM currents and the Standby1 function. The threshold voltage of this pin is set to approximately 1.75 V.

- When $V_{REF} \leq 1.5$ V (low level), the REF/STANDBY1 pin functions as the reference voltage input for normal operation.
- When $V_{REF} \geq 2.0$ V (high level), the REF/STANDBY1 pin disables all outputs and then puts the IC into the Standby1 mode. This Standby1 mode disables internal linear circuitry and minimizes the main power supply current, I_{BB}. Although much of the internal circuitry is disabled, the logic circuit is still active. If an input signal on the CLOCK pin is asserted, the internal sequencer/translator circuit reacts and sets a step starting point for the next operation.

The Reset function is asynchronous. If an input on the RESET pin is high, the internal logic circuit is reset. Note that a signal on the RESET pin cannot control an output disable command. If not the Standby state, outputs turn on at the starting point of excitation.

The Sync function runs only at “2-phase excitation timing." (2-phase excitation timing is a point where the step reference current ratio of both phases A and B is either of Mode 8 or F.) If this function is used at other than the 2-phase excitation timing, an overall balance might collapse because PWM OFF-times and setting currents are different in each of phase A and phase B control scenario. (If this function is used at a point of 1-phase excitation, it does not react as the Sync function does. But there is no problem.)

Table 9-2. Commutation & Standby2 Truth Table for Common Input Pins

Excitation Mode	Pin Name			Remarks
	M1	M2	M3	
Full step (2 Phase)	L	L	L	Mode 8 fixed
	H	L	L	Mode F fixed
Half step (1-2 Phase)	L	H	L	Mode 8, and F
	H	H	L	Mode F fixed
Quarter step (W1-2 Phase)	L	L	H	Mode 4, 8, C, and F
Eighth step (2W1-2 Phase)	H	L	H	Mode 2, 4, 6, 8, A, C, E, and F
Sixteenth step (4W1-2 Phase)	L	H	H	Mode 1 to F
Standby2	H	H	H	Output Disable & Protection Release

The Standby2 function operates in the same way as the Standby1 function does, except that the internal logic circuit enters the Hold mode. Therefore, in the Standby2 mode, the internal sequencer/translator circuit is not activated even if a step command signal occurs on the CLOCK input pin.

The Standby2 function can release the state in which the Protection function is active (i.e., Protection Release).

(2) Output Pins

Table 9-3. Truth Table for Monitor Output Pins

Pin Name	Low Level	High Level (Hi-Z)
MO	Other than 2-phase excitation timing	2-phase excitation timing
FLAG	Normal operation	Protection circuit operation

"2-phase excitation timing" is a point where the step reference current ratio of both phases A and B is either of Mode 8 or F.

Each monitor output pin is **an open-drain type** configuration. When using these pins, add a pull-up resistor of approximately 5.1 to 10 kΩ.

The outputs turn off when the protection circuit starts operating. To release the protection state, re-input the main power supply voltage (V_{BB}) or put the IC into the Standby2 mode.

10. Logic Input Pins

The low pass filter (LPF) incorporated with the logic input pins (CLOCK, RESET, CW/CCW, M1, M2, M3, and SYNC) improves noise rejection.

The logic inputs are MOS input compatible; therefore, they are in a high impedance state. **Note that the IC should be used at a fixed input level, either low or high.**

If there is a possibility that signals from the microcontroller are in high impedance, add a pull-up/-down resistor. Since outputs from the logic input pins, which function as output ON/OFF controllers, may result in abnormal oscillation, leading to MOSFET breakdown as the worst-case scenario.

11. Logic Input Timing

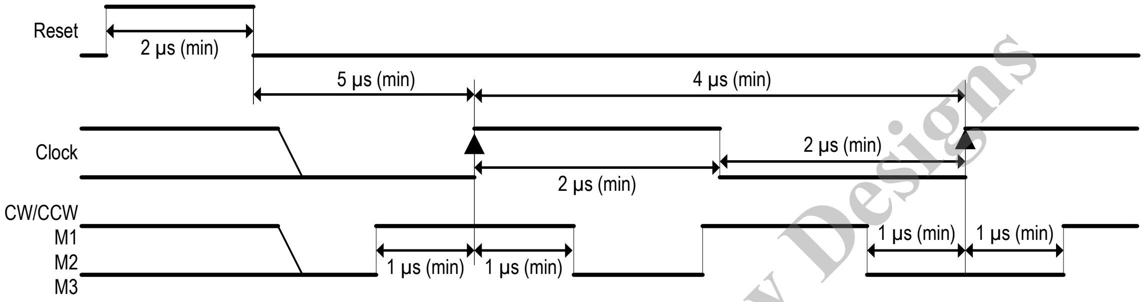
(1) Clock Signal

a. A low-to-high transition on the CLOCK input signal advances the sequencer/translator. Clock pulse width should be set at 2 μs or longer in both positive and negative polarities. Therefore, clock response frequency is set to 250 kHz.

b. Clock Edge Timing

With regard to the input logic of the CW/CCW, M1, M2, and M3 pins, a 1 μs delay should occur both before and after a pulse edge, as setup and hold times (see Figure 11-1). The sequencer logic circuitry might malfunction if the logic polarity is changed during these setup and hold times.

Figure 11-1. Input Signal Timing



NOTE: When awaking from the Standby1 or Standby2 mode, a delay of *100 μs or longer* before sending a clock pulse is recommended.

(2) Reset Signal

a. Reset Signal Pulse Width

Reset pulse width is equivalent to the hold time of a high level input. It should be 2 μs or longer, same as the clock pulse width.

b. Reset Release and Clock Input Timing

When the timing of a reset release (falling edge) and a clock edge is simultaneous, the internal logic might result in an unexpected operation. Therefore, a greater than 5 μs delay is required between the falling edge of the RESET input signal and the next rising edge of the CLOCK input signal (see Figure 11-1).

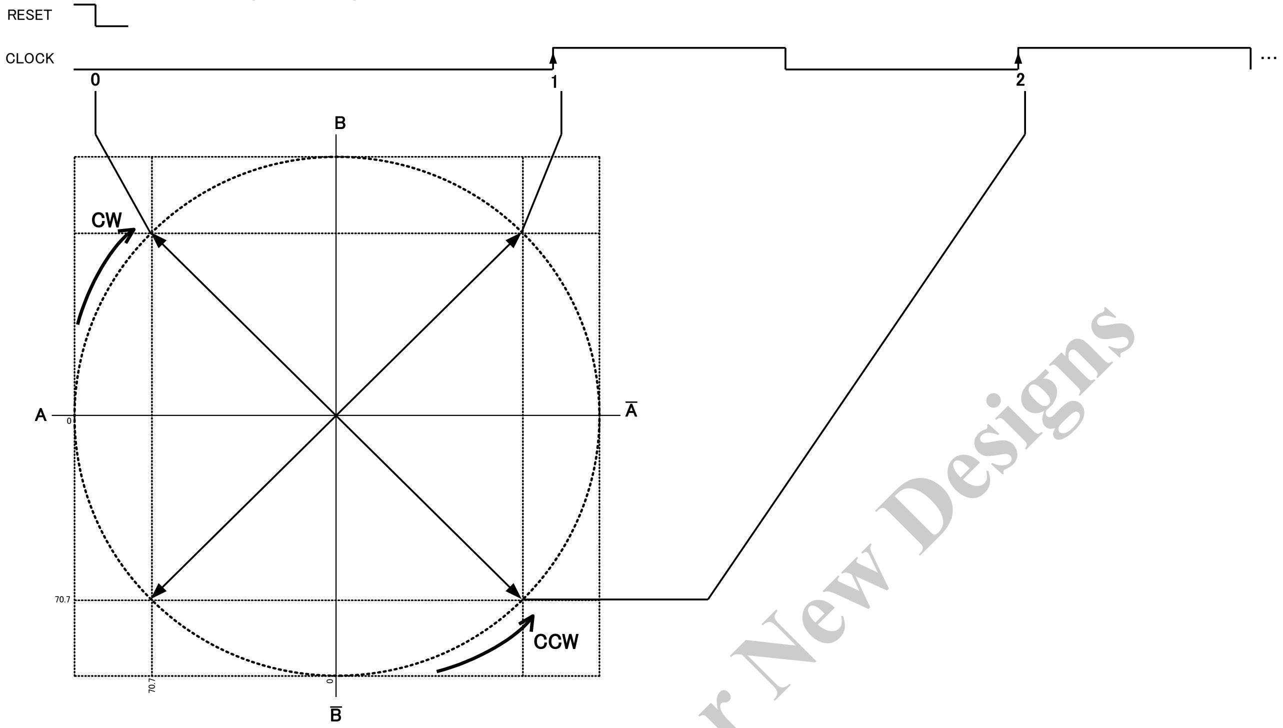
(3) Logic Level Change

Logic level inputs on CW/CCW, M1, M2, and M3 set the translator step direction (CW/CCW) and step mode (M1, M2, and M3; see also Table 9-2, the commutation truth table). Changes to those inputs do not take effect until the rising edge of an input signal on the CLOCK pin. However, depending on the type and state of a motor, there may be errors in motor operation such as step-out. A thorough evaluation on the changes of sequence should be carried out.

12. Step Sequence Diagrams

Figure 12-1. Full Step (2 Phase Excitation)

M1: L, M2: L, M3: L (Mode 8)



M1: H, M2: L, M3: L (Mode F)

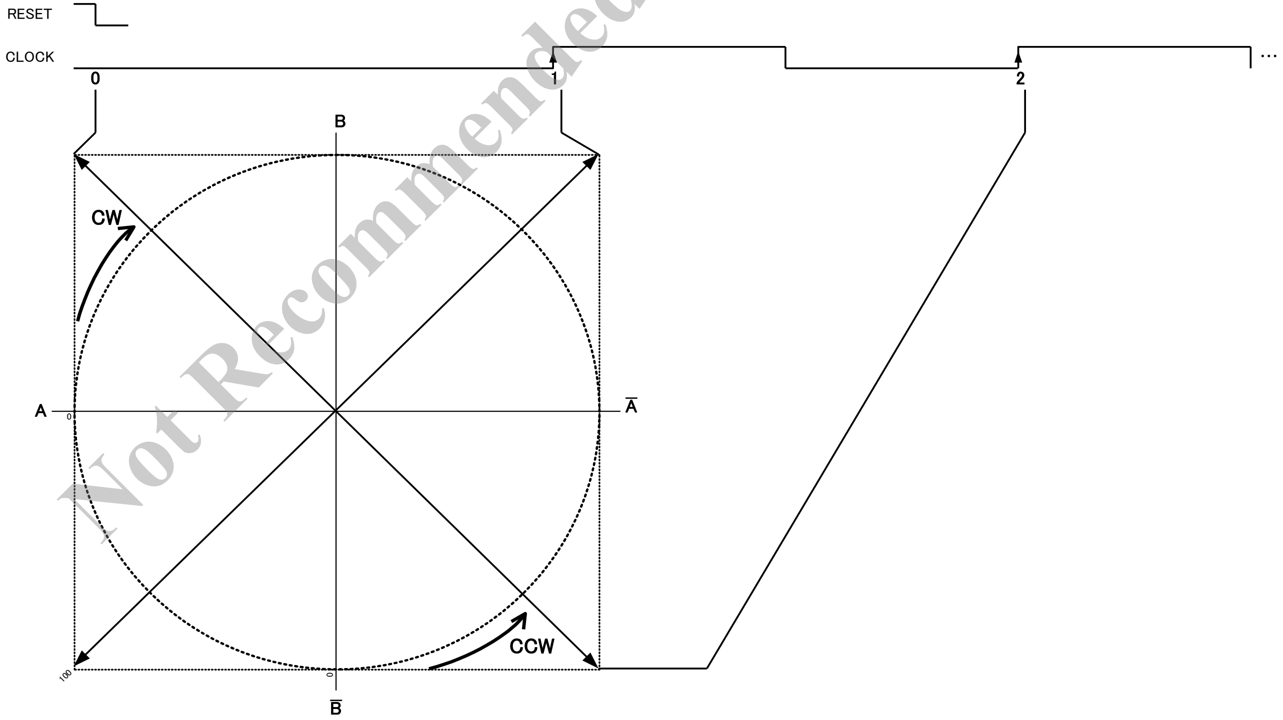
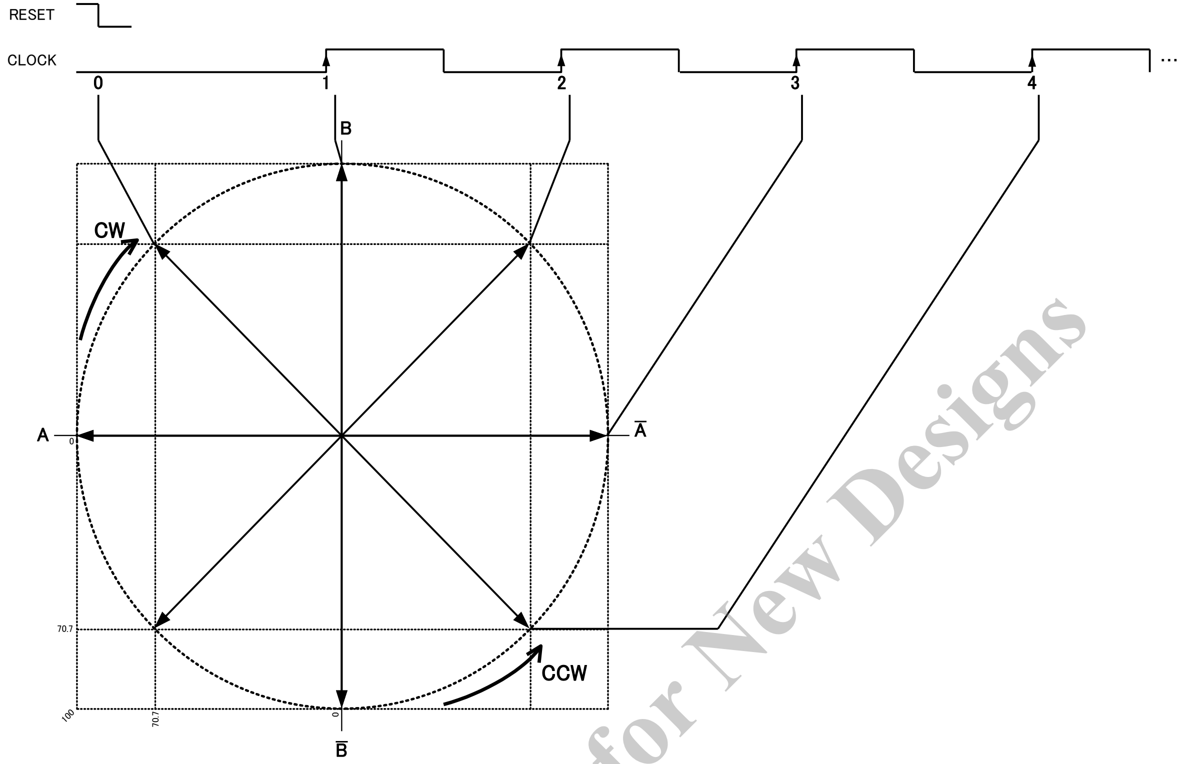


Figure 12-2. Half Step (1-2 Phase Excitation)

M1: L, M2: H, M3: L (1 Phase: Mode F / 2 Phase: Mode 8)



M1: H, M2: H, M3: L (Mode F)

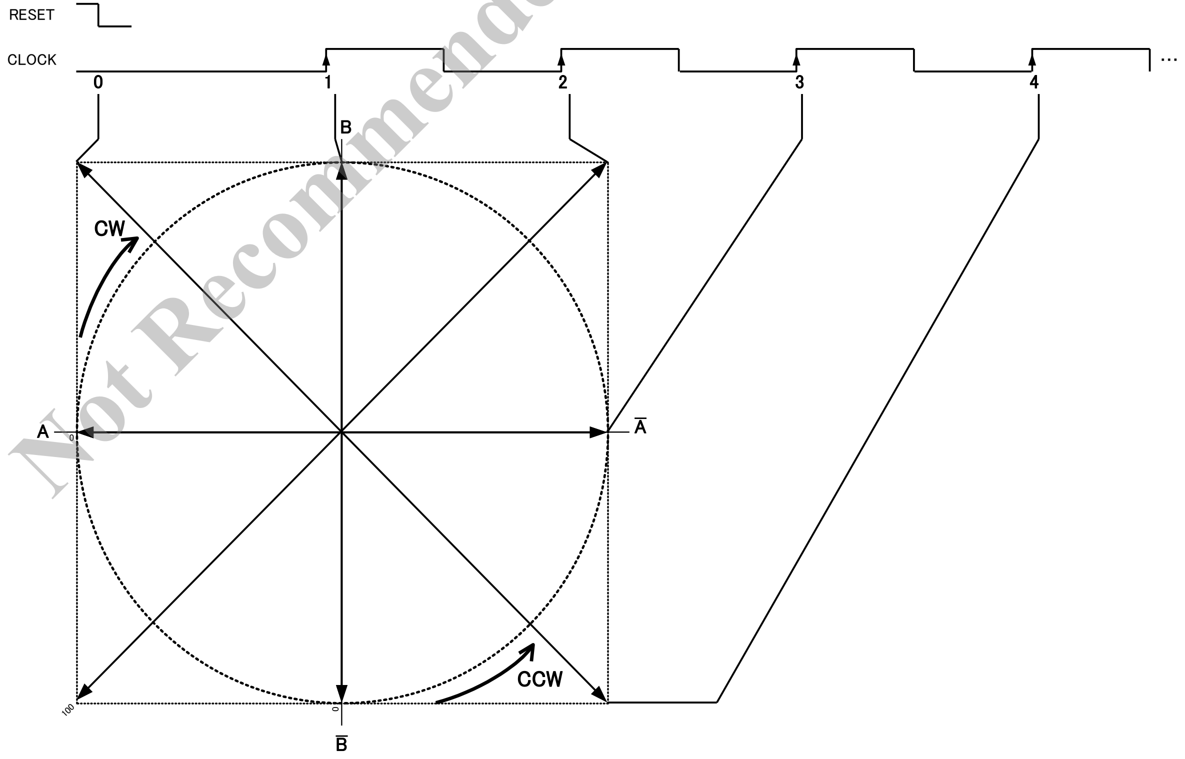


Figure 12-3. Quarter Step (W1-2 Phase Excitation)

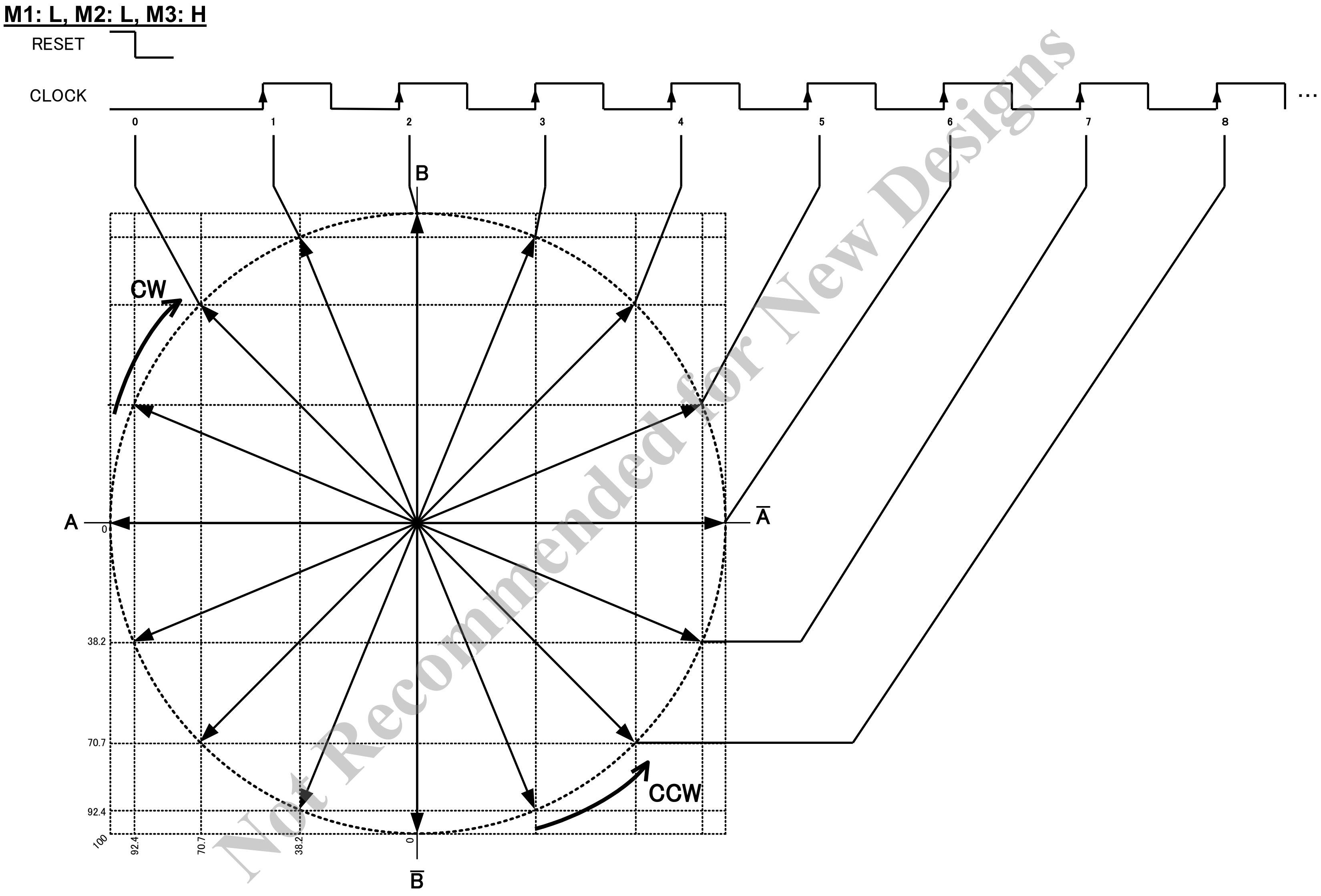


Figure 12-4. Eighth Step (2W1-2 Phase Excitation)

M1: H, M2: L, M3: H

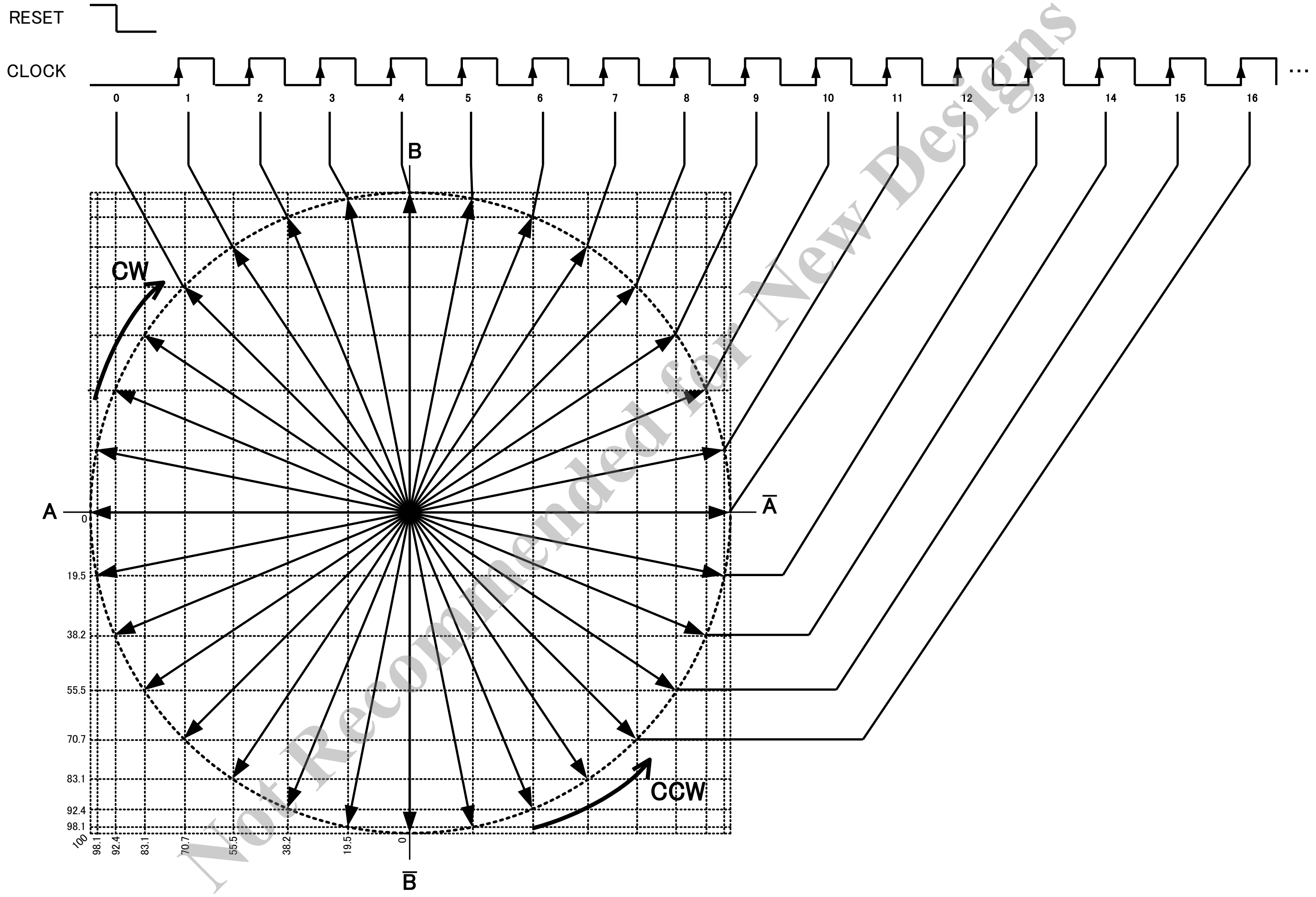
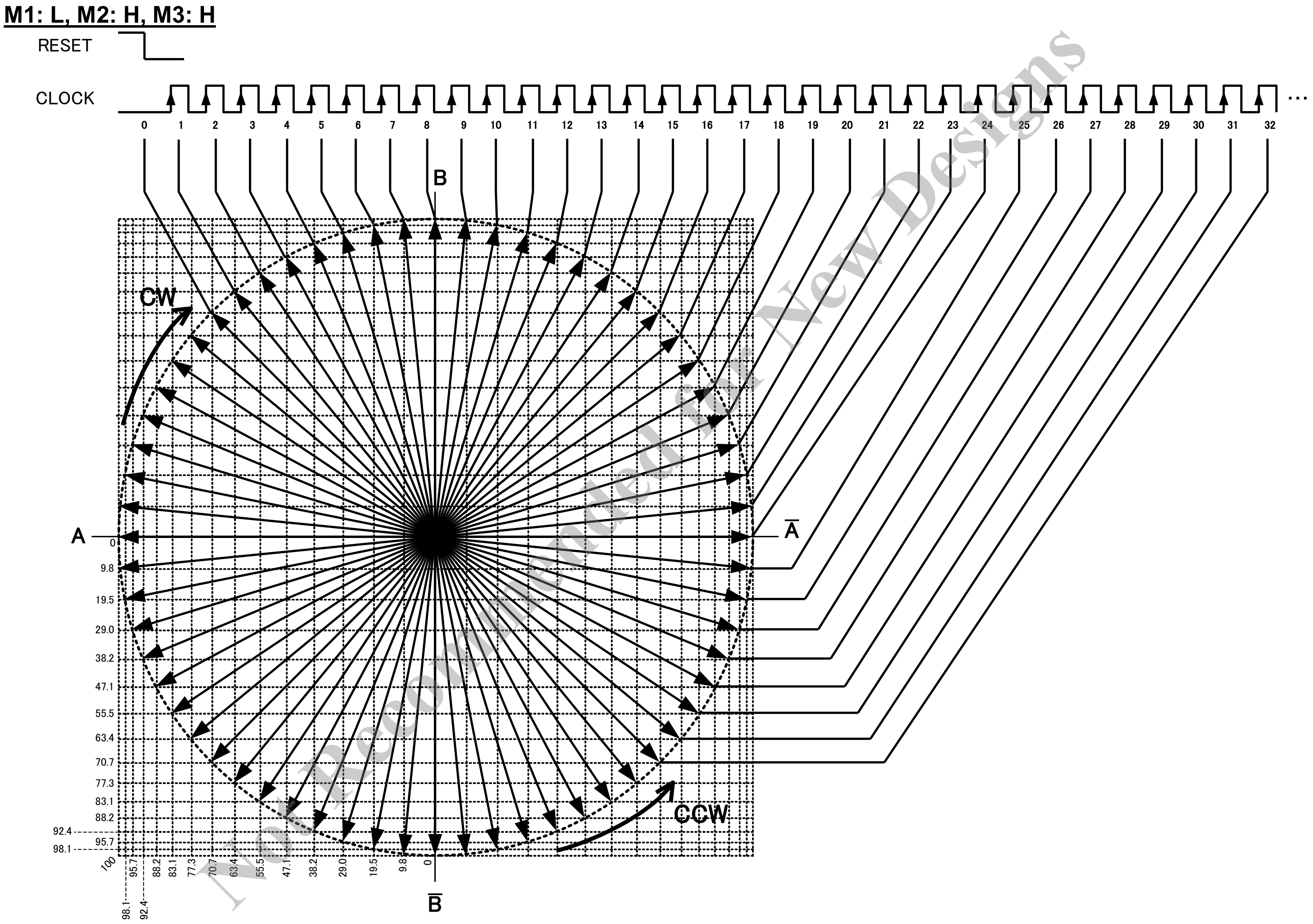


Figure 12-5. Sixteenth Step (4W1-2 Phase Excitation)



Excitation Change Sequence

The change of excitation modes is determined by the settings of the excitation pins (M1, M2, and M3) before and after a step signal. Table 12-1 shows each excitation mode state setting.

Table 12-1. Excitation Mode States

Direction	Internal Sequence State[1]				Step Sequencing[2]						
	Phase A		Phase B		2 Phase (Full Step)		1-2 Phase (Half Step)		W1-2 Phase (1/4 Step)	2W1-2 Phase (1/8 Step)	4W1-2 Phase (1/16 Step
	PWM	Mode	PWM	Mode	Mode 8	Mode F	Mode 8/F	Mode F			
CCW ↕ CW	A	8	B	8	X	**XX**	X	**XX**	X	X	X
	A	7	B	9							X
	A	6	B	A						X	X
	A	5	B	B							X
	A	4	B	C					X	X	X
	A	3	B	D							X
	A	2	B	E						X	X
	A	1	B	F							X
	-	-	B	F			X	X	X	X	X
	/A	1	B	F							X
	/A	2	B	E						X	X
	/A	3	B	D							X
	/A	4	B	C					X	X	X
	/A	5	B	B							X
	/A	6	B	A						X	X
	/A	7	B	9							X
	/A	8	B	8	X	**XX**	X	**XX**	X	X	X
	/A	9	B	7							X
	/A	A	B	6						X	X
	/A	B	B	5							X
	/A	C	B	4					X	X	X
	/A	D	B	3							X
	/A	E	B	2						X	X
	/A	F	B	1							X
	/A	F	-	-			X	X	X	X	X
	/A	F	/B	1							X
	/A	E	/B	2						X	X
	/A	D	/B	3							X
	/A	C	/B	4					X	X	X
	/A	B	/B	5							X
	/A	A	/B	6						X	X
	/A	9	/B	7							X
	/A	8	/B	8	X	**XX**	X	**XX**	X	X	X
	/A	7	/B	9							X
	/A	6	/B	A						X	X
	/A	5	/B	B							X
	/A	4	/B	C					X	X	X
	/A	3	/B	D							X
	/A	2	/B	E						X	X
	/A	1	/B	F							X
	-	-	/B	F			X	X	X	X	X
	A	1	/B	F							X
	A	2	/B	E						X	X
	A	3	/B	D							X
	A	4	/B	C					X	X	X
	A	5	/B	B							X
	A	6	/B	A						X	X
	A	7	/B	9							X
	A	8	/B	8	X	**XX**	X	**XX**	X	X	X
	A	9	/B	7							X
	A	A	/B	6						X	X
	A	B	/B	5							X
	A	C	/B	4					X	X	X
	A	D	/B	3							X
	A	E	/B	2						X	X
	A	F	/B	1							X
	A	F	-	-			X	X	X	X	X
	A	F	B	1							X
	A	E	B	2						X	X
	A	D	B	3							X
	A	C	B	4					X	X	X
	A	B	B	5							X
	A	A	B	6						X	X
	A	9	B	7							X

[1] Each mode is defined accordingly to the SLA7070MPRT series.

[2] **XX** indicates that sequence state is Mode 8; but step reference current ratio is Mode F. Mode F has a step reference current ratio of 100%, and a PWM OFF-time of 12 µs.

13. Individual Circuit Descriptions

(1) Monolithic IC (MIC)

- Sequencer Logic

  A single clock strategy is employed for step timing. An input on the CW/CCW pin determines the direction of motor rotation. Excitation mode is controlled by the combination of the M1, M2, and M3 input logic levels. See Section 9 for truth tables, and Section 11 for input timings.

- DAC (D-to-A Converter)

  DACs that generate the reference voltage for controlling current. In microstep sequencing, the current at each step is set by the values of a sense resistor (R_S), a reference voltage (V_{REF}), the output voltage of the DACs, controlled by the output of the sequencer/translator circuit.

  Internal Reference Voltage = Reference Voltage / 3 × Step Reference Current Ratio

  For the step reference current ratios, see the electrical characteristics tables given in Section 4.

- PWM Control

  Circuits that allow self-excitation PWM current controlling with a fixed OFF-time are used in this series. Each built-in oscillator (OSC) determines an OFF-time and a blanking time for proper PWM operation. The operation mechanism of the PWM control circuitry is identical to that of the STA7130M family. For more detailed functional descriptions, see Section 14.

- Synchronous Control

  A synchronous chopping circuit that prevents occasional motor noise during a hold state which normally results from the asynchronous PWM operation of both motor phases. When the SYNC input pin is set to logic high, the circuit sends a timing signal that simultaneously turns off the chopping of phases A and B.

  This function adopts the same operation mechanism applied to the STA7130M series. Therefore, the use of the synchronous control during normal stepping is not recommended, because it produces less motor torque or may cause motor vibration due to staircase current.

  The use of the synchronous control when the motor is not in operation is only allowed in 2-phase excitation timing, because the differences in current control values and PWM OFF-times between phases A and B exist at other excitation timings; otherwise, these two phases may not be synchronized or may be greatly disrupted in their current control values.

- Regulator Circuit

  An integrated regulator circuit is used for powering the output MOSFET gate drive circuit (pre-driver) and other internal linear circuits.

- Protection Circuit

  Built-in protection circuits against motor coil opens or shorts are provided. This protection is activated by sensing the voltage across internal sense resistors, R_S. Therefore, an overcurrent condition cannot be detected which results from the OUTx pins or SENSEx pins, or both, shorting to GND. The protection against motor coil opens is available only during PWM operation; therefore, it does not work at constant voltage driving, when the motor is rotating at a high speed.

  The operation of the protection circuit disables all outputs and reduces the circuit current to approximately one-third. To return from the Protection mode, perform the following steps:

  1) Cycle the main power supply, V_{BB}.
  2) Release the protection state by setting logic input pins (M1, M2, and M3) high to change into the Standby2 mode.

- TSD Circuit

  A TSD circuit that protects a driver by shifting an output to the Disable mode is incorporated. When the temperature of the product control IC (MIC) rises and becomes higher than its threshold, the circuit starts operating.

  To reset the function, perform the same steps as described in the Protection Circuit description.

(2) Output MOSFET Chip

The type of MOSFET chips to be mounted varies according to which of the two different output current ratings has been selected. For specifications, see Table 4-3.

(3) Sense Resistor

Sense resistors are incorporated in this series to detect motor current. The resistance of these varies according to which of the two different output current ratings has been selected. For specifications, see Table 4-3.

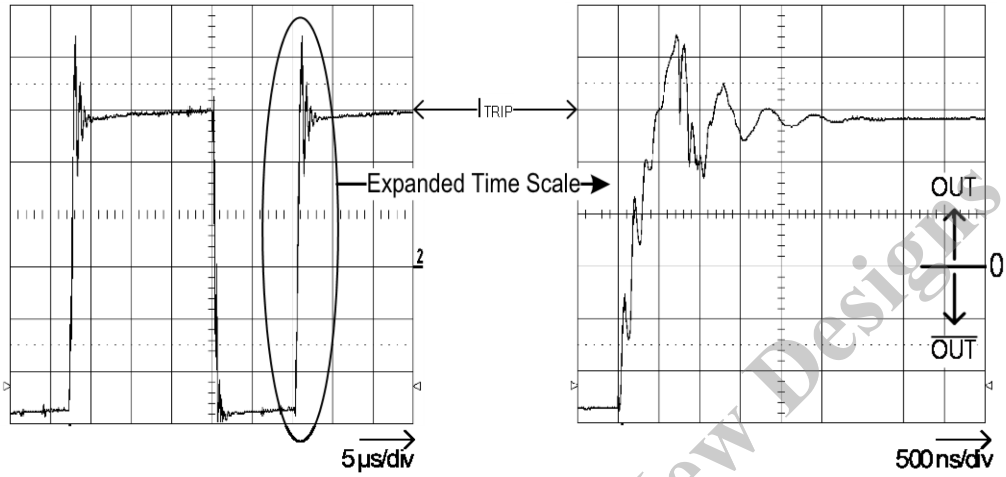
14. Functional Descriptions

(1) PWM Current Control

[1] Blanking Time

An actual operating waveform on the SENSEx pin when driving a motor is shown in Figure 14-1.

Figure 14-1. Operating Waveform on SENSEx Pin during PWM Chopping
(Circled area of the left panel is shown in expanded scale in the right panel)

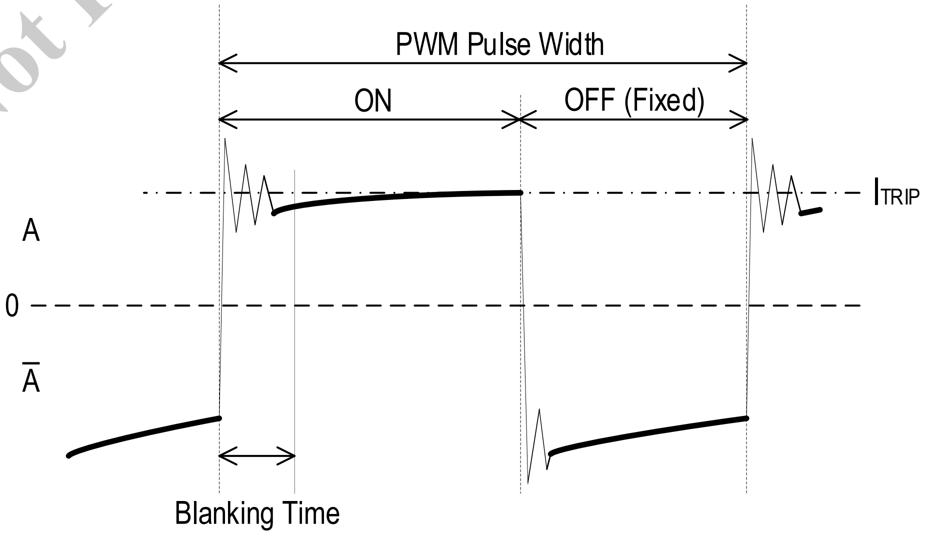


Immediately after a PWM turns off, ringing (or spike) noise on the SENSEx pin is observed for a period of a few microseconds. Ringing noise can be generated by various causes, such as capacitance between motor coils or inappropriate motor wiring.

Each pair of outputs is controlled by a fixed OFF-time PWM current-control circuit that limits the load current to a target value, I_{TRIP}. Initially, an output is enabled and then currents flow through the motor winding and the current sense resistors. When the voltage across the current sense resistors equals the DAC output voltage, V_{TRIP}, the current sense comparator resets a PWM latch. This turns off the driver for the fixed OFF-time, during which the load inductance causes the current to recirculate for the OFF-time period. Therefore, if the ringing noise on the sense resistor(s) equals and surpasses V_{TRIP}, the PWM turns off (i.e., a hunting phenomenon).

To prevent this phenomenon, a blanking time is set to override signals from the current sense comparator for a certain period immediately after the PWM turns on (Figure 14-2).

Figure 14-2. SENSEx Pin Waveform Pattern during PMW Control

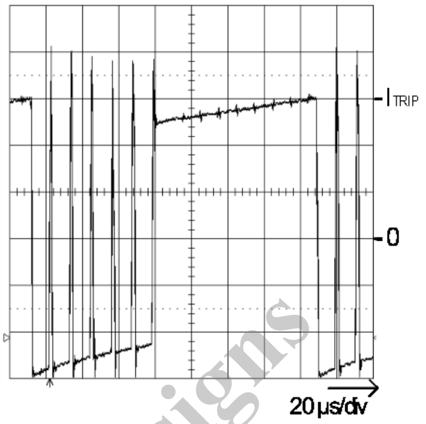


[2] Blanking Time and Hunting Phenomenon

Although current control can be improved by shortening a blanking time, the degree of margin to a ringing noise decreases simultaneously. For this reason, when a motor is driven by the device, a hunting phenomenon may occur. Figure 14-3 shows an example of the waveform pattern when the phenomenon occurs.

In order to overcome this problem, Sanken has released a new option, "type B", which offers a longer blanking time. Having the longer banking time, the optional type B can improve problems such as torque reduction and huge motor noise that are occasionally found during the hunting phenomenon.

Figure 14-3. Example of SENSEx Pin Waveform during Hunting Phenomenon



[3] Blanking Time Difference

Table 14-1 shows characteristic differences between two blanking times, shorter and longer blanking periods.

This comparison is based on the case where drive conditions, such as a motor, motor power supply voltage, REF input voltage, and circuit constant were kept the same while only the indicated parameters were changed.

Table 14-1. Characteristic Comparison of Difference in Blanking Time

Parameter	Better Performance	
Internal blanking time	Short	Long
Minimum PWM ON-time	Small ←	
Ringing noise suppression	→	Large
Minimum coil current	Small ←	
Coil current waveform distortion at a high rotation (mainly microstep)	→	Large

Brief descriptions for each parameter are as follows:

- Minimum PWM ON-time, $t_{ON(min)}$

  This series has a blanking time that is effectively selected and fixed by the PWM control. Therefore, even if an application attempts to shorten its ON-time for limiting currents, it would not go below the fixed blanking time. Minimum PWM ON-time refers to the time when an output is on during this blanking time period, that is, when an output MOSFET is actually turned on. In other words, a blanking time determines a minimum ON-time ("Small" in Table 14-1).

- Minimum Coil Current

  This refers to the coil current when the PWM control is performed during a minimum PWM ON-time. In other words, the device with a shorter blanking time can reduce more coil current.

- Coil Current Waveform Distortion during High-Velocity Revolution

  While a microstep drive is active, the I_{TRIP} value changes to a predetermined value in accordance with a clock input. The I_{TRIP} value (internal reference voltage splitting ratio) is then set up to be a sine wave. Because the PWM control of motor coil current is set according to the I_{TRIP} value, (the envelope of) the motor coil current will also be controlled to be sine wave-like.

In fact, due to the inductance characteristic of the coil, the device requires some time to bring the coil current completely to a targeted value (I_{TRIP}).

Roughly, the relationship between the convergence time (t_{conv}), a time until the coil current settles to its I_{TRIP} value, and the duty cycle (t_{clk}) of an input clock pulse in any mode is

$$t_{CONV} < t_{clk} ,$$

where the coil current waveform amplitude serves as the limit for I_{TRIP}.

When the current attempts to increase, the full limit of t_{conv} is determined by power supply voltage and the time constant of the motor coil used. While the current attempts to decrease, the full limit is determined by the power supply voltage, the damping time constant of the motor coil used, and the minimum ON-time.

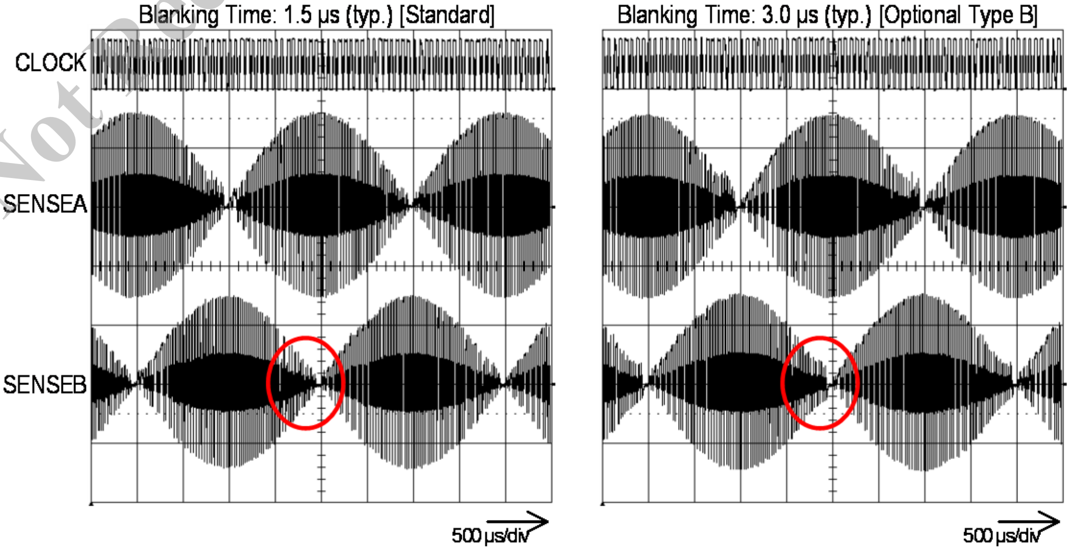
The duty cycle (t_{clk}) is determined by the frequency of an input clock. It becomes smaller as the frequency of the input clock increases. When the frequency of the input clock is raised, because t_{clk} becomes small, it is normal that the coil current cannot be raised to the I_{TRIP} value within a single clock period. In this situation, the waveform amplitude of the coil current degenerates from the sine wave, referred to as "waveform distortion."

Figure 14-4 illustrates the comparison result of waveform distortions. Devices with different blanking times were compared under the operating conditions that power supply voltages, current preset values, motors, and so forth were kept the same.

As shown in the areas circled (blanking times) in the figure below, the amplitude envelope of the SENSEx pin waveform in the 1.5 µs case, which is the same as the current waveform, has become sine wave-like whereas the waveform in the 3.0 µs blanking time case has degenerated from an ideal sine wave.

The meaning of the team "Large" in Table 14-1 is as follows: if making a comparison under the same operating conditions, the device with a longer blanking time will result in less waveform distortion due to a lower clock frequency. But if the clock frequency is the same, waveform distortion will be larger due to a shorter blanking time. Even if such distortion is observed, it does not always mean that the motor characteristics will be negatively affected. Therefore, thorough evaluations should be carried out to make an informed decision.

Figure 14-4. Comparison of SENSEx Pin Waveforms during High-Speed Revolution



[4] PWM OFF-time

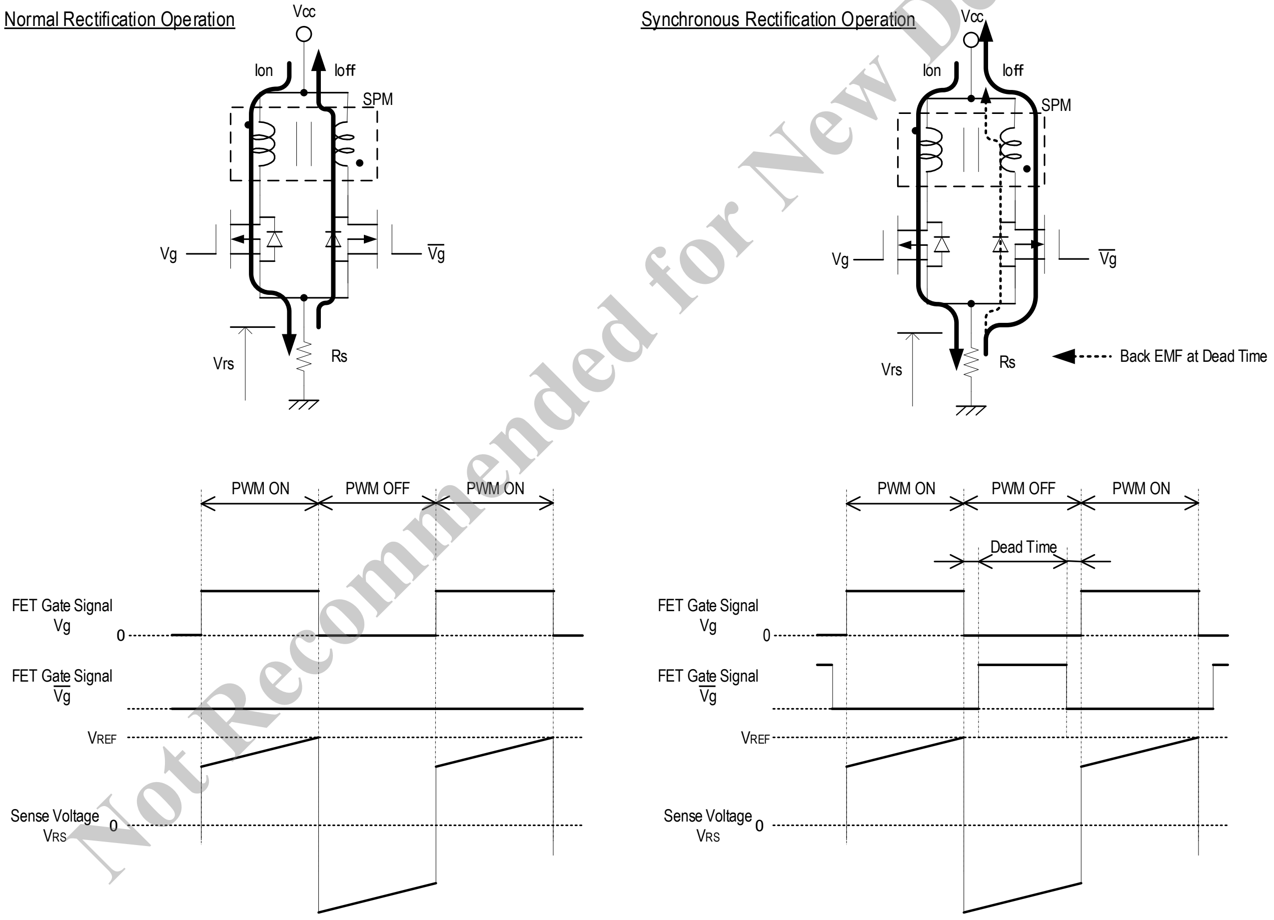
PWM OFF-time for the STA7130MC series is controlled at a fixed time generated by the corresponding internal oscillator. It also is switched in three levels by step current reference ratios. (See Table 4-3 for more details.)

In addition, the STA7130MC series provides a function that decreases power losses occurring when the PWM turns off. This function dissipates the back EMF stored in the motor coil at MOSFET turn-on, as well as at PWM turn-on (synchronous rectification operation).

Figure 14-5 explains differences between two back EMF generation mechanisms. Whereas the older version of our product series only performs ON/OFF operations using a MOSFET on the PWM-ON side, the STA7130MC series can perform ON/OFF operations using a MOSFET on the PWM-OFF side.

To prevent simultaneous switching of the MOSFETs at the synchronous rectification operation, the IC has a dead time of approximately 0.5 µs. During the dead time, the back EMF flows through the body diodes of the MOSFETs.

Figure 14-5. Difference in Back EMF Generation



Back EMF flows through the body diode of MOFSET during dead time.

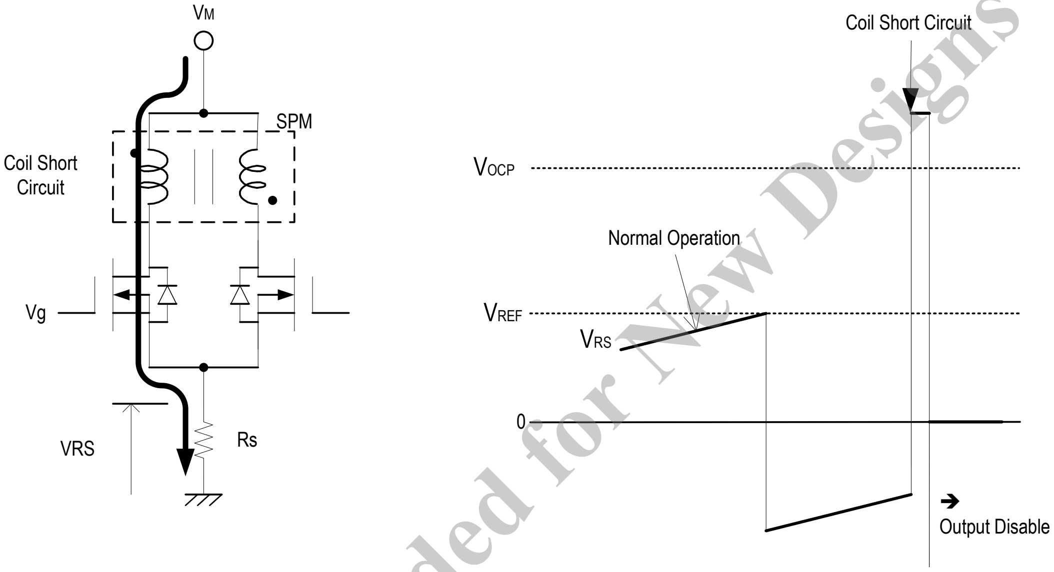
(2) Protection Functions

The STA7130MC series includes a motor coil short protection circuit, a motor coil open protection circuit, and an overheat protection circuit. Detailed explanations of each protection circuit are provided below.

[1] Motor Coil Short Circuit Protection (Load Short) Circuit

This protection circuit, embedded in the STA7130MC series, begins to operate when the device detects an increase in the sense resistor voltage level, V_{RS}. The threshold voltage of this protection circuit, V_{SOC}, is set to approximately 0.45 V. Outputs are disabled at the time the protection circuit starts, **where V_{RS} exceeds V_{SOC}.**

Figure 14-6. Motor Coil Short Protection Circuit Operation



NOTE: Overcurrent that flows without passing the sense resister is undetectable.

[2] Motor Coil Open Protection Circuit *(Patent acquired)*

Driver destruction can occur when one output pin (motor coil) is disconnected in unipolar drive operation. This is because a MOSFET connected after disconnection will be in an avalanche breakdown state, where very high energy is added with back EMF when PWM is off. With the avalanche state, an output cancels the energy stored in the motor coil where the resisting pressure between the drain and source of the MOSFET is reached (i.e., the condition in which the breakdown occurred).

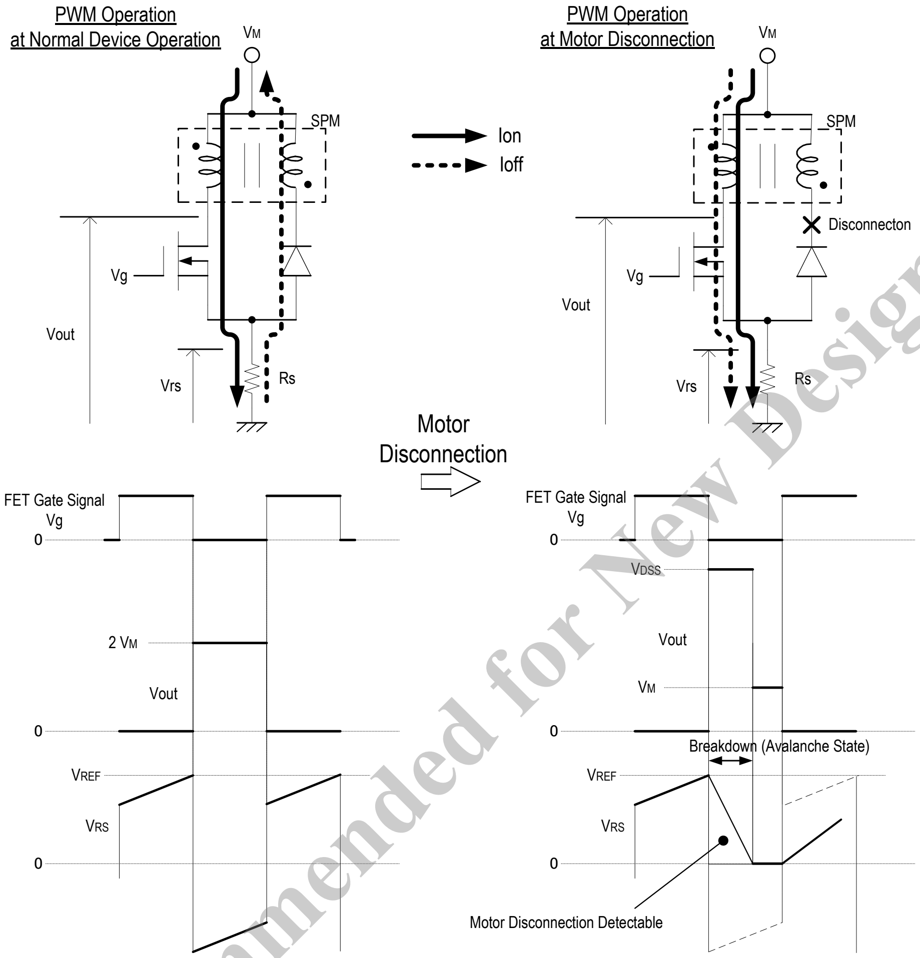
Although MOSFETs with a certain amount of an avalanche energy tolerance rating are used in the STA7130MC series, the avalanche energy tolerance falls as a temperature increases.

Because high energy is added repeatedly whenever PWM operation disconnects the MOSFET, the temperature of the MOSFET rises; and when the applied energy exceeds the tolerance, the driver will be destroyed. Therefore, a circuit which detects this avalanche state and protects the driver is added in the STA7130MC series.

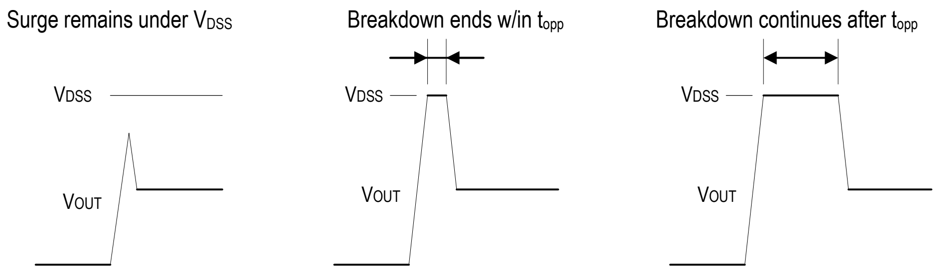
As explained above, when the motor coil is disconnected, accumulated voltage in the MOSFET causes a reverse current to flow during a PWM OFF-time. For this reason, V_{RS} that is negative during a PWM OFF-time in a normal operation becomes positive when the motor coil is disconnected. Thus, the disconnected motor is detectable by sensing that V_{RS} in the PWM OFF-time is positive.

In order to avoid detection malfunctions, the STA7130MC series actuates a dedicated protection function, the motor coil open protection circuit, when the motor disconnection state is detected three times continuously (see Figure 14-7).

Figure 14-7. Coil Open Protection Operation



NOTE: In addition to requiring three breakdown cycles to confirm the open circuit condition, the STA7130MC series provides a fixed delay, an overload disconnection undetected time (t_{opp}), before the protection is activated. This is to avoid false detections, which can be occurred by surge noise after PWM turn-off, causing an unwanted operation of the function even when the load is not actually disconnected. The figure below describes alternative t_{opp} scenarios. If a total period of breakdown time exceeds t_{opp}, the device shuts down the output. If this is the case, check the motor and wiring layout to reduce surge noise. Shortening the breakdown time will allow the protection circuit to function properly. (Variation among device variants and applications should be taken into consideration.) When there is no actual breakdown, normal operations will continue. One possible solution is adding a capacitor between the OUTx and GND pins, which could damp the surge noise sufficiently.



(A) Breakdown confirmed after 3 cycles

(B) No effect on operations

(C) Generates false detections

[3] Overheat Protection Circuit

When a product temperature rises and exceeds T_{tsd}, this protection circuit starts operating and sets all outputs to be disabled.

NOTE: This product series has multichip composition (one IC for control, four MOSFETs, and two chip resistors). Although main heat sources are the MOSFETs and chip resisters, the location which actually detects temperature is the control IC (MIC). Separated from these main heat sources, the control IC cannot detect a rapid temperature change. Accordingly, perform worst-case thermal evaluations, in which junction temperatures must not exceed a guaranteed value of 150 °C, in your application design phase.

15. Application Information

(1) Motor Current Ratio Setting

The motor current, I_O (Mode F, 100%), for the STA7130MC series is determined by the values chosen for the external components, R1, R2, and the current sense resistors, R_S, in the case of the sample application circuit shown in Figure 8-1. The formula to calculate I_O is shown below:

$$Io = \underline{\underline{\frac{R2}{R1+R2} \times V_{DD}}} \times \frac{1}{3} / Rs. \qquad (1)$$

The double-underlined term represents the reference voltage, V_{REF}.

If V_{REF} is set below 0.1 V, the accuracy of IO setting is more likely to be degraded due to the variation between individual devices and/or the impedance of application trace layout.

The standard voltage for current I_{TRIP} that the STA7130MC series controls is partially divided by internal DACs:

$$I_{TRIP} = \frac{V_{REF}}{R_S} \times \frac{1}{3} \times (\text{Mode Proportion}). \qquad (2)$$

(2) Lower Limit of Control Current

The STA7130MC series uses a self-oscillating PWM current-control topology in which an OFF-time is fixed. As energy stored in motor coil is eliminated within the fixed PWM OFF-time, coil current flows intermittently, as shown in Figure 15-1. Thus, average current decreases as well as motor torque decreases. The point at which current starts flowing to the coil is considered as the lower limit of the control current, $I_{O(min)}$, where I_{OUT} is a target current level.

The lower limit of control current differs by application conditions of the motor or other factors, but it can be calculated from the following formula:

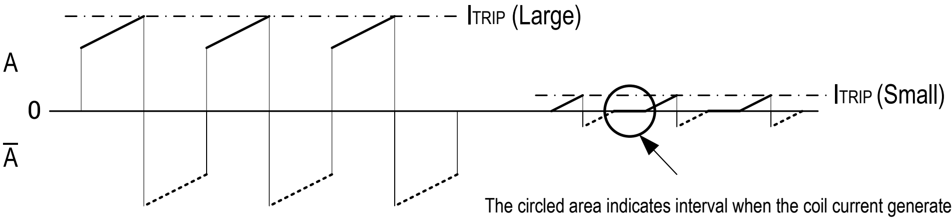
$$I_{O(\min)} = \frac{V_M}{R}\left(\frac{1}{\exp\left(-t_{OFF}/t_C\right)} - 1\right), \quad \text{with } t_C = \frac{L_m}{R}, \text{ and } R = R_m + R_{DS(on)} + R_S. \qquad (3)$$

Where:

V_M is the motor supply voltage,
$R_{DS(on)}$ is the MOS FET on-resistance,
R_m is the motor winding resistance,
L_m is the motor winding inductance,
t_{OFF} is the PWM OFF-time, and
R_S is the current sense resistor.

Even if the control current value is set at less than its lower limit, there is no setting at which the IC fails to operate. However, the control current will worsen against its target current.

Figure 15-1. Model Waveform of Control Current Lower Limit



(3) Avalanche Energy

In the unipolar topology of the STA7130MC series, a surge voltage (ringing noise) that exceeds the MOSFET capacity to withstand might be applied to the IC. To prevent damage, the STA7130MC series is designed with built-in MOSFETs having sufficient avalanche resistance to withstand this surge voltage. Therefore, even if surge voltages occur, users will be able to use the IC without any problems.

However, in case the motor harness used is too long or the IC is used above its rated current or voltage, there is a possibility that an avalanche energy could be applied that exceeds Sanken design expectations. Thus, users must test the avalanche energy applied to the IC under actual application conditions.

The following procedure can be used to check the avalanche energy in an application. Figure 15-2 and Figure 15-3 show test points and waveform characteristics resultant, respectively.

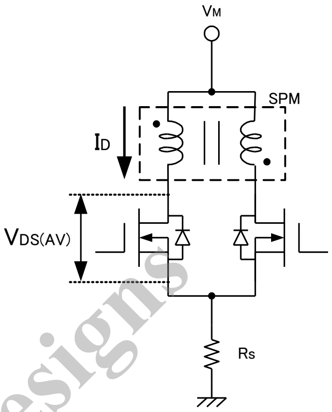


Figure 15-2. Test Points

From the waveform test result shown in Figure 15-3:

$V_{DS(AV)} = 80$ V,
$I_D = 1$ A, and
$t = 0.5$ μs.

The avalanche energy, E_{AV}, then can be calculated using the following formula:

$$E_{AV} \approx V_{DS(AV)} \times 1/2 \times I_D \times t \quad (4)$$

$$= 80\,(\text{V}) \times 1/2 \times 1\,(\text{A}) \times 0.5 \times 10^{-6}\,(\mu\text{s})$$

$$= 0.02\,(\text{mJ}).$$

By comparing the calculated E_{AV} values with the graph shown in Figure 15-4, the application can be evaluated if it is safe for the IC by being within the avalanche energy-tolerated dose range of the MOFSETs.

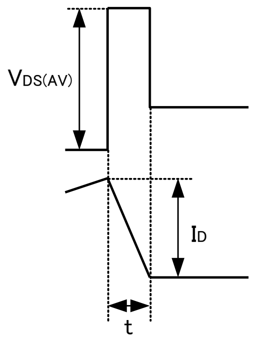
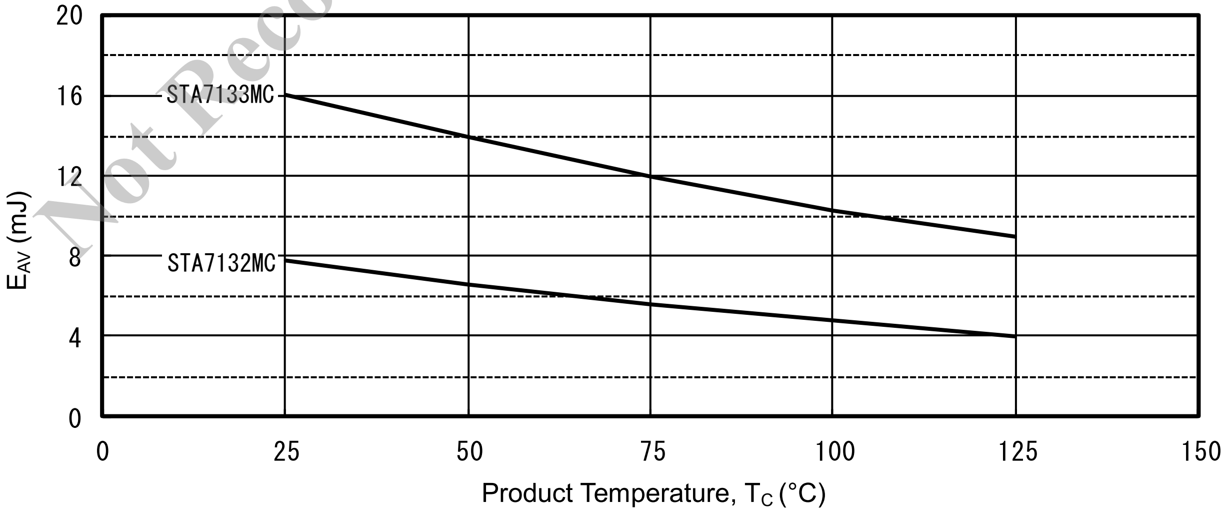


Figure 15-3. Waveform at Avalanche Breakdown

Figure 15-4. Iterated Avalanche Energy Tolerated Level, E_{AV}



(4) Motor Supply Voltage (V_M) and Main Power Supply Voltage (V_{BB})

Because the STA7130MC series has a structure that separates the control IC (MIC) and the power MOSFETs as shown in Figure 7-1, the motor supply and main power supply are electrically separated. Therefore, it is possible to drive the IC with using different power supplies and different voltages for the motor supply and the main power supply. However, extra caution is required because the supply voltage ranges differ among power supplies.

(5) Internal Logic Circuits

a. Reset for the Internal Sequencer

The sequencer/translator circuit embedded in this product series is initialized by the built-in power-on reset function, which is activated at a time when the main power supply (V_{BB}) is applied. Therefore, the output immediately after power-on indicates a status that the power circuits are in the home state.

When the sequencer/translator must be reset after the motor has been operating, a signal must be input on the RESET pin. In a case in which external reset control is not necessary and the RESET pin is not used, the RESET pin must be pulled to logic low on the application circuit board. When external reset controlling is not necessary and the RESET pin is not used, the RESET pin must be pulled to logic low on an application circuit board.

b. Clock Input

The STA7130MC series is designed to move one sequence increment at a time, according to the current stepping mode, when a positive clock pulse edge is detected.

When a clock input signal stops, the present excitation state enters a motor hold state. At this time, there is no difference to the IC if the clock input signal is at low level or high level.

c. Chopping Synchronous Circuit

The STA7130MC series has a chopping synchronous function to protect from abnormal noises that may occasionally occur during the motor Hold mode. This function can be operated by setting the SYNC pin at high level. However, if this function is used during motor rotation, control current does not stabilize; and that may result in reduced motor torque and/or increased vibration.

Note that the synchronous circuit should be disabled to control the motor current properly even when it is used in other than the 2-phase excitation state (Modes 8 and F) or the 1-phase excitation hold state.

In normal operation, an external microcomputer sends an input signal for switching. However, in applications where any input signals cannot be transmitted adequately due to a limited number of ports, the following method can be taken to use the function.

The schematic diagram in Figure 15-5 shows how the IC is designed so that a signal on the SYNC pin can be determined by an input signal on the CLOCK pin.

Figure 15-5. Clock Signal Shutoff Detection Circuit

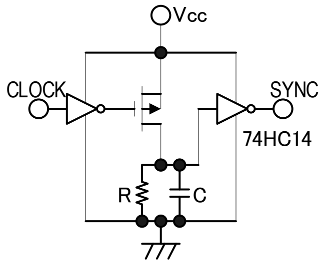
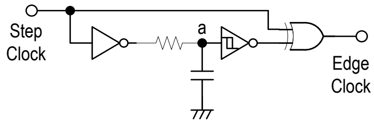


Figure 15-6. Clock Signal Edge Detection Circuit



When the CLOCK pin receives a logic high signal, the internal capacitor, C, is charged, and the SYNC pin signal is set to logic low. However, if the input signal on the CLOCK pin cannot rise above a logic low level, the capacitor is discharged by the internal resistor, R, and the SYNC pin signal is set to logic high, causing the IC to shift to the synchronous mode. RC time constant in the circuit should be determined by the minimum clock frequency used.

When using a sequence that keeps an input signal on the CLOCK pin at logic high, an inverter circuit must be added.

When the CLOCK pin signal is set at an undetermined level, an edge detection circuit (Figure 15-6) can be added to prepare a proper clock input signal, allowing correct processing by the circuit illustrated in Figure 15-5.

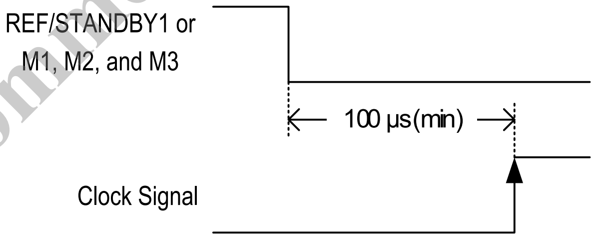
d. Output Disable Circuits (Standby1 and Standy2)

There are two methods to set the IC to a motor free-state (coast, with outputs disabled). One is to set the REF pin to more than 2 V (Standby1). And the other is to set all the excitation mode setting pins (M1, M2, and M3) to high (Standby2). In either way, the IC is put into the Standby mode, which stops the main power supply and reduces circuit current.

The difference between the two methods is that the Standby1 keeps the internal sequencer enabled, whereas the Standby2 puts the internal sequencer into a hold state. That is to say, in the Standby2 mode, the excitation sequence remains in the hold state even after a signal is input on the CLOCK pin. The Standby2 also works as a function to return from the state in which the protection function is activated.

When awaking to normal operation mode (motor rotation) from the Disable (Standby1 or Standby2) mode, set an appropriate delay time, i.e., a time period from cancellation of the Disable mode to an initial clock input edge. In doing so, consider not only a rise time for the IC, but also a rise time for the motor excitation current (Figure 15-7).

Figure 15-7. Timing Delay between Disable Mode Cancellation and the Next Clock Input



e. REF/STANDBY1 Pin

The REF pin provides access to the following functions:

[1] Reference voltage setting for output current setting: Low level ($V_{REF} \leq 0.9$ V)

[2] Output Enable-Disable control input: High level ($V_{REF} \geq 2.0$ V)

These functions are further described in Section 9, and in the discussion of output disabling, above. Moreover, the threshold voltage to switch the output enable-disable signals is set to approximately 1.75 V.

To control the REF voltage, pay attention to the following points:

Range A – Control current value varies in accordance with V_{REF}, not only within the range specified in [1], but also within the range from [1] to the threshold voltage (typically 1.75 V). Therefore, power dissipation in the IC and the sense resistors must be given extra consideration. In addition, note that OCP operation may start depending on the reference voltage splitting ratio.

Range B – In this range, the voltage that switches output enable and disable exists. At enable, the same cautions apply as in *Range A*. For some cases, there are possibilities that an output status will become unstable as a result of iterations between enable and disable states.

f. Logic Input Pins (CLOCK, RESET, CW/CCW, M1, M2, M3, and SYNC)

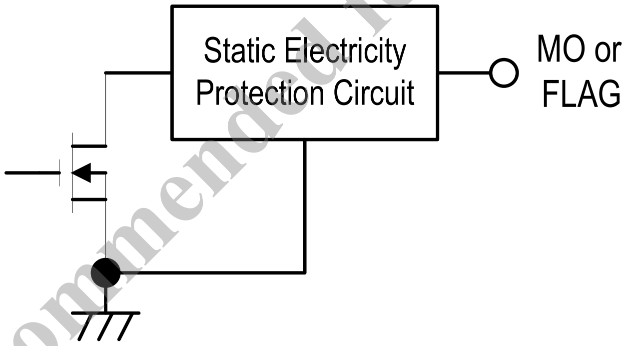
When a logic input pin (CLOCK, RESET, CW/CCW, M1, M2, M3, or SYNC) is not used, the pin must be tied to V_{DD} or GND.

Do not leave any of these pins floating, because there is possibility of undefined effects on IC performance if they are left open.

g. Monitor Output Pins (MO and FLAG)

The MO and FLAG output pins are designed as monitor outputs. Moreover, the IC consists of **an open-drain output** configuration, as shown in Figure 15-8. When using the monitor output pin, add a pull-up resistor of approximately 5.1 to 10 kΩ. Therefore, let these output pins open when they are not used.

Figure 15-8. MO/FLAG Pin General Internal Circuit Layout



16. Thermal Design Information

It is not practical to calculate the power dissipation of the STA7130MC series accurately, because that would require factors that are variable during operation, such as time periods and excitation modes during motor rotation, input frequencies and sequences, and so forth.

Given this situation, it is preferable to perform approximate calculations at worst conditions. The following is a simplified formula for the calculation of power dissipation using extracted minimum necessary parameters:

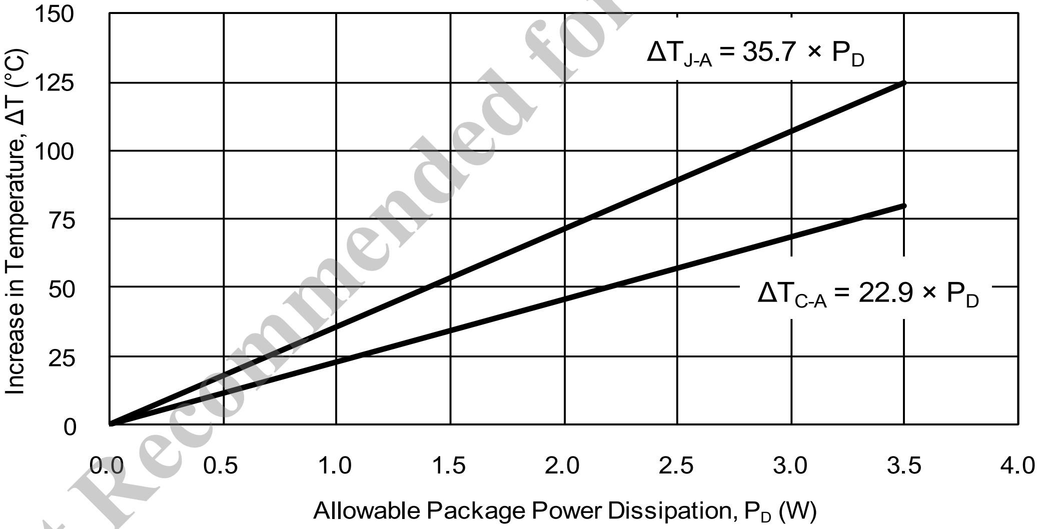
$$P = I^2 \times (R_{DS(on)} + Rs) \times 2,$$

where:

P is the power dissipation in the IC,
I is the operation current (≈ Io),
$R_{DS(on)}$ is the on-resistance of the output MOSFET, and
Rs is the current sense resistance.

Based on the power dissipation in the IC calculated using the above formula, the expected increase in operating junction temperature, ΔT_J, of the IC can be estimated using Figure 16-1. This result should be added to the worst-case ambient temperature when operating, $T_{A(max)}$. Based on the calculation, there is no problem unless $T_{A(max)} + \Delta T_J > 150$ °C. However, final confirmation should be made by measuring the IC temperature during operation and then verifying power dissipation and junction temperature in the corresponding graph in Figure 16-1.

Figure 16-1. Temperature Increase



When the IC is used with a heatsink mounted, product package thermal resistance, $\theta_{J\text{-}A}$, is a variable used in calculating $\Delta T_{J\text{-}A}$. The value of $\theta_{J\text{-}A}$ is calculated from the following formula:

$$\theta_{J\text{-}A} \approx \theta_{J\text{-}C} + \theta_{FIN} = (\theta_{J\text{-}A} - \theta_{C\text{-}A}) + \theta_{FIN},$$

where θ_{FIN} is the thermal resistance of the heatsink. Then, $\Delta T_{J\text{-}A}$ can be calculated with using the value of $\theta_{J\text{-}A}$.

The following procedure should be used to measure product temperature and to estimate junction temperature in actual operation.

First, measure a temperature rise in the center of backside of mold resin used for the device ($\Delta T_{C\text{-}A}$).

Second, estimate power dissipation (P) and junction temperature (T_J) from the temperature rise with reference to Figure 16-1, the Temperature Increase graph. At this point, the device temperature rise ($\Delta T_{C\text{-}A}$) and the junction temperature rise (T_J) become almost equivalent in the following formula:

$$\Delta T_J \approx \Delta T_{C\text{-}A} + P \times \theta_{J\text{-}C} .$$

CAUTION

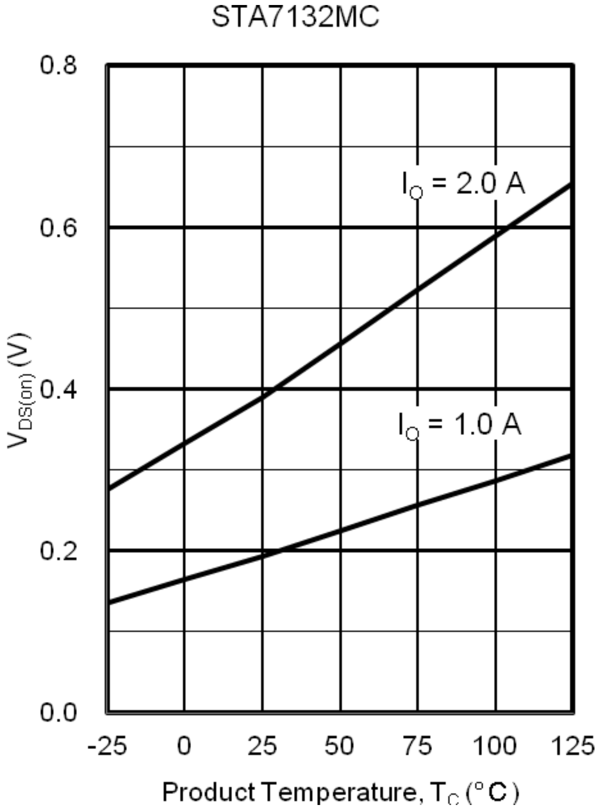
The STA7130MC series is designed as a multichip, consisting of four separate power elements (MOSFETs), one control IC (MIC), and two sense resistors. Moreover, because the control IC cannot accurately detect the temperature of the built-in power elements, which are the primary sources of heat, the STA7130MC series does not provide a protection function against overheating. For thermal protection, users must conduct sufficient thermal evaluations to ensure that the junction temperature of the IC does not exceed a guaranteed level of 150 °C.

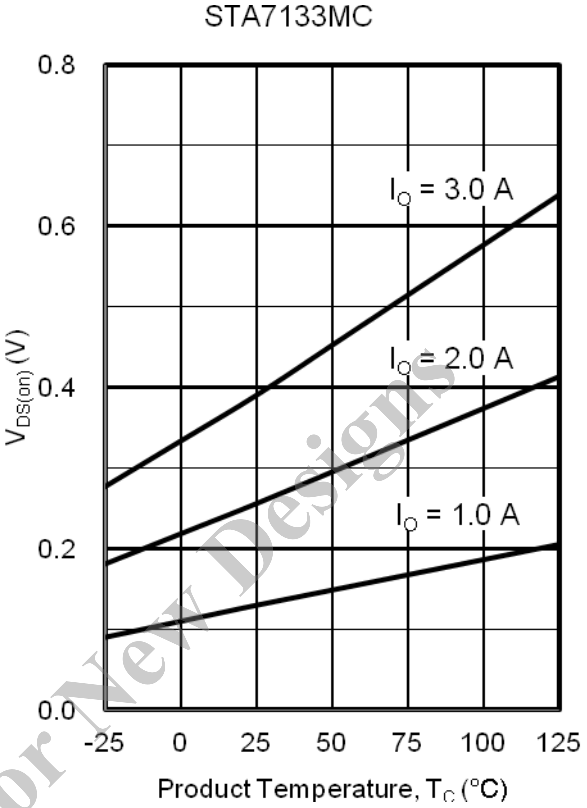
This thermal design information is provided for preliminary design estimations only. Before operating the IC in an application, users must experimentally determine its actual thermal performance (the case temperature of Pin 10). The maximum recommended case temperatures (Pin 10) for the IC are:

- With no external heatsink connection: 85 °C
- With external heatsink connection: 75 °C

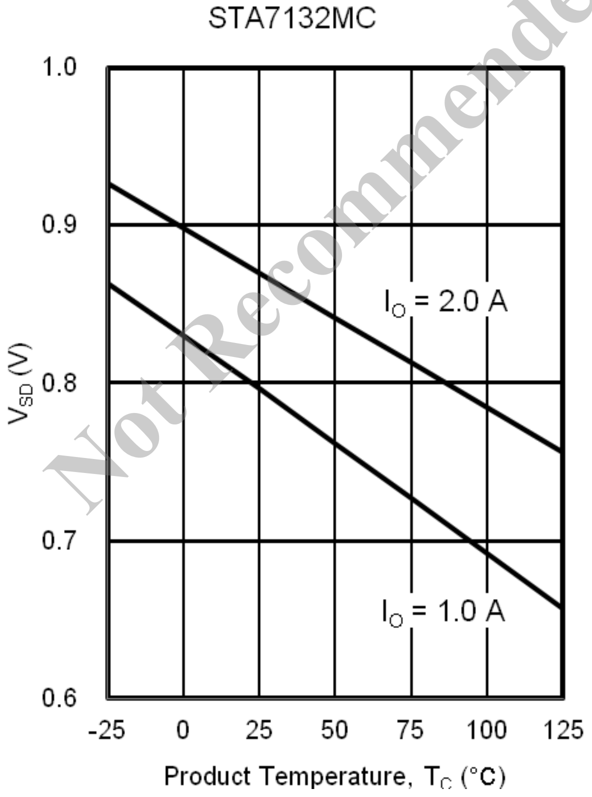
17. Characteristics Data

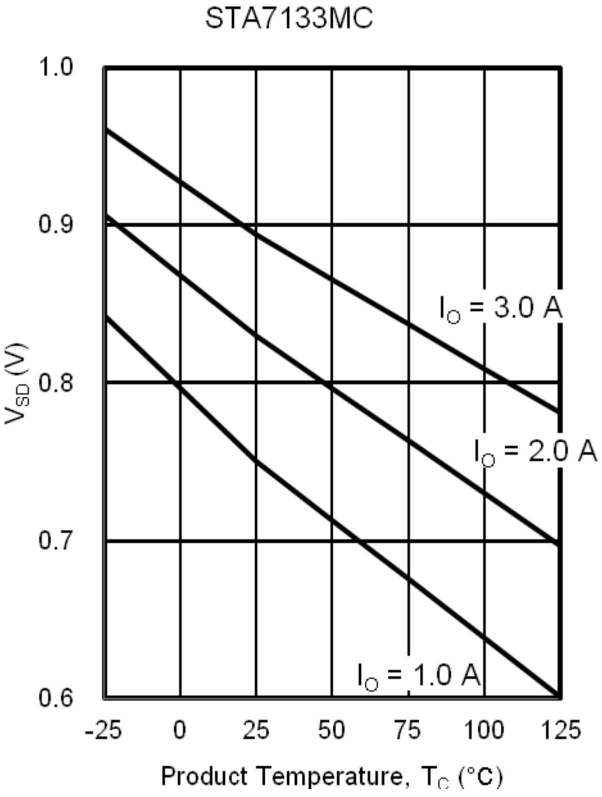
(1) Output MOSFET On-Voltage, $V_{DS(on)}$





(2) Output MOSFET Body Diodes Forward Voltage, V_F





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