

NTTFS5C673NL

Power MOSFET

60 V, 9.3 mΩ, 50 A, Single N-Channel

Features

- Small Footprint (3.3x3.3 mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

| Parameter | Symbol | Value | Unit | |
|---|--|---------------------------|------------------|---|
| Drain-to-Source Voltage | V_{DSS} | 60 | V | |
| Gate-to-Source Voltage | V_{GS} | ± 20 | V | |
| Continuous Drain Current $R_{\theta JC}$ (Notes 1, 3) | Steady State | $T_C = 25^\circ\text{C}$ | I_D 50 | A |
| | | $T_C = 100^\circ\text{C}$ | 35 | |
| Power Dissipation $R_{\theta JC}$ (Note 1) | Steady State | $T_C = 25^\circ\text{C}$ | P_D 46 | W |
| | | $T_C = 100^\circ\text{C}$ | 23 | |
| Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2, 3) | Steady State | $T_A = 25^\circ\text{C}$ | I_D 13 | A |
| | | $T_A = 100^\circ\text{C}$ | 9 | |
| Power Dissipation $R_{\theta JA}$ (Notes 1 & 2) | Steady State | $T_A = 25^\circ\text{C}$ | P_D 3.1 | W |
| | | $T_A = 100^\circ\text{C}$ | 1.6 | |
| Pulsed Drain Current | $T_A = 25^\circ\text{C}, t_p = 10 \mu\text{s}$ | I_{DM} 290 | A | |
| Operating Junction and Storage Temperature | T_J, T_{stg} | -55 to +175 | $^\circ\text{C}$ | |
| Source Current (Body Diode) | I_S | 52 | A | |
| Single Pulse Drain-to-Source Avalanche Energy ($I_{L(pk)} = 2.3 \text{ A}$) | E_{AS} | 88 | mJ | |
| Lead Temperature for Soldering Purposes (1/8" from case for 10 s) | T_L | 260 | $^\circ\text{C}$ | |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

| Parameter | Symbol | Value | Unit |
|---|-----------------|-------|---------------------------|
| Junction-to-Case – Steady State | $R_{\theta JC}$ | 3.2 | $^\circ\text{C}/\text{W}$ |
| Junction-to-Ambient – Steady State (Note 2) | $R_{\theta JA}$ | 48 | |

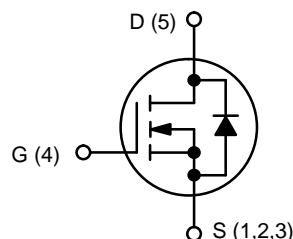
1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface-mounted on FR4 board using a 650 mm², 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.



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| $V_{(BR)DSS}$ | $R_{DS(on)}$ MAX | I_D MAX |
|---------------|------------------|-----------|
| 60 V | 9.3 mΩ @ 10 V | 50 A |
| | 13.3 mΩ @ 4.5 V | |

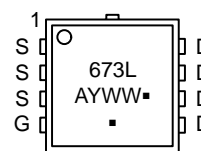


N-CHANNEL MOSFET



WDFN8
(μ8FL)
CASE 511AB

MARKING DIAGRAM



673L = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

NTTFS5C673NL

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|-------------------|---|---------------------------|-----|-----|----------------------|
| OFF CHARACTERISTICS | | | | | | |
| Drain-to-Source Breakdown Voltage | $V_{(BR)DSS}$ | $V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$ | 60 | | | V |
| Drain-to-Source Breakdown Voltage Temperature Coefficient | $V_{(BR)DSS}/T_J$ | | | 28 | | mV/ $^\circ\text{C}$ |
| Zero Gate Voltage Drain Current | I_{DSS} | $V_{GS} = 0\text{ V}, V_{DS} = 60\text{ V}$ | $T_J = 25^\circ\text{C}$ | | 10 | μA |
| | | | $T_J = 125^\circ\text{C}$ | | 250 | |
| Gate-to-Source Leakage Current | I_{GSS} | $V_{DS} = 0\text{ V}, V_{GS} = 20\text{ V}$ | | | 100 | nA |

ON CHARACTERISTICS (Note 4)

| | | | | | | |
|-----------------------------------|------------------|--|-----|------|------|----------------------|
| Gate Threshold Voltage | $V_{GS(TH)}$ | $V_{GS} = V_{DS}, I_D = 35\ \mu\text{A}$ | 1.2 | | 2.0 | V |
| Threshold Temperature Coefficient | $V_{GS(TH)}/T_J$ | | | -4.5 | | mV/ $^\circ\text{C}$ |
| Drain-to-Source On Resistance | $R_{DS(on)}$ | $V_{GS} = 10\text{ V}, I_D = 25\text{ A}$ | | 8.0 | 9.3 | m Ω |
| | | $V_{GS} = 4.5\text{ V}, I_D = 25\text{ A}$ | | 11 | 13.3 | |
| Forward Transconductance | g_{FS} | $V_{DS} = 15\text{ V}, I_D = 25\text{ A}$ | | 37 | | S |

CHARGES AND CAPACITANCES

| | | | | | | |
|------------------------------|--------------|--|--|-----|--|----|
| Input Capacitance | C_{ISS} | $V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = 25\text{ V}$ | | 880 | | pF |
| Output Capacitance | C_{OSS} | | | 450 | | |
| Reverse Transfer Capacitance | C_{RSS} | | | 11 | | |
| Total Gate Charge | $Q_{G(TOT)}$ | $V_{GS} = 4.5\text{ V}, V_{DS} = 30\text{ V}; I_D = 25\text{ A}$ | | 4.5 | | nC |
| Total Gate Charge | $Q_{G(TOT)}$ | $V_{GS} = 10\text{ V}, V_{DS} = 30\text{ V}; I_D = 25\text{ A}$ | | 9.5 | | nC |
| Threshold Gate Charge | $Q_{G(TH)}$ | $V_{GS} = 4.5\text{ V}, V_{DS} = 30\text{ V}; I_D = 25\text{ A}$ | | 1.0 | | nC |
| Gate-to-Source Charge | Q_{GS} | | | 2.0 | | |
| Gate-to-Drain Charge | Q_{GD} | | | 0.8 | | |
| Plateau Voltage | V_{GP} | | | 2.9 | | |

SWITCHING CHARACTERISTICS (Note 5)

| | | | | | | |
|---------------------|--------------|---|--|-----|--|----|
| Turn-On Delay Time | $t_{d(ON)}$ | $V_{GS} = 4.5\text{ V}, V_{DS} = 30\text{ V}, I_D = 25\text{ A}, R_G = 2.5\ \Omega$ | | 9.0 | | ns |
| Rise Time | t_r | | | 50 | | |
| Turn-Off Delay Time | $t_{d(OFF)}$ | | | 13 | | |
| Fall Time | t_f | | | 3.0 | | |

DRAIN-SOURCE DIODE CHARACTERISTICS

| | | | | | | | |
|-------------------------|----------|--|---------------------------|----|-----|-----|----|
| Forward Diode Voltage | V_{SD} | $V_{GS} = 0\text{ V}, I_S = 25\text{ A}$ | $T_J = 25^\circ\text{C}$ | | 0.9 | 1.2 | V |
| | | | $T_J = 125^\circ\text{C}$ | | 0.8 | | |
| Reverse Recovery Time | t_{RR} | $V_{GS} = 0\text{ V}, di/dt = 100\text{ A}/\mu\text{s}, I_S = 25\text{ A}$ | | 28 | | ns | |
| Charge Time | t_a | | | 14 | | | |
| Discharge Time | t_b | | | 14 | | | |
| Reverse Recovery Charge | Q_{RR} | | | 18 | | | nC |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.

5. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

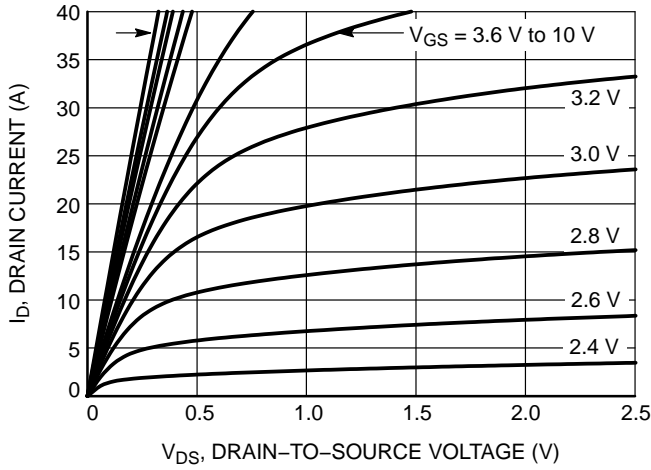


Figure 1. On-Region Characteristics

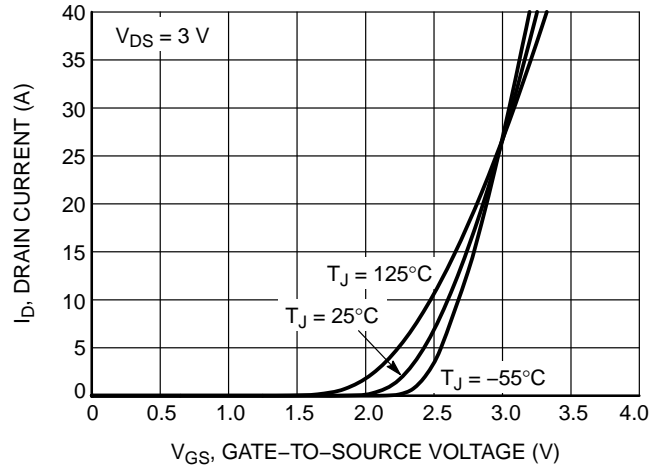


Figure 2. Transfer Characteristics

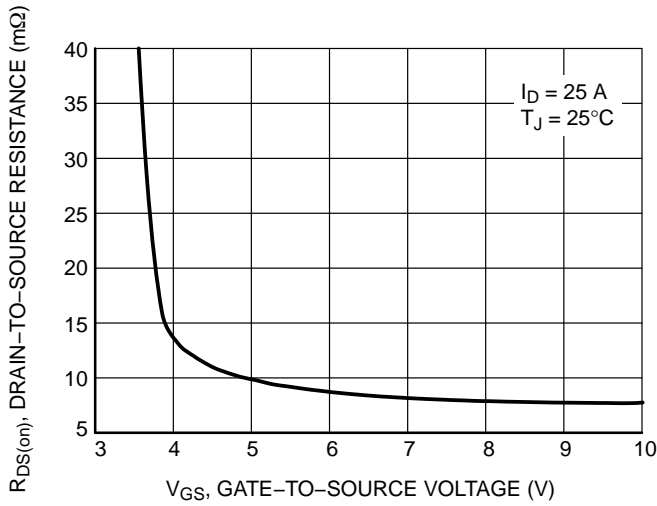


Figure 3. On-Resistance vs. Gate-to-Source Voltage

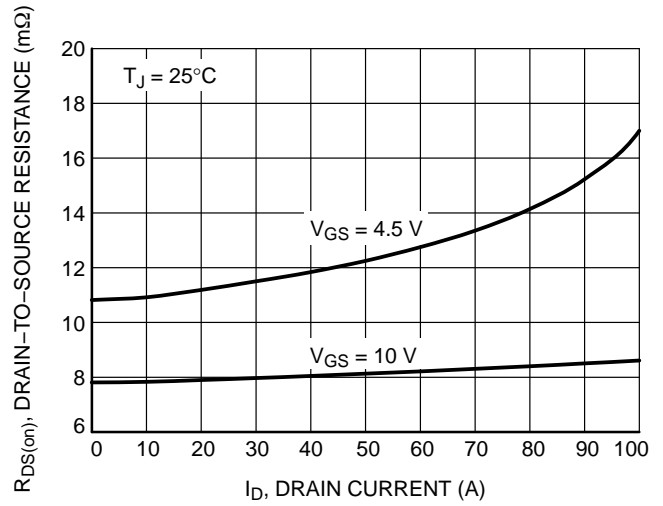


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

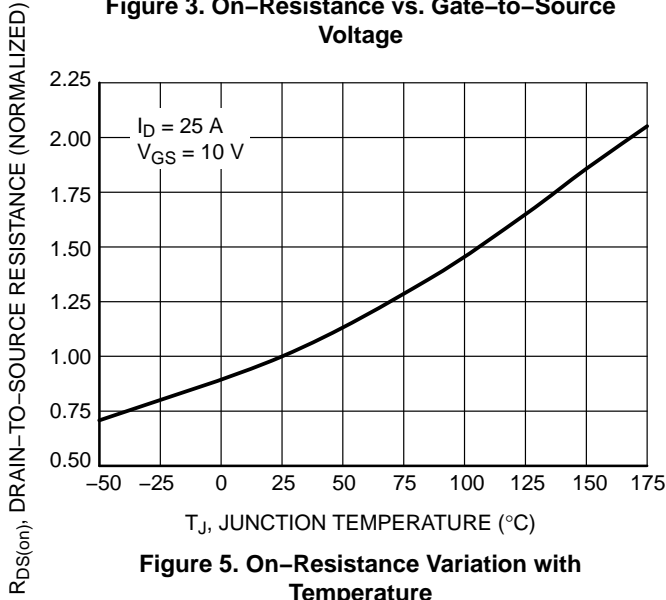


Figure 5. On-Resistance Variation with Temperature

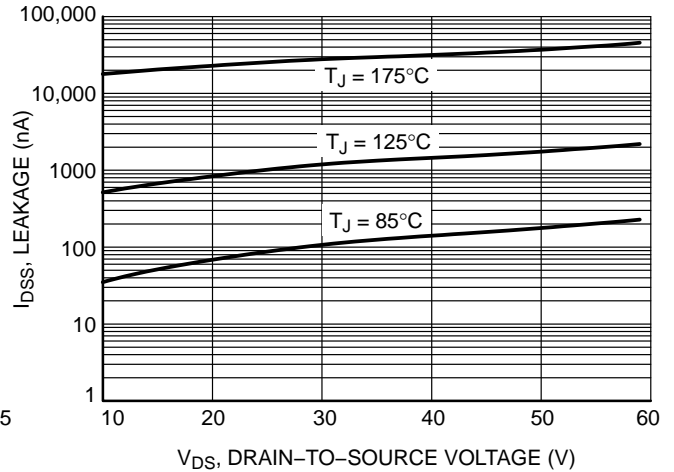


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

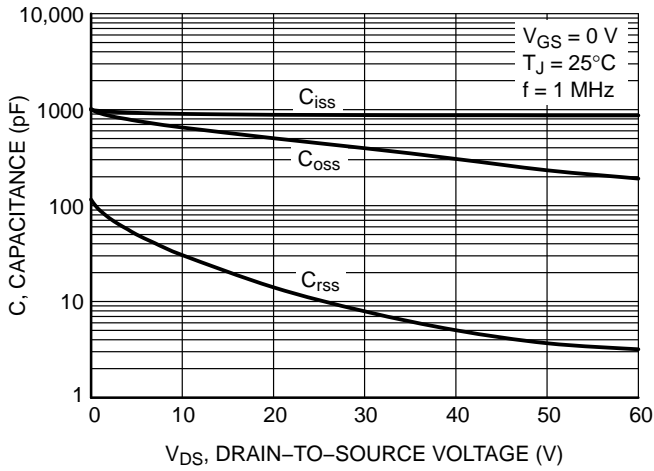


Figure 7. Capacitance Variation

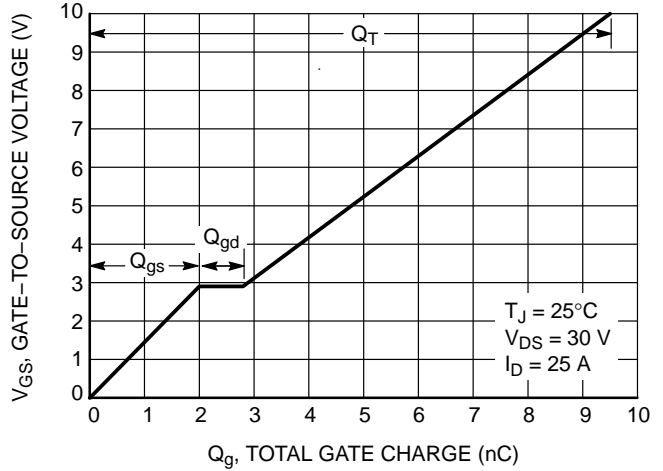


Figure 8. Gate-to-Source vs. Total Charge

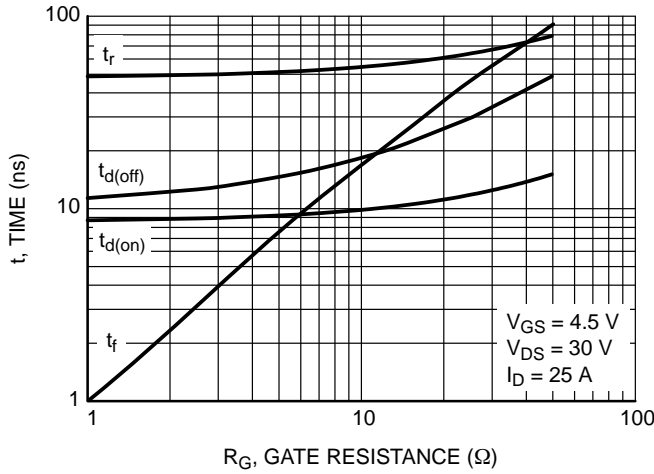


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

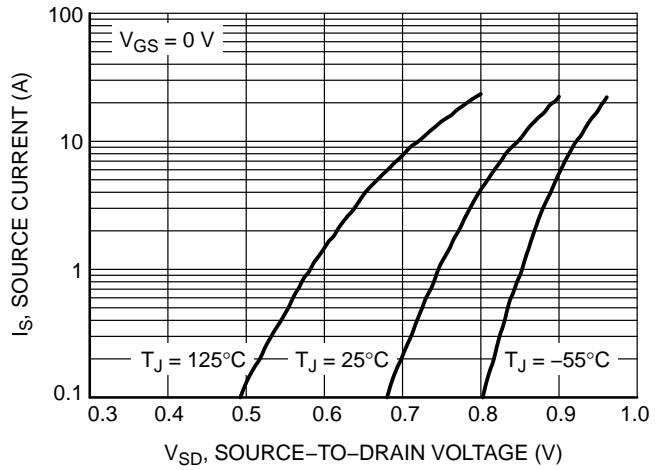


Figure 10. Diode Forward Voltage vs. Current

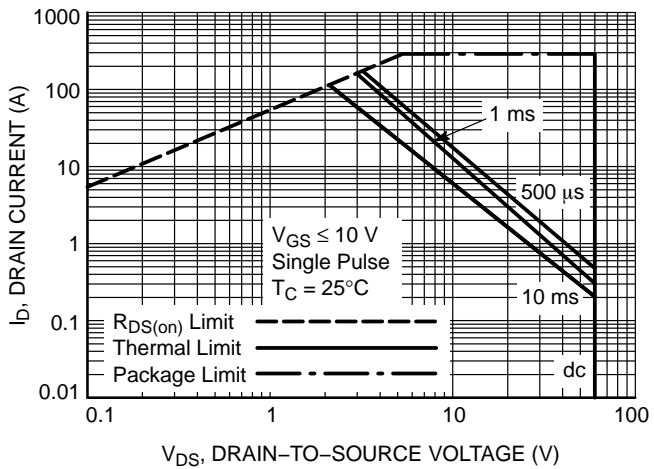


Figure 11. Maximum Rated Forward Biased Safe Operating Area

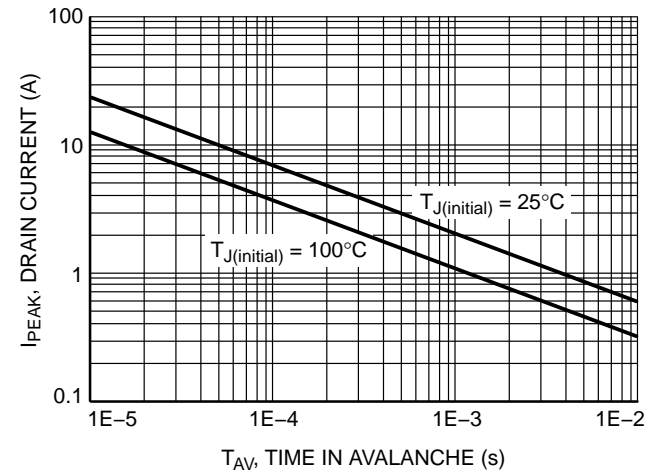


Figure 12. Maximum Drain Current vs. Time in Avalanche

NTTFS5C673NL

TYPICAL CHARACTERISTICS

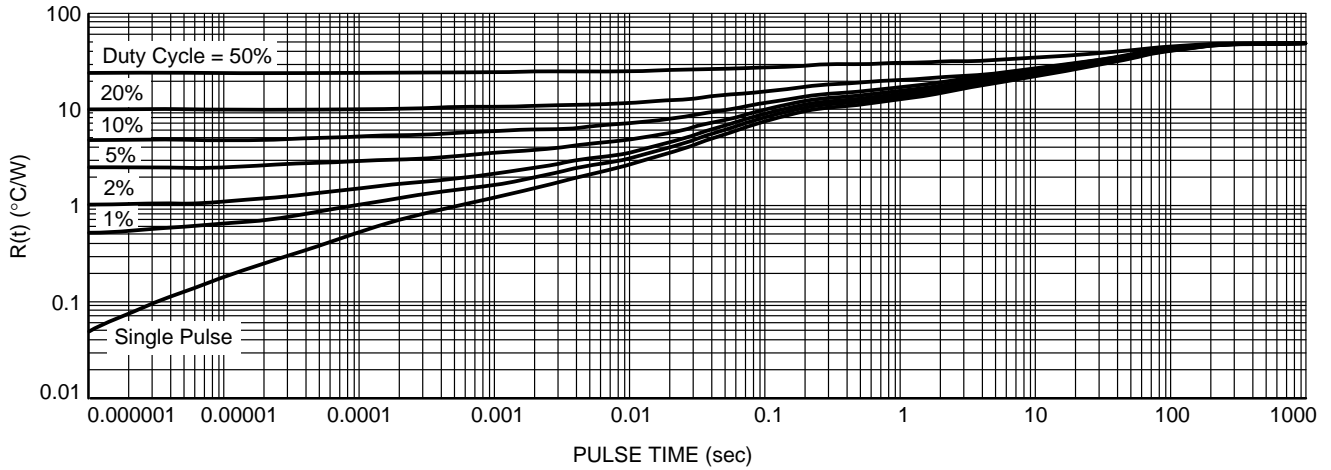


Figure 13. Thermal Response

DEVICE ORDERING INFORMATION

| Device | Marking | Package | Shipping† |
|-----------------|---------|-------------------|--------------------|
| NTTFS5C673NLTAG | 673L | DFN5 (Pb-Free) | 1500 / Tape & Reel |
| NTTFS5C673NLTWG | 673L | DFN5 (Pb-Free) | 5000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE

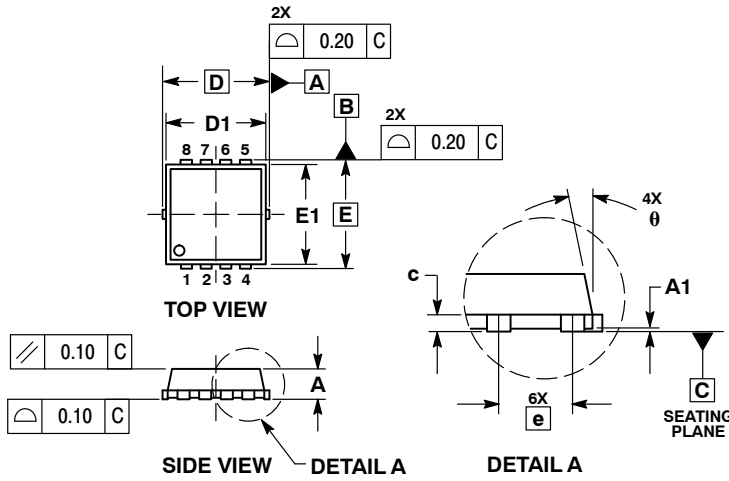
PACKAGE DIMENSIONS



SCALE 2:1

WDFN8 3.3x3.3, 0.65P
CASE 511AB
ISSUE D

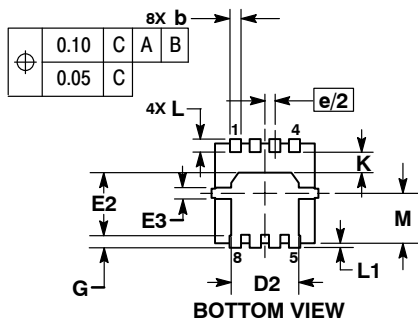
DATE 23 APR 2012



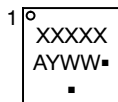
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

| DIM | MILLIMETERS | | | INCHES | | |
|-----|-------------|------|------|-----------|-------|-------|
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | 0.70 | 0.75 | 0.80 | 0.028 | 0.030 | 0.031 |
| A1 | 0.00 | --- | 0.05 | 0.000 | --- | 0.002 |
| b | 0.23 | 0.30 | 0.40 | 0.009 | 0.012 | 0.016 |
| c | 0.15 | 0.20 | 0.25 | 0.006 | 0.008 | 0.010 |
| D | 3.30 BSC | | | 0.130 BSC | | |
| D1 | 2.95 | 3.05 | 3.15 | 0.116 | 0.120 | 0.124 |
| D2 | 1.98 | 2.11 | 2.24 | 0.078 | 0.083 | 0.088 |
| E | 3.30 BSC | | | 0.130 BSC | | |
| E1 | 2.95 | 3.05 | 3.15 | 0.116 | 0.120 | 0.124 |
| E2 | 1.47 | 1.60 | 1.73 | 0.058 | 0.063 | 0.068 |
| E3 | 0.23 | 0.30 | 0.40 | 0.009 | 0.012 | 0.016 |
| e | 0.65 BSC | | | 0.026 BSC | | |
| G | 0.30 | 0.41 | 0.51 | 0.012 | 0.016 | 0.020 |
| K | 0.65 | 0.80 | 0.95 | 0.026 | 0.032 | 0.037 |
| L | 0.30 | 0.43 | 0.56 | 0.012 | 0.017 | 0.022 |
| L1 | 0.06 | 0.13 | 0.20 | 0.002 | 0.005 | 0.008 |
| M | 1.40 | 1.50 | 1.60 | 0.055 | 0.059 | 0.063 |
| θ | 0° | --- | 12° | 0° | --- | 12° |



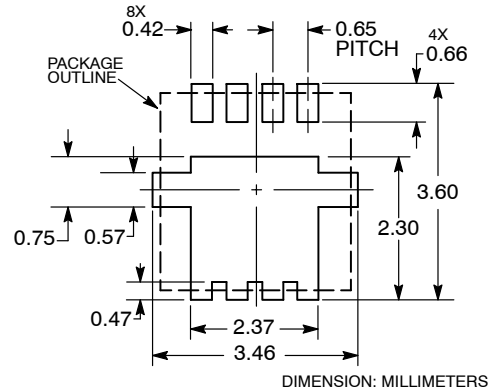
GENERIC MARKING DIAGRAM*



- XXXXX = Specific Device Code
- A = Assembly Location
- Y = Year
- WW = Work Week
- = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

| | | |
|------------------|----------------------|--|
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| DESCRIPTION: | WDFN8 3.3X3.3, 0.65P | PAGE 1 OF 1 |

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