THC63LVDM83E

28bits LVTTL/CMOS to 4ch LVDS Serializer/Transmitter

General Description

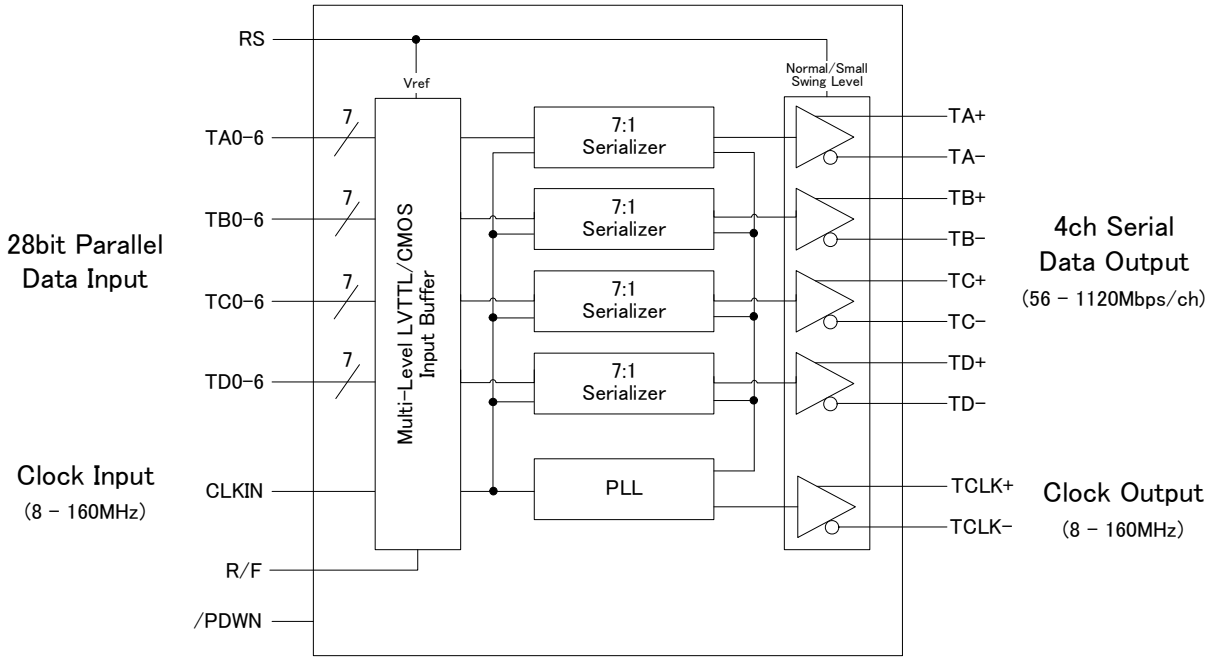
The THC63LVDM83E is a general purpose data serializer based on LVDS technology with no overhead for protocol or encoding.

The THC63LVDM83E converts 28bits of CMOS/TTL data into 4ch LVDS data stream. The transmitter can be programmed for rising edge or falling edge clocks through a dedicated pin.

Features

- 49pin 0.65mm pitch VFBGA Package
- Wide Input clock range: 8-160MHz
- Maximum total throughput 4.48Gbit/s@160MHz
- 3.3/2.5/1.8/1.2V voltage logic input
- LVDS swing is reducible by RS-pin to reduce EMI and power consumption.
- PLL requires no external components.
- On chip jitter filtering.
- Spread Spectrum Clock input tolerant.
- Power down mode.
- Input clock triggering edge is selectable by R/F-pin.
- Operates from a Single 3.3V Supply and 110mW(typ.) at 75MHz.

Block Diagram



Ball Out

TOP VIEW

	1	2	3	4	5	6	7
A	TA6	TA5	TA4	TA3	TA2	TA1	TA0
B	TB4	TD3	TD2	TD1	TD0	TA−	TA+
C	TB5	TB0	GND	VCC	RS	TB−	TB+
D	TB6	TB1	GND	LVDS VCC	LVDS VCC	TC−	TC+
E	TC0	TB2	GND	PLL VCC	R/F	TCLK−	TCLK+
F	TC1	TB3	TD4	TD5	TD6	TD−	TD+
G	TC2	TC3	TC4	TC5	TC6	CLKIN	/PDWN

Pin Description

<table>
<tr><th>Pin Name</th><th>Pin #</th><th>Type</th><th>Description</th></tr>
<tr><td>TA+, TA-</td><td>B7, B6</td><td rowspan="4">LVDS Output</td><td rowspan="3">4ch Serial Data Output</td></tr>
<tr><td>TB+, TB-</td><td>C7, C6</td></tr>
<tr><td>TC+, TC-</td><td>D7, D6</td></tr>
<tr><td>TD+, TD-</td><td>F7, F6</td></tr>
<tr><td>TCLK+, TCLK-</td><td>E7, E6</td><td>Clock Output</td></tr>
<tr><td>TA0 ~ TA6</td><td>A7,A6,A5,A4,A3,A2,A1</td><td rowspan="5">3.3V LVTTL
2.5/1.8/1.2V CMOS
Digital Input</td><td rowspan="4">28bit Parallel Data Input</td></tr>
<tr><td>TB0 ~ TB6</td><td>C2,D2,E2,F2,B1,C1,D1</td></tr>
<tr><td>TC0 ~ TC6</td><td>E1,F1,G1,G2,G3,G4,G5</td></tr>
<tr><td>TD0 ~ TD6</td><td>B5,B4,B3,B2,F3,F4,F5</td></tr>
<tr><td>CLKIN</td><td>G6</td><td>Clock Input</td></tr>
<tr><td>/PDWN</td><td>G7</td><td rowspan="2">3.3V LVTTL
Digital Input</td><td>Power Down Control
H: Normal operation
L: Power Down (All output are Hi-Z.)</td></tr>
<tr><td>R/F</td><td>E5</td><td>Input Clock Triggering Edge Select
H: Rising edge
L: Falling edge</td></tr>
<tr><td>RS</td><td>C5</td><td>Analog Input</td><td>Input/output Level Select and 2.5/1.8/1.2V Logic level Reference Voltage Input
<table>
<tr><th>RS-pin Input Voltage Setting</th><th>Data/Clock Input Voltage</th><th>Input Buffer Vref</th><th>LVDS Output VOD</th></tr>
<tr><td>VCC</td><td>3.3V</td><td>VCC/2</td><td rowspan="4">350mV</td></tr>
<tr><td>1.25V</td><td>2.5V</td><td>1.25V</td></tr>
<tr><td>0.9V</td><td>1.8V</td><td>0.9V</td></tr>
<tr><td>0.6V</td><td>1.2V</td><td>0.6V</td></tr>
<tr><td>GND</td><td>3.3V</td><td>VCC/2</td><td>200mV</td></tr>
</table></td></tr>
<tr><td>VCC</td><td>C4</td><td rowspan="4">Power</td><td>Power Supply Pin for LVTTL/CMOS input and digital circuit.</td></tr>
<tr><td>GND</td><td>C3,D3,E3</td><td>Ground Pins for Common.</td></tr>
<tr><td>LVDS VCC</td><td>D4,D5</td><td>Power Supply Pins for LVDS Outputs.</td></tr>
<tr><td>PLL VCC</td><td>E4</td><td>Power Supply Pin for PLL circuit.</td></tr>
</table>

Absolute Maximum Ratings

Parameter	Min	Max	Units
Supply Voltage	-0.3	+4.0	V
LVTTL/CMOS and Analog Input Voltage	-0.3	VCC + 0.3	V
LVDS Transmitter Output Voltage	-0.3	VCC + 0.3	V
Output Current	-30	30	mA
Junction Temperature	-	+125	°C
Storage Temperature	-55	+125	°C
Reflow Peak Temperature	-	+260	°C
Reflow Peak Temperature Time	-	10	sec
Maximum Power Dissipation @+25°C	-	1.2	W

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
VCC	All Supply Voltage	3.0	3.3	3.6	V
Ta	Operating Ambient Temperature	0	25	+70	°C
CLKIN	Clock Frequency	8	-	160	MHz

Power Consumption

VCC = 3.0~3.6V, Ta= 0~+70ºC

Symbol	Parameter	Conditions	Typ*	Max	Units
I_{TCCW}	LVDS Transmitter Operating Current Gray Scale Pattern 16(Fig.1)	RL=100Ω, CL=5pF, f=85MHz RS=VCC, (RS=GND)	42 (34)	-	mA
		RL=100Ω, CL=5pF, f=160MHz RS=VCC, (RS=GND)	58 (50)	-	mA
	LVDS Transmitter Operating Current Worst Case Pattern(Fig.2)	RL=100Ω, CL=5pF, f=85MHz RS=VCC, (RS=GND)	45 (36)	67 (56)	mA
		RL=100Ω, CL=5pF, f=160MHz RS=VCC, (RS=GND)	63 (55)	92 (80)	mA
I_{TCCS}	LVDS Transmitter Power Down Current		-	10	µA

*Typ values are at VCC=3.3V, Ta = +25ºC

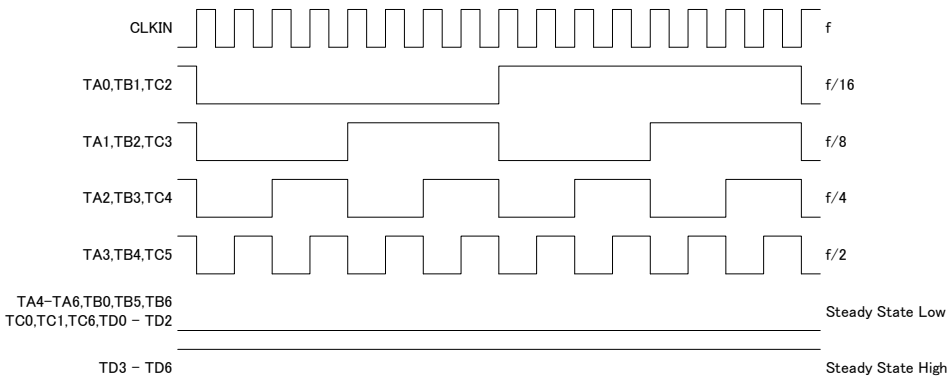


Figure 1. 16 Grayscale Pattern

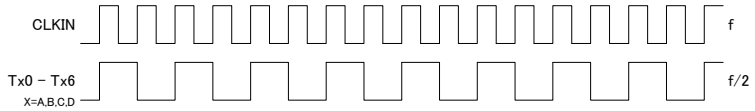


Figure 2. Worst Case Pattern

LVTTL/CMOS DC Specifications

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	High Level Input Voltage	3.3V LVTTL V_{ref} =VCC/2	2.0	-	VCC	V
		2.5/1.8/1.2V CMOS V_{ref} = RS Input Voltage	V_{ref} +0.1	-	VCC	
V_{IL}	Low Level Input Voltage	3.3V LVTTL V_{ref} =VCC/2	GND	-	0.8	V
		2.5/1.8/1.2V CMOS V_{ref} = RS Input Voltage	GND	-	V_{ref} -0.1	
I_{INC}	Input Current	GND ≤ V_{IN} ≤ VCC	-	-	±10	μA

*Typ values are at VCC=3.3V, Ta = +25ºC.

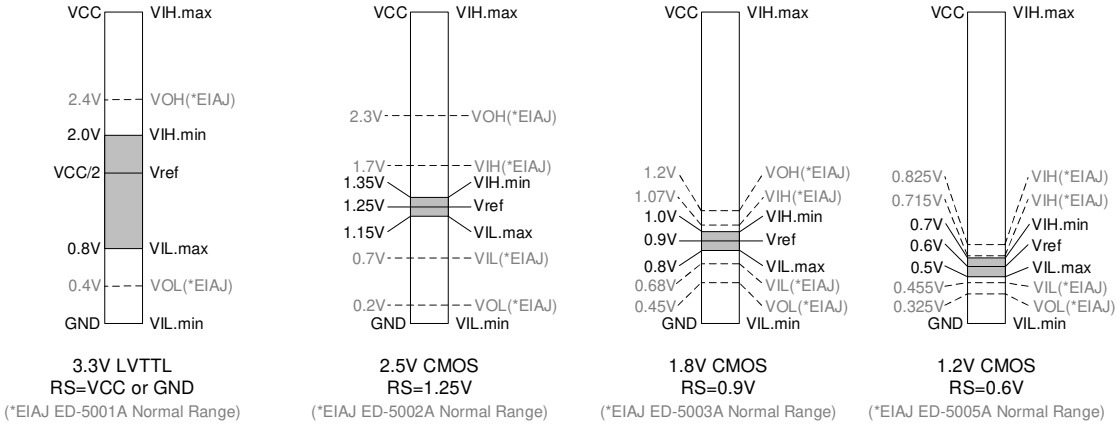


Figure 3. LVTTL/CMOS Digital Input Compatibility

LVDS DC Specifications

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
VOD	Differential Output Voltage	RS=VCC, 0.6 ~ 1.4V RL=100Ω	250	350	450	mV
		RS=GND RL=100Ω	120	200	300	mV
ΔVOD	Change in VOD between complementary output states	RL=100Ω	-	-	35	mV
VOC	Common Mode Voltage	RL=100Ω	1.125	1.25	1.375	V
ΔVOC	Change in VOC between complementary output states	RL=100Ω	-	-	35	mV
I_{OS}	Output Short Circuit Current	V_{OUT}=GND, RL=100Ω	-	-	-24	mA
I_{OZ}	Output TRI-STATE Current	/PDWN=GND, V_{OUT}=GND to VCC	-	-	±10	μA

*Typ values are at VCC=3.3V, Ta = +25ºC.

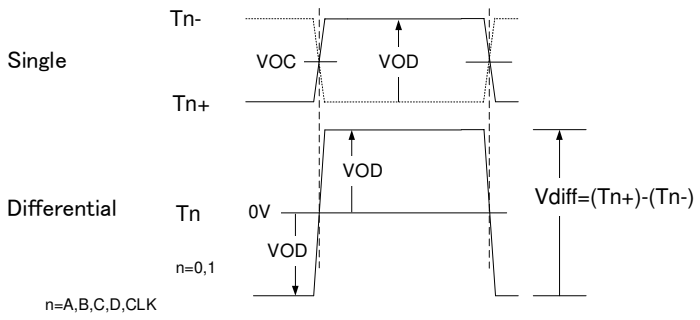


Figure 4. LVDS DC Specifications

LVTTL/CMOS AC Specifications

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Units
t_{TCIT}	CLKIN Transition Time	-	-	5.0	ns
t_{TCP}	CLKIN Period	6.25	T	125	ns
t_{TCH}	CLKIN High Time	0.35T	0.5T	0.65T	ns
t_{TCL}	CLKIN Low Time	0.35T	0.5T	0.65T	ns
t_{TCD}	CLKIN to TCLK+/- Delay	-	3T	-	ns
t_{TS}	Tx0-6 Setup time to CLKIN	2.0	-	-	ns
t_{TH}	Tx0-6 Hold time to CLKIN	0.0	-	-	ns

*Typ values are at VCC=3.3V, Ta = +25ºC

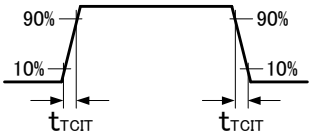


Figure 5. CLKIN Transmission Time

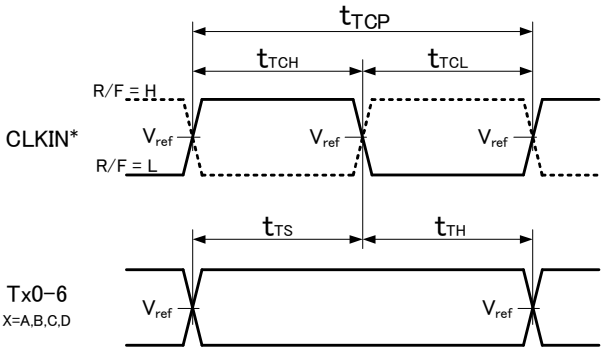


Figure 6. LVTTL/CMOS Input Timings

LVDS AC Specifications

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Units
t_{LVT}	LVDS Transition Time	-	0.6	1.5	ns
t_{TOP1}	Output Data Position0 (T=6.25ns ~ 20ns)	-0.15	0.0	+0.15	ns
t_{Top0}	Output Data Position1 (T=6.25ns ~ 20ns)	T/7-0.15	T/7	T/7+0.15	ns
t_{Top6}	Output Data Position2 (T=6.25ns ~ 20ns)	2T/7-0.15	2T/7	2T/7+0.15	ns
t_{Top5}	Output Data Position3 (T=6.25ns ~ 20ns)	3T/7-0.15	3T/7	3T/7+0.15	ns
t_{Top4}	Output Data Position4 (T=6.25ns ~ 20ns)	4T/7-0.15	4T/7	4T/7+0.15	ns
t_{Top3}	Output Data Position5 (T=6.25ns ~ 20ns)	5T/7-0.15	5T/7	5T/7+0.15	ns
t_{Top2}	Output Data Position6 (T=6.25ns ~ 20ns)	6T/7-0.15	6T/7	6T/7+0.15	ns

*Typ values are at VCC=3.3V, Ta = +25ºC

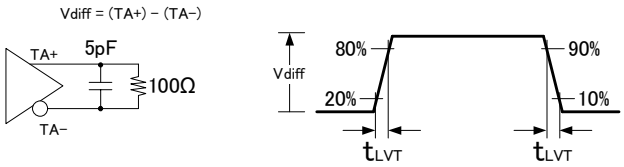


Figure 7. LVDS Output Load and Transmission Time

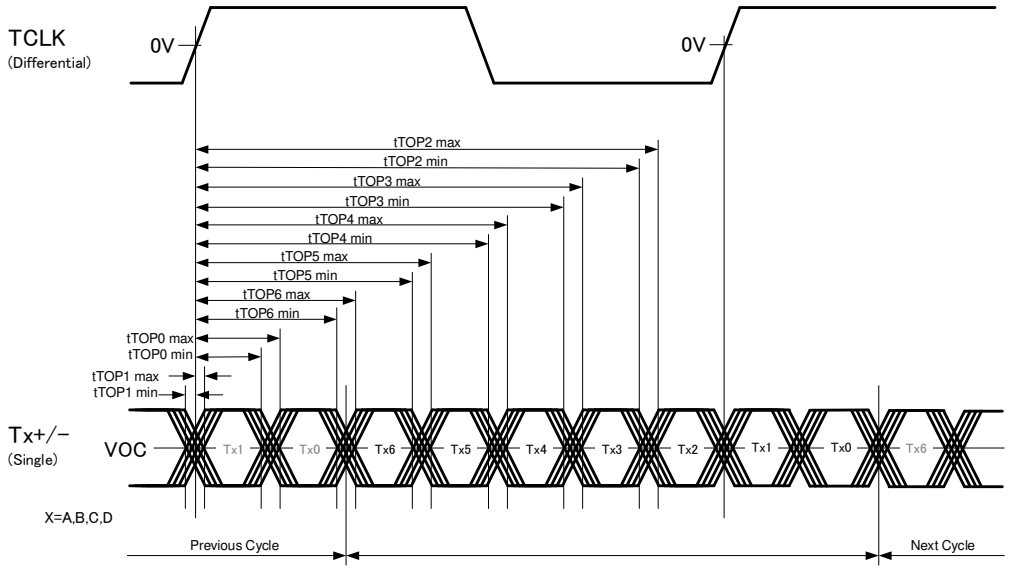


Figure 8. LVDS Output Data Position

Input to Output AC Specifications

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Units
t_{TCD}	CLKIN to TCLK+/- Delay	-	3T	-	ns
t_{TPLL}	Phase Lock Loop Set	-	-	10.0	ms

*Typ values are at VCC=3.3V, Ta = +25ºC

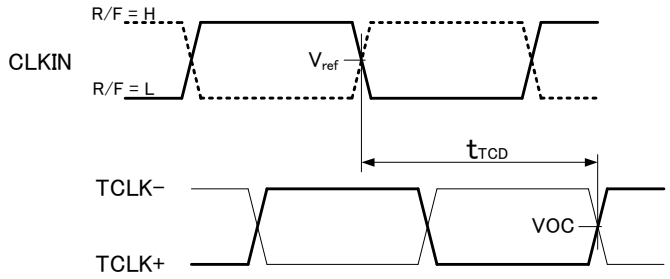


Figure 9. CLKIN to TCLK+/- Delay

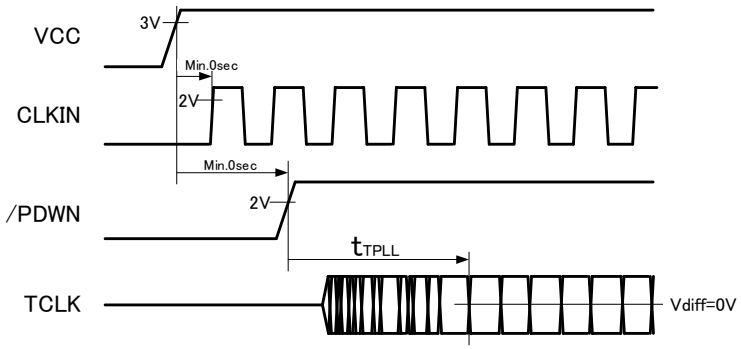
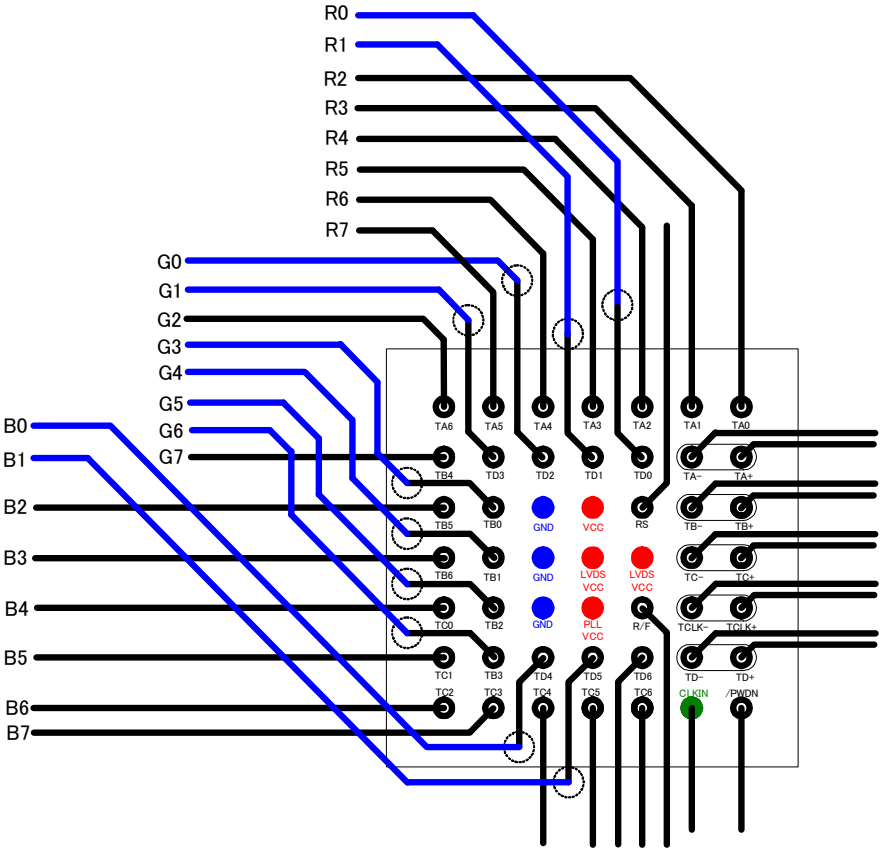


Figure 10. PLL Set Time

Board Layout Example

TOP VIEW

	1	2	3	4	5	6	7	
A	TA6	TA5	TA4	TA3	TA2	TA1	TA0	A
B	TB4	TD3	TD2	TD1	TD0	TA-	TA+	B
C	TB5	TB0	GND	VCC	RS	TB-	TB+	C
D	TB6	TB1	GND	LVDS VCC	LVDS VCC	TC-	TC+	D
E	TC0	TB2	GND	PLL VCC	R/F	TCLK-	TCLK+	E
F	TC1	TB3	TD4	TD5	TD6	TD-	TD+	F
G	TC2	TC3	TC4	TC5	TC6	CLKIN	/PDWN	G
	1	2	3	4	5	6	7	



Note

1) Cable Connection and Disconnection

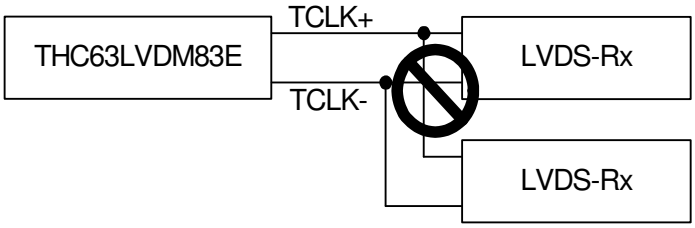
Don't connect and disconnect the LVDS cable, when the power is supplied to the system.

2) GND Connection

Connect the each GND of the PCB which THC63LVDM83E and LVDS-Rx on it. It is better for EMI reduction to place GND cable as close to LVDS cable as possible.

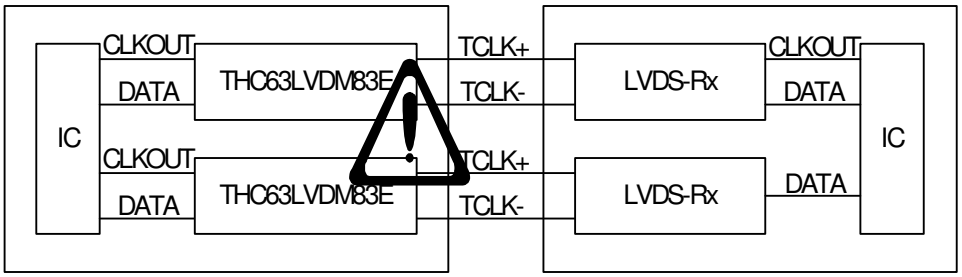
3) Multi Drop Connection

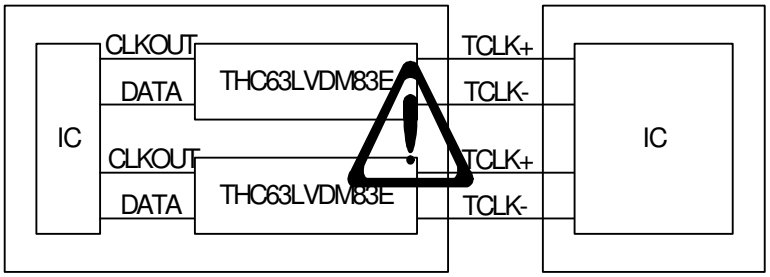
Multi drop connection is not recommended.



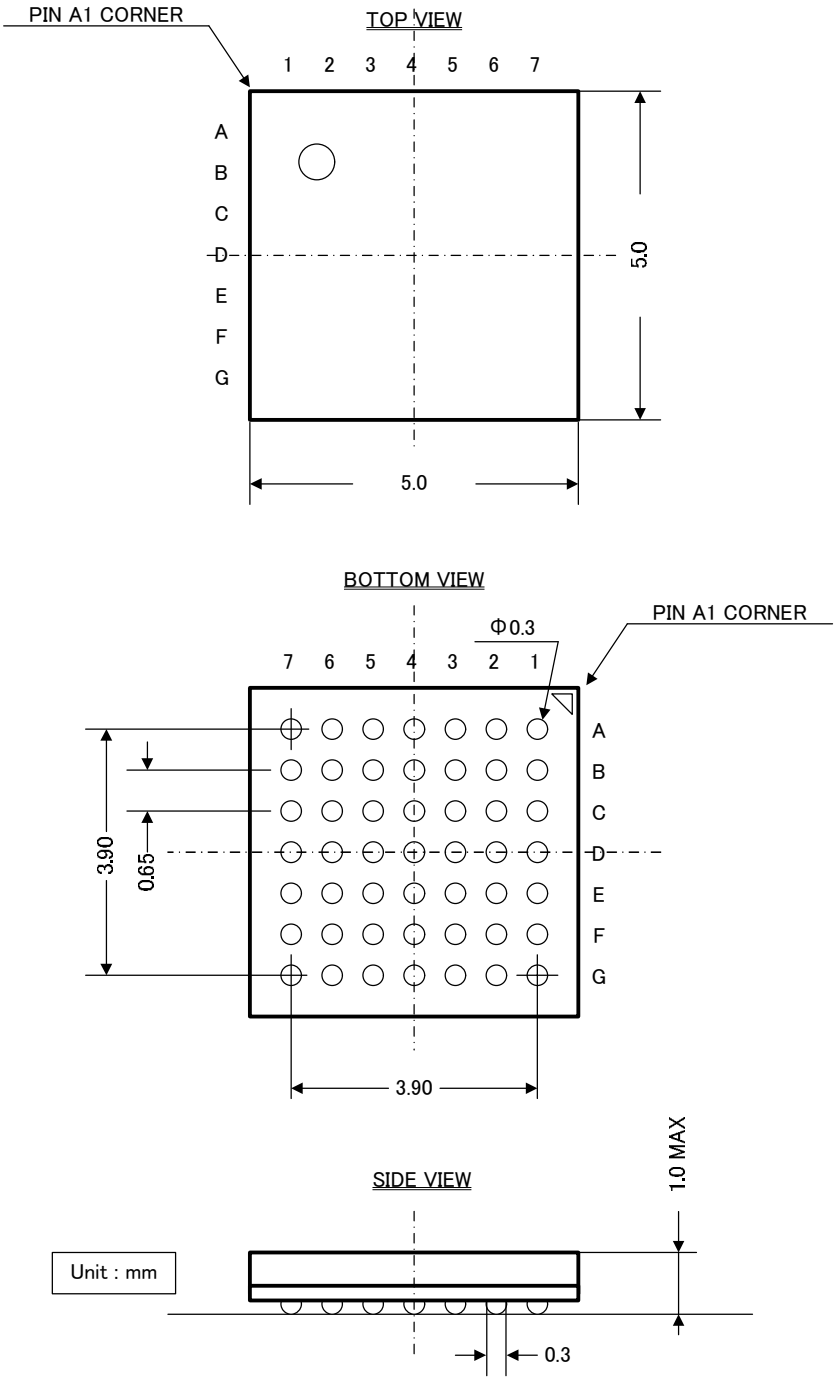
4) Asynchronous use

Asynchronous using such as following systems are not recommended.





Package


PIN A1 CORNER
TOP VIEW
1 2 3 4 5 6 7
A
B
C
D
E
F
G
5.0
5.0
BOTTOM VIEW
Φ0.3
PIN A1 CORNER
7 6 5 4 3 2 1
A
B
C
D
E
F
G
3.90
0.65
3.90
SIDE VIEW
1.0 MAX
Unit : mm
0.3

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1. The product specifications described in this material are subject to change without prior notice.

2. The circuit diagrams described in this material are examples of the application which may not always apply to the customer's design. THine Electronics, Inc. (“THine”) is not responsible for possible errors and omissions in this material. Please note even if errors or omissions should be found in this material, THine may not be able to correct them immediately.

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5. Product Application

5.1 Application of this product is intended for and limited to the following applications: audio-video device, office automation device, communication device, consumer electronics, smartphone, feature phone, and amusement machine device. This product must not be used for applications that require extremely high-reliability/safety such as aerospace device, traffic device, transportation device, nuclear power control device, combustion chamber device, medical device related to critical care, or any kind of safety device.

5.2 This product is not intended to be used as an automotive part, unless the product is specified as a product conforming to the demands and specifications of IATF16949 ("the Specified Product") in this data sheet. THine accepts no liability whatsoever for any product other than the Specified Product for it not conforming to the aforementioned demands and specifications.

5.3 THine accepts liability for demands and specifications of the Specified Product only to the extent that the user and THine have been previously and explicitly agreed to each other.

6. Despite our utmost efforts to improve the quality and reliability of the product, faults will occur with a certain small probability, which is inevitable to a semi-conductor product. Therefore, you are encouraged to have sufficiently redundant or error preventive design applied to the use of the product so as not to have our product cause any social or public damage.

7. Please note that this product is not designed to be radiation-proof.

8. Testing and other quality control techniques are used to this product to the extent THine deems necessary to support warranty for performance of this product. Except where mandated by applicable law or deemed necessary by THine based on the user's request, testing of all functions and performance of the product is not necessarily performed.

9. Customers are asked, if required, to judge by themselves if this product falls under the category of strategic goods under the Foreign Exchange and Foreign Trade Act.

10. The product or peripheral parts may be damaged by a surge in voltage over the absolute maximum ratings or malfunction, if pins of the product are shorted by such as foreign substance. The damages may cause a smoking and ignition. Therefore, you are encouraged to implement safety measures by adding protection devices, such as fuses.

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