NLAS9041

SPDT, 1 Ω R_{ON} Switch

The NLAS9041 is a low R_{ON} SPDT analog switch. This device is designed for low operating voltage, high current switching of speaker output for cell phone applications. It can switch a balanced stereo output. The NLAS9041 can handle a balanced microphone/speaker/ringtone generator in a monophone mode. The device contains a break−before−make (BBM) feature.

Features

- Single Supply Operation:
  1.65 V to 5.5 V V_{CC}
  Function Directly from LiON Battery
- Tiny SC88 6−Pin Pb−Free Package:
  Meets JEDEC MO−220 Specifications
- R_{ON} Typical = 0.8 Ω @ V_{CC} = 4.5 V
- Low Static Power
- This is a Pb−Free Device

Typical Applications

- Cell Phone Speaker/Microphone Switching
- Ringtone−Chip/Amplifier Switching
- Stereo Balanced (Push−Pull) Switching

Important Information

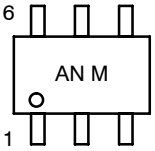
- Ringtone−Chip/Amplifier Switching
- Continuous Current Rating Through each Switch ±300 mA
- Conforms to: JEDEC MO−220, Issue H, Variation VEED−6
- Pin for Pin Compatible with FSA9041

ON Semiconductor®

http://onsemi.com

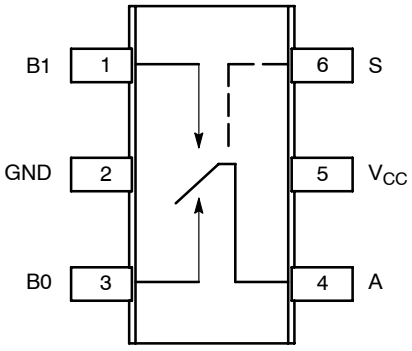
SC−88 (SOT−363)
CASE 419B

MARKING DIAGRAM



AN = Specific Device Code
M = Date Code
G or ▪ = Pb−Free Package

PIN ASSIGNMENTS



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 8 of this data sheet.

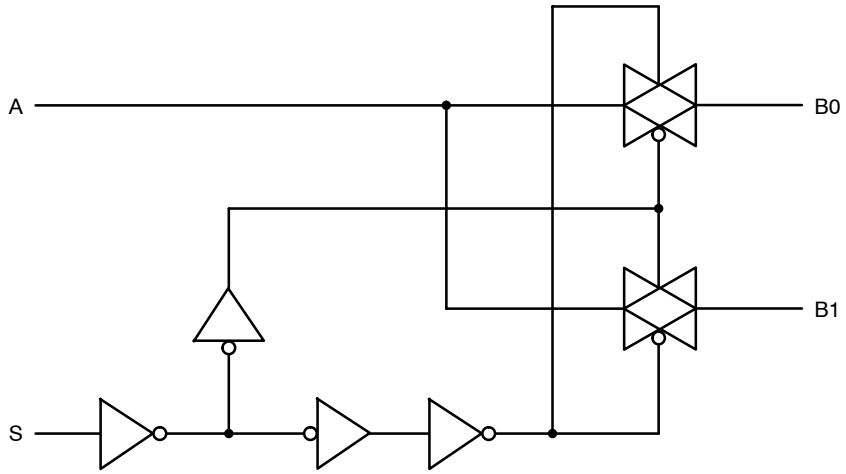


Figure 1. Input Equivalent Circuit

PIN DESCRIPTION

Pin Name	Description
A, B0, B1	Data Ports
S	Control Input

TRUTH TABLE

Control Input	Function
L	B0 Connected to A
H	B1 Connected to A

H = HIGH Logic Level.
L = LOW Logic Level.

MAXIMUM RATINGS

Symbol	Rating	Value	Unit
V_{CC}	Positive DC Supply Voltage	−0.5 to +6.0	V
V_{IS}	Analog Input Voltage (V_{NO}, V_{NC}, or V_{COM})	−0.5 to V_{CC} +0.5	V
V_{IN}	Digital Select Input Voltage	−0.5 to +6.0	V
I_{anl1}	Continuous DC Current from COM to NC/NO	±300	mA
$I_{anl-pk1}$	Peak Current from COM to NC/NO, 10 Duty Cycles (Note 1)	±500	mA
I_{clmp}	Continuous DC Current into COM/NC/NO with respect to V_{CC} or GND	±100	mA

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.
1. Defined as 10% ON, 90% off duty cycle.

RECOMMENDED OPERATING CONDITIONS

Symbol	Rating		Min	Max	Unit
V_{CC}	Positive DC Supply Voltage		1.65	5.5	V
V_{IS}	Analog Input Voltage (A, B0, B1)		0	V_{CC}	V
V_{IN}	Digital Select Input Voltage (S)		0	V_{CC}	V
T_A	Operating Temperature Range		−40	85	°C
t_r, t_f	Input Rise or Fall Time, SELECT	V_{CC} = 3.0 V V_{CC} = 5.5 V		20 10	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} (V)	T_A = +25°C			T_A = −40°C to +85°C		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	HIGH Level Input Voltage		2.7 4.5				2.0 2.4		V
V_{IL}	LOW Level Input Voltage		2.7 4.5					0.6 0.8	V
I_{IN}	Input Leakage Current	0 ≤ V_{IN} ≤ 5.5 V	0−5.5			±0.1		±1	μA
I_{OFF}	OFF State Leakage Current (Note 7)	0 ≤ A, B ≤ V_{CC}	5.5	−2.0		+2.0		±20	nA
I_{ON}	ON State Leakage Current (Note 7)	0 ≤ A, B ≤ V_{CC}	5.5	−4.0		+4.0		±40	nA
R_{ON}	Switch On Resistance (Note 2)	I_O = −100 mA, B_0 or B_1 = 3.5 V	2.7		2.0	4.0		4.3	Ω
		I_O = −100 mA, B_0 or B_1 = 1.5 V	4.5		0.8	1.15		1.3	
I_{CC}	Quiescent Supply Current All Channels ON or OFF	V_{IN} = V_{CC} or GND, I_{OUT} = 0	5.5			0.5		1.0	μA
Analog Signal Range									
ΔR_{ON}	On Resistance Match Between Channels (Notes 2, 3, 4)	I_A = −100 mA, B_0 or B_1 = 1.5 V I_A = −100 mA, B_0 or B_1 = 3.5 V	2.7 4.5		0.15 0.12			 0.15	Ω
R_{flat}	On Resistance Flatness (Notes 2, 3, 5)	I_A = −100 mA, B_0 or B_1 = 0 V, 0.75 V, 1.5 V I_A = −100 mA, B_0 or B_1 = 0 V, 1.0 V, 2.0 V	2.7 4.5		1.4 0.3			 0.4	Ω

2. Measured by the voltage drop between A and B pins at the indicated current through the switch. On Resistance is determined by the lower of the voltages on the two (A or B Ports).
3. Parameter is characterized but not tested in production.
4. DR_{ON} = R_{ON} max − R_{ON} min measured at identical V_{CC}, temperature and voltage levels.
5. Flatness is defined as the difference between the maximum and minimum value of On Resistance over the specified range of conditions.
6. Guaranteed by Design.
7. This parameter is guaranteed by design but not tested. The bus switch contributes no propagation delay other than the RC delay of the On Resistance of the switch and the 50 pF load capacitance, when driven by an ideal voltage source (zero output impedance).

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} (V)	T_A = +25°C			T_A = −40°C to +85°C		Unit	Figure #
				Min	Typ	Max	Min	Max		
t_{PHL} t_{PLH}	Propagation Delay Bus−to−Bus (Note 9)	V_I = OPEN	2.7 4.5			2.0 0.3			ns	3, 4
t_{ON}	Output Enable Time Turn On Time (A to B_n)	B_0 or B_1 = 1.5 V, R_L = 50 Ω, C_L = 35 pF B_0 or B_1 = 3.0 V, R_L = 50 Ω, C_L = 35 pF	2.7 4.5			30 20		35 25	ns	3, 4
t_{OFF}	Output Disable Time Turn Off Time (A Port to B Port)	B_0 or B_1 = 1.5V, R_L = 50 Ω, C_L = 35 pF B_0 or B_1 = 3.0 V, R_L = 50 Ω, C_L = 35 pF	2.7 4.5			20 15		25 20	ns	3, 4
t_{BBM}	Break Before Make Time (Note 8)		2.7 4.5	0.5 0.5			0.5 0.5		ns	2
Q	Charge Injection (Note 8)	C_L = 1.0 nF, V_{GEN} = 0 V R_{GEN} = 0 Ω	2.7 4.5		26 48				pC	6
O_{IRR}	Off Isolation (Note 10)	R_L = 50 Ω f = 1.0 MHz	2.7 – 5.5		−52				dB	5
X_{talk}	Crosstalk	R_L = 50 Ω f = 1.0 MHz	2.7 – 5.5		−57				dB	7
BW	−3 dB Bandwidth	R_L = 50 Ω	2.7 – 5.5		40				MHz	8
THD	Total Harmonic Distortion (Note 8)	R_L = 600 Ω 0.5 V_{P-P} f = 20 Hz to 20 kHz	2.7 – 5.5		0.012				%	9

8. Guaranteed by Design.
9. This parameter is guaranteed by design but not tested. The bus switch contributes no propagation delay other than the RC delay of the On Resistance of the switch and the 50 pF load capacitance, when driven by an ideal voltage source (zero output impedance).
10. Off Isolation = 20 $\log_{10}$ [V_A/V_{Bn}].

CAPACITANCE (Note 11)

Symbol	Parameter	Test Conditions	Typ	Max	Unit	Figure #
C_{IN}	Select Pin Input Capacitance	V_{CC} = 0 V, f = 1 MHz	10		pF	
C_{IO-B}	B Port Off Capacitance	V_{CC} = 4.5 V, f = 1 MHz	25		pF	
C_{IOA-ON}	A Port Capacitance when Switch is Enabled	V_{CC} = 4.5 V, f = 1 MHz	87		pF	

11. T_A = +25°C, f = 1 MHz, Capacitance is characterized but not tested in production.

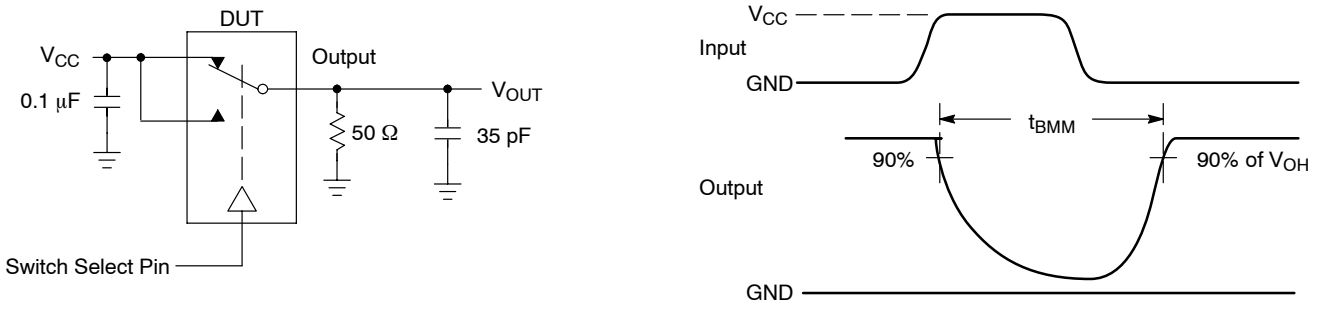


Figure 2. t_{BBM} (Time Break−Before−Make)

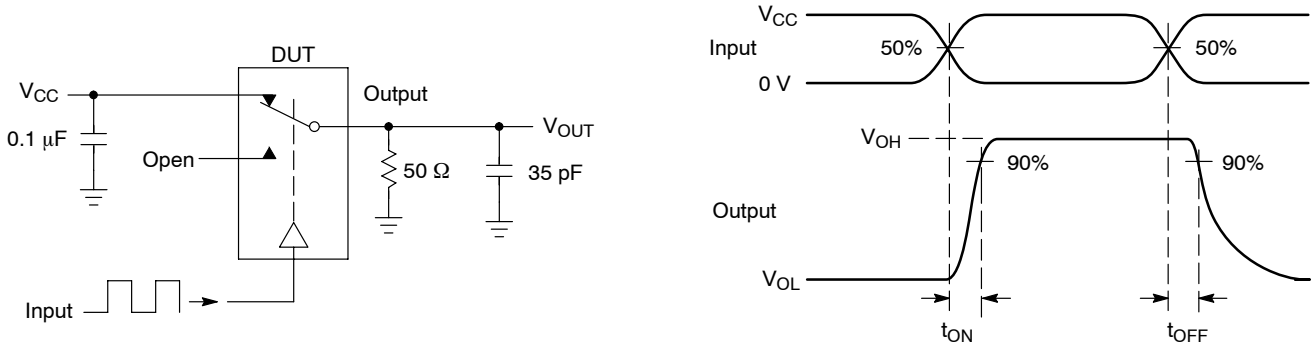


Figure 3. t_{ON}/t_{OFF}

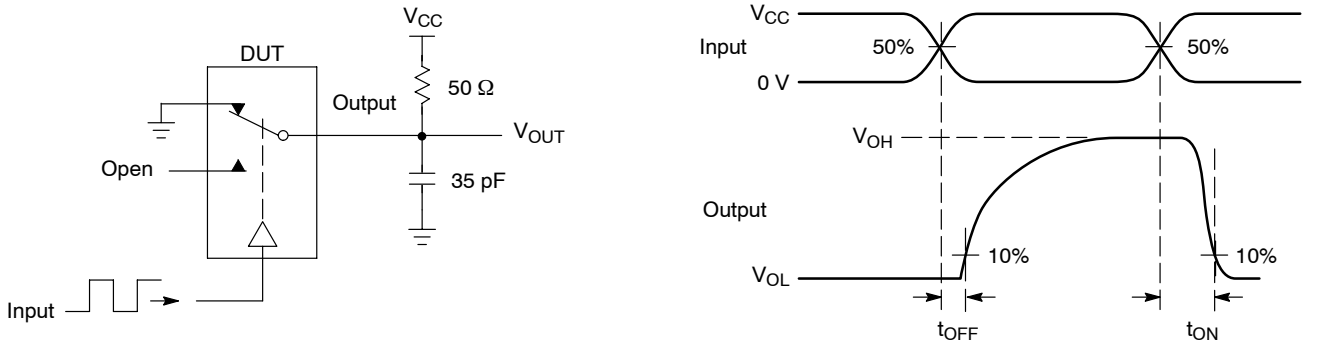
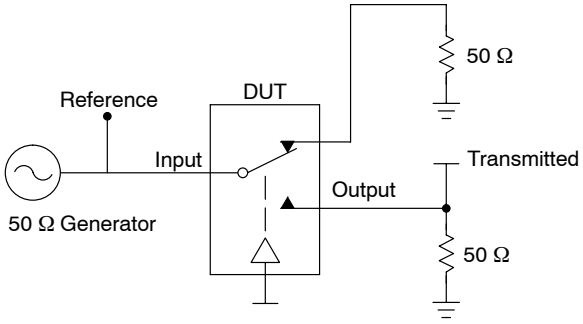


Figure 4. t_{ON}/t_{OFF}



Channel switch control/s test socket is normalized. Off isolation is measured across an off channel. On loss is the bandwidth of an On switch. V_{ISO}, Bandwidth and V_{ONL} are independent of the input signal direction.

V_{ISO} = Off Channel Isolation = 20 Log $\left(\frac{V_{OUT}}{V_{IN}}\right)$ for V_{IN} at 100 kHz

V_{ONL} = On Channel Loss = 20 Log $\left(\frac{V_{OUT}}{V_{IN}}\right)$ for V_{IN} at 100 kHz to 50 MHz

Bandwidth (BW) = the frequency 3 dB below V_{ONL}
V_{CT} = Use V_{ISO} setup and test to all other switch analog input/outputs terminated with 50 Ω

Figure 5. Off Channel Isolation/On Channel Loss (BW)/Crosstalk (On Channel to Off Channel)/V_{ONL}

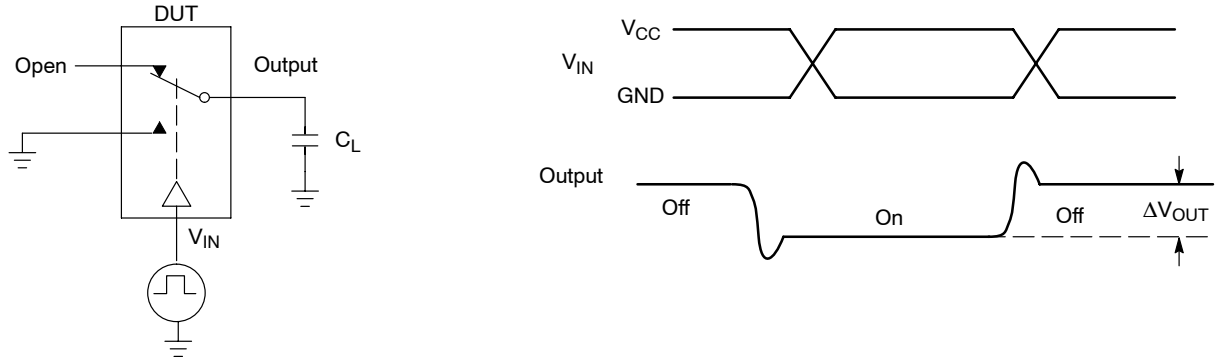


Figure 6. Charge Injection: (Q)

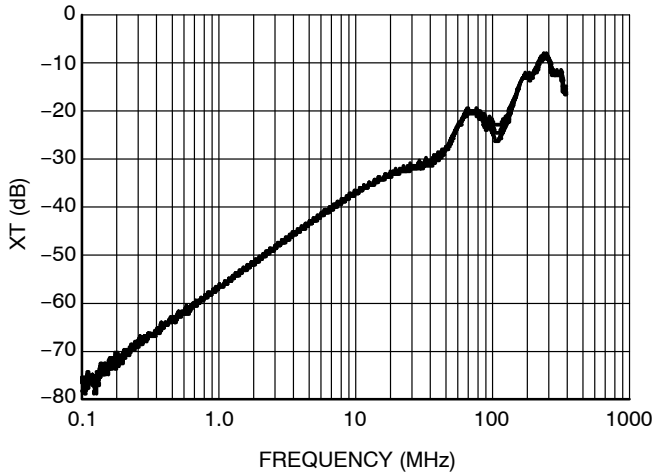


Figure 7. Cross Talk vs. Frequency @ V_{CC} = 4.5 V

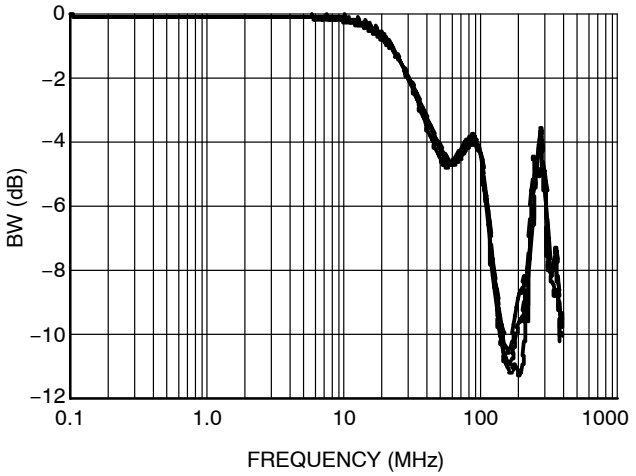


Figure 8. Bandwidth vs. Frequency

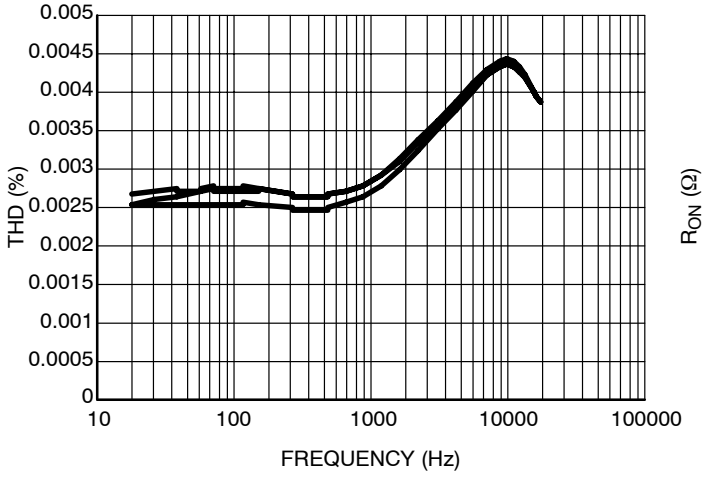


Figure 9. Total Harmonic Distortion

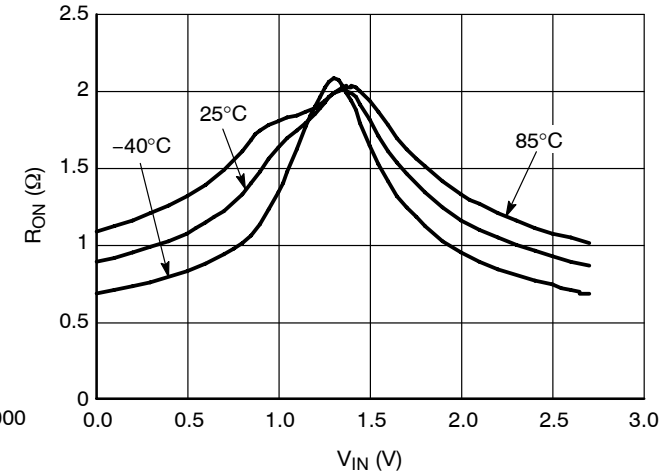


Figure 10. On−Resistance vs. Input Voltage @ V_{CC} = 2.7 V

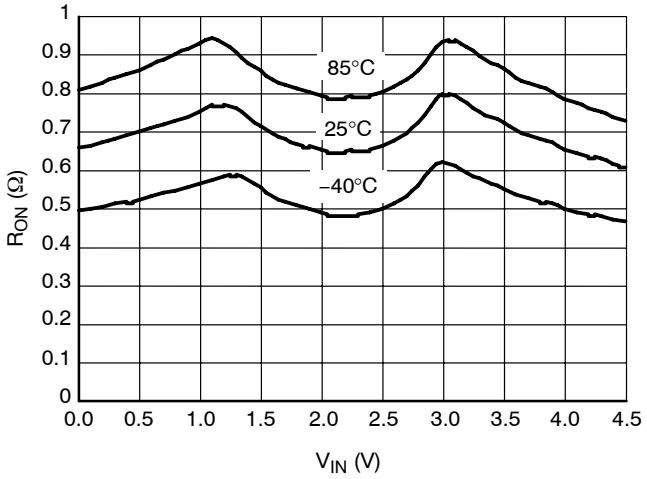


Figure 11. On−Resistance vs. Input Voltage @ V_{CC} = 4.5 V

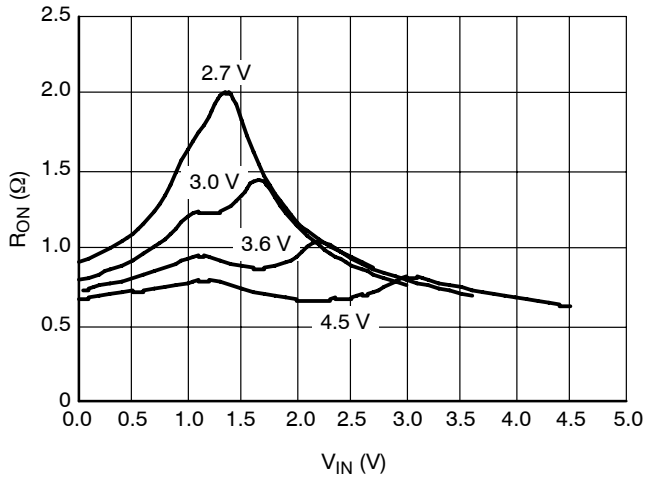


Figure 12. On−Resistance vs. Input Voltage

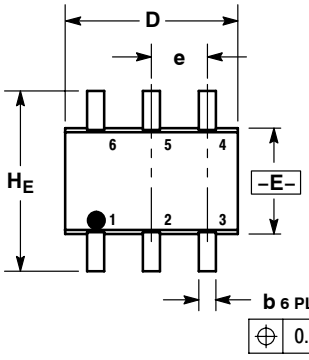
DEVICE ORDERING INFORMATION

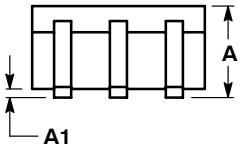
Device Order Number	Device Nomenclature					Package Type	Tape & Reel Size†
	Circuit Indicator	Technology	Device Function	Package Suffix	Tape & Reel Suffix		
NLAS9041DFT2G	NL	AS	9041	DFT	2	SC−88 (Pb−Free)	3000 / Tape & Reel

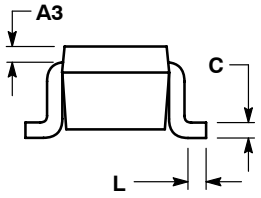
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

SC−88/SC70−6/SOT−363
CASE 419B−02
ISSUE W



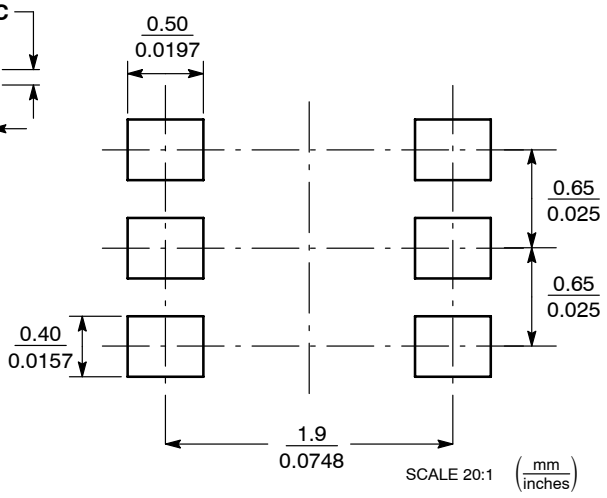




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 419B−01 OBSOLETE, NEW STANDARD 419B−02.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.95	1.10	0.031	0.037	0.043
A1	0.00	0.05	0.10	0.000	0.002	0.004
A3		0.20 REF			0.008 REF	
b	0.10	0.21	0.30	0.004	0.008	0.012
C	0.10	0.14	0.25	0.004	0.005	0.010
D	1.80	2.00	2.20	0.070	0.078	0.086
E	1.15	1.25	1.35	0.045	0.049	0.053
e		0.65 BSC			0.026 BSC	
L	0.10	0.20	0.30	0.004	0.008	0.012
H_E	2.00	2.10	2.20	0.078	0.082	0.086

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

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