ZCU1275 Characterization Board

User Guide

UG1285 (v1.2) September 2, 2020

XILINX

Revision History

The following table shows the revision history for this document.

Section	Revision Summary
09/02/2020 Version 1.2	
Connecting the System Controller User Interface	Revised to specify Interface 1 instead of 2.
07/22/2019 Version 1.1	
Figure 1-2: ZCU1275 Board Features	Updated photo and its table.
Figure 1-15: SuperClock-RF2 Module Features	Updated photo.
11/12/2018 Version 1.0	
Initial Xilinx release.	N/A

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ZCU1275 Board Features and Operation

Introduction

This user guide describes the components, features, and operation of the Xilinx® Zynq® UltraScale+™ RFSoC ZCU1275 characterization kit. The ZCU1275 kit provides the hardware environment for characterizing and evaluating the radio frequency data converter subsystem (RF-ADC/RF-DAC) and high-speed serial transceivers (GTY/PS-GTR) available on the XCZU29DR-2FFVF1760E Zynq UltraScale+ RFSoC. The ZCU1275 schematic, bill of material (BOM), and Allegro board files are in the XTP523 document package on the Zynq UltraScale+ RFSoC ZCU1275 Characterization Kit page.

Electrostatic Discharge Caution

CAUTION! *ESD can damage electronic components when they are improperly handled, and can result in total or intermittent failures. Always follow ESD-prevention procedures when removing and replacing components.*

To prevent ESD damage:

- Use an ESD wrist or ankle strap and ensure that it makes skin contact. Connect the equipment end of the strap to an unpainted metal surface on the chassis.
- Avoid touching the adapter against your clothing. The wrist strap protects components from ESD on the body only.
- Handle the adapter by its bracket or edges only. Avoid touching the printed circuit board or the connectors.
- Put the adapter down only on an antistatic surface such as the bag supplied in your kit.
- If you are returning the adapter to Xilinx Product Support, place it back in its antistatic bag immediately.

Zynq UltraScale+ RFSoC Compatibility

The ZCU1275 board is provided with the XCZU29DR-2FFVF1760E Zynq UltraScale+ RFSoC. There are no other pin compatible devices that come in this package.

ZCU1275 Board Features

- XCZU29DR-2FFVF1760E Zynq UltraScale+ RFSoC
- Samtec Bulls Eye® cable access to all 16 radio frequency analog-to-digital converter (RF-ADC) channels
- Samtec Bulls Eye cable access to all 16 radio frequency digital-to-analog converter (RF-DAC) channels
- Samtec Bulls Eye cable access to all 16 GTY transceivers
- Samtec Bulls Eye cable access to all four PS-GTR transceivers
- Onboard power supplies for all necessary voltages
- Connectors for external power supplies
- SMA connectors for probing RF-ADC/RF-DAC power rails, GTY/PS-GTR power rails, and V_{CCINT}/V_{CCO_HP}/V_{CCO_HD} power rails
- Embedded USB-to-JTAG programming port
- JTAG programming header
- Programmable logic (PL) JTAG connector connected to HPIO bank 66
- System Controller (Zynq®-7000 SoC XC7Z010-CLG225)
- One analog power module supporting RF data converter power requirements
- One power module to support GTY transceiver power requirements
- One power module to support PS-GTR transceiver power requirements
- 300 MHz LVDS oscillator connected to HPIO global clock (GC) pins on bank 66
- 33.3333333 MHz LVCMOS oscillator connected to processing system (PS) bank 503 PS_REF_CLK pin
- Two pairs of SMA connectors connected to HPIO global clock (GC) pins on bank 66
- SuperClock-RF2 Module (HW-CLK-103) supporting RF data converter clock requirements
- SuperClock-2 Module (HW-CLK-101) supporting GTY/PS-GTR reference clock requirements

- General purpose DIP switches, LEDs, pushbuttons, and test I/O
- One VITA 57.1 FPGA mezzanine card (FMC) high pin count (HPC) connector
- One VITA 57.1 FPGA mezzanine card low pin count (LPC) connector
- USB-to-UART bridge connected to PL, PS, and System Controller
- Inter IC (I2C) interface
- 4x 4 Gb DDR3 SDRAM PS memory
- 1 Gb Quad SPI flash PS memory
- PMBus connectivity to the board's digital power supplies

The ZCU1275 block diagram is shown in Figure 1-1.

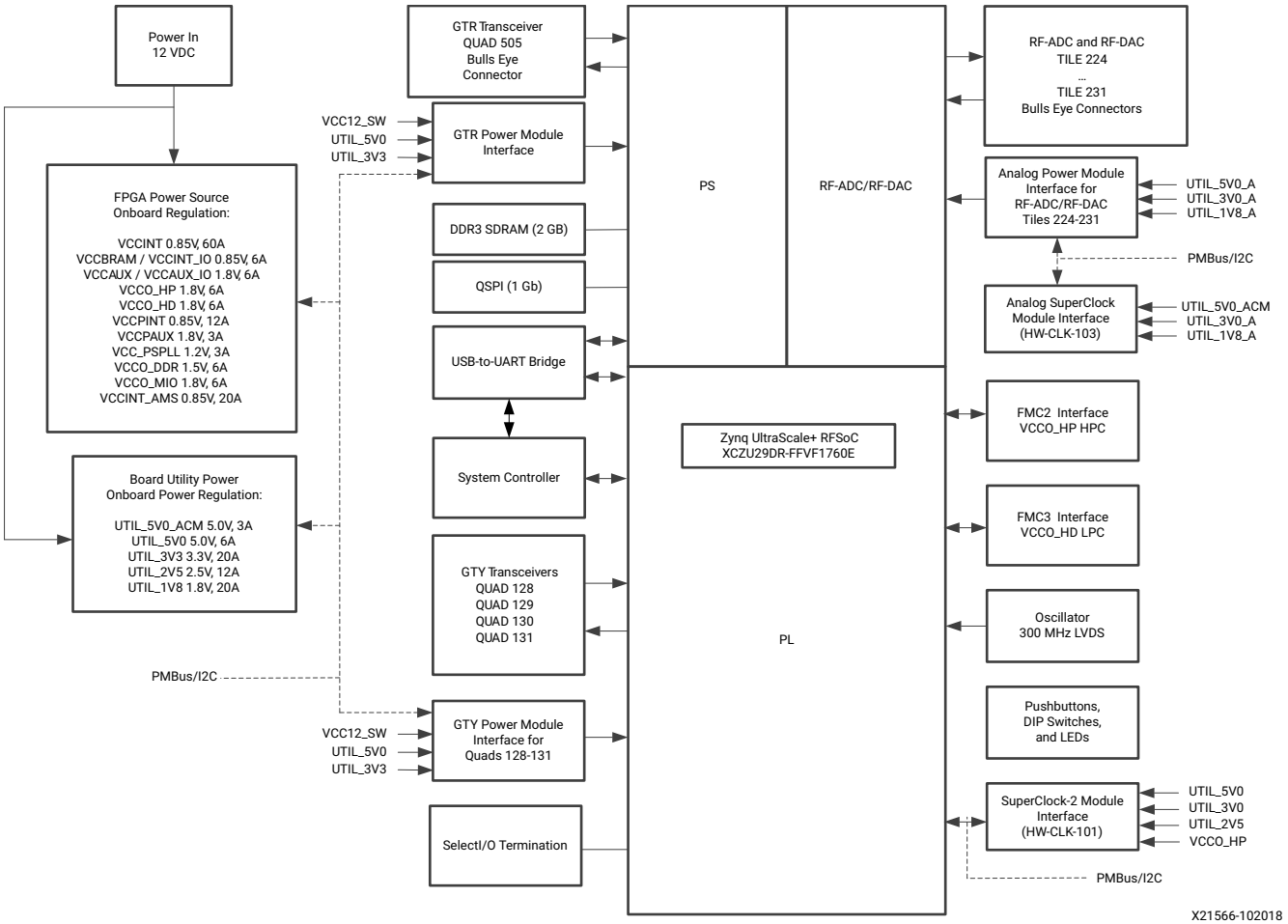

Figure 1-1: **ZCU1275 Board Block Diagram**

Detailed Description

Figure 1-2 shows the ZCU1275 board described in this user guide. Each numbered feature referenced in Figure 1-2 is described in Table 1-1 and the sections that follow.

CAUTION! *Do not remove the rubber feet from the board. The feet provide clearance to prevent short circuits on the back side of the board.*

IMPORTANT: *Figure 1-2 is for reference only and might not reflect the current revision of the board.*

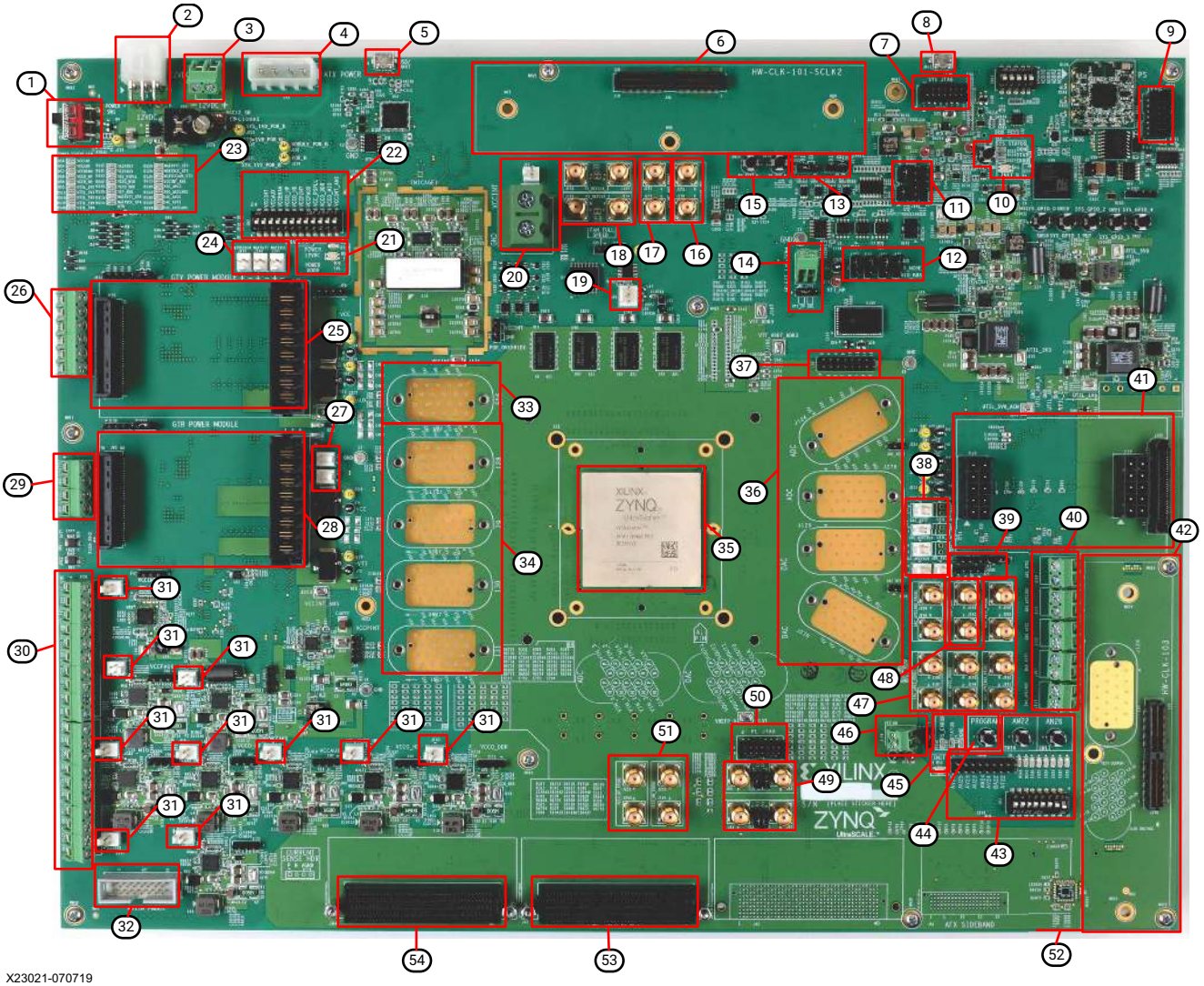

Figure 1-2: **ZCU1275 Board Features**

Table 1-1: **ZCU1275 Board Features and Operation**

Figure 1-2 Callout	Reference Designator	Feature Description
1	SW1	Power Switch
2	J28	12V Mini-Fit connector (12V Input Power)
3	J27	12V external power supply connector (12V Input Power, Using External Power Sources)
4	J73	ATX power connector (12V Input Power)
5	J1	USB to Quad-UART Bridge (Micro-B receptacle)
6	J36	SuperClock-2 Module connector (HW-CLK-101-SCLK2)
7	J3	System Controller JTAG connector
8	J69	USB-to-JTAG connector (Micro-B receptacle) (RFSoC Configuration)
9	J2	Xilinx Platform USB JTAG connector (alternate access for programming cables) (RFSoC Configuration)
10	SW4, DS12, DS16, DS27, DS1	System Controller status LEDs and POR pushbutton (System Controller Reset, System Controller Status LEDs)
11	J4, J145, J154, J8	Serial transceiver power module PMBus connectors and isolation selection headers (Monitoring Voltage and Current)
12	J163, J164, J166, J165	Boot Mode Selection Headers
13	J121, J125	I2C bus master selection headers (I2C Bus Management)
14	J160, J275	VTT_HP external connector and selection header
15	SW15, SW14	PS_POR_B Pushbutton and PS_SRST_B Pushbutton
16	J250, J251	VCCINT power probe SMA
17	J276, J277	VCCINT_AMS power probe SMA
18	J158, J159, J156, J194	PS-GTR ref clock SMAs (Serial Transceivers and Reference Clocks)
19	J99	Active Heat Sink and Power Connector
20	J181	VCCINT external power connector and voltage sense header
21	DS18, DS2	12V and Power Good LEDs (Power Switch)
22	SW2	Power regulation inhibitor switch for onboard regulators (Using External Power Sources)
23	DS4–DS11, DS13–DS15, DS28–DS38, DS42–DS45, DS49	Status LEDS for RFSoC logic, processor, transceiver, data converter, and utility power
24	J149, J148, J147	GTY voltage sense headers
25	J174, J155	GTY power module connector (Serial Transceiver Power Modules)
26	J150	GTY external power supply connector
27	J63, J62	PS-GTR voltage sense headers

Table 1-1: **ZCU1275 Board Features and Operation *(Cont'd)***

Figure 1-2 Callout	Reference Designator	Feature Description
28	J138, J93	PS-GTR power module connector (Serial Transceiver Power Modules)
29	J67	PS-GTR external power supply connector
30	J151, J96	RFSoC logic and processor external power supply connectors
31	J146, J144, J143, J142, J64, J23, J19, J18, J177	RFSoC logic and processor voltage sense headers
32	J21	PMBus connector (Monitoring Voltage and Current)
33	J39	PS-GTR transceiver connector pad, bank 505 (Serial Transceivers and Reference Clocks)
34	J117, J118, J280, J281	GTY transceiver connector pads Q128, Q129, Q130, and Q131
35	U1	XCZU29DR-2FFVF1760E, Zynq UltraScale+ RFSoC
36	J124, J278, J129, J279	RF-ADC and RF-DAC Bulls Eye connector pads, tiles 224–231 (RF Data Converters and Sampling Clocks)
37	J20	RF-ADC VCM connector
38	J75, J76, J78, J81, J79	RF-ADC and RF-DAC voltage sense headers
39	J46, J43, J60, J25	RF-ADC and RF-DAC PMBus connector and selection headers (Monitoring Voltage and Current)
40	J114, J115, J116, J107, J113	RF-ADC and RF-DAC external power supply connectors
41	J131, J119, J120	Analog Power Module connector
42	J170	SuperClock-RF2 Module connector (HW-CLK-103)
43	SW16, SW17, J95, SW3, DS22–DS26, DS46–DS48	User configurable I/O header, DIP switch, LEDs, and pushbuttons (User LEDs, User DIP Switches and I/O Header)
44	SW7	RFSoC PROGRAM Pushbutton
45	DS40, DS39, DS17, DS3	RFSoC DONE LED, INIT LED, STATUS LED, and ERROR LED
46	J106, J216	VTT_HP external connector and selection header
47	J190, J189, J188, J187, J192, J191, J257, J256, J162, J161	Power probe SMAs for DAC_AVCC, DAC_AVTT, DAC_AVCCAUX, ADC_AVCC, and ADC_AVCCAUX
48	J243, J242	RF-DAC SYSREF SMA
49	J84, J85, J83, J86	SMA connectors to differential GC pins on RFSoC (Differential SMA Pin Inputs)
50	J5	PL JTAG connector tied to RFSoC I/O pins
51	J254, J255, J253, J252	Power probe SMAs for VCCO_HP and VCCO_HD
52	J287	RFSoC SD Card slot (bottom side of board)
53	JA3	FMC2 HPC connector tied to VCCO_HP banks (FPGA Mezzanine Card Interface, FMC Tab)
54	JA4	FMC3 LPC connector tied to VCCO_HD banks (FPGA Mezzanine Card Interface, FMC Tab)

Power Management

12V Input Power

The ZCU1275 board receives 12V main power through J28 (callout 2, Figure 1-2) using the 12V AC adapter included with the ZCU1275 characterization kit. J28 is a 6-pin (2 x 3), right angle, Mini-Fit connector.

CAUTION! *When supplying 12V through J28, use only the power supply provided for use with this board (Xilinx part number 3800033).*

CAUTION! *Do NOT use a 6-pin, PC ATX power supply connector with J28. The pinout of the 6-pin, PC ATX connector is not compatible with J28 and the board will be damaged if an attempt is made to power it from a PC ATX power supply connector.*

12V power can also be provided through:

- Connector J73 (callout 4, Figure 1-2) which accepts an ATX hard drive 4-pin power plug
- Connector J27 (callout 3, Figure 1-2) which can be connected to a bench-top power supply

CAUTION! *Because connector J73 provides no reverse polarity protection, use a power supply with a current limit set at 6A maximum.*

CAUTION! *Do NOT apply 12V power to more than a single input source. For example, do not apply power to J73 and J27 at the same time.*

CAUTION! *If J73 or J27 is used to supply the 12V input power, be careful that board power consumption does not exceed 75W (this includes the RFSoC).*

Power Switch

The ZCU1275 board main power is turned on or off using switch SW1 (callout 1, Figure 1-2). When the switch is in the ON position, power is applied to the board and the power good LED DS18 illuminates green (callout 21, Figure 1-2).

Onboard Power Regulation

Figure 1-3 shows the onboard power supply architecture.

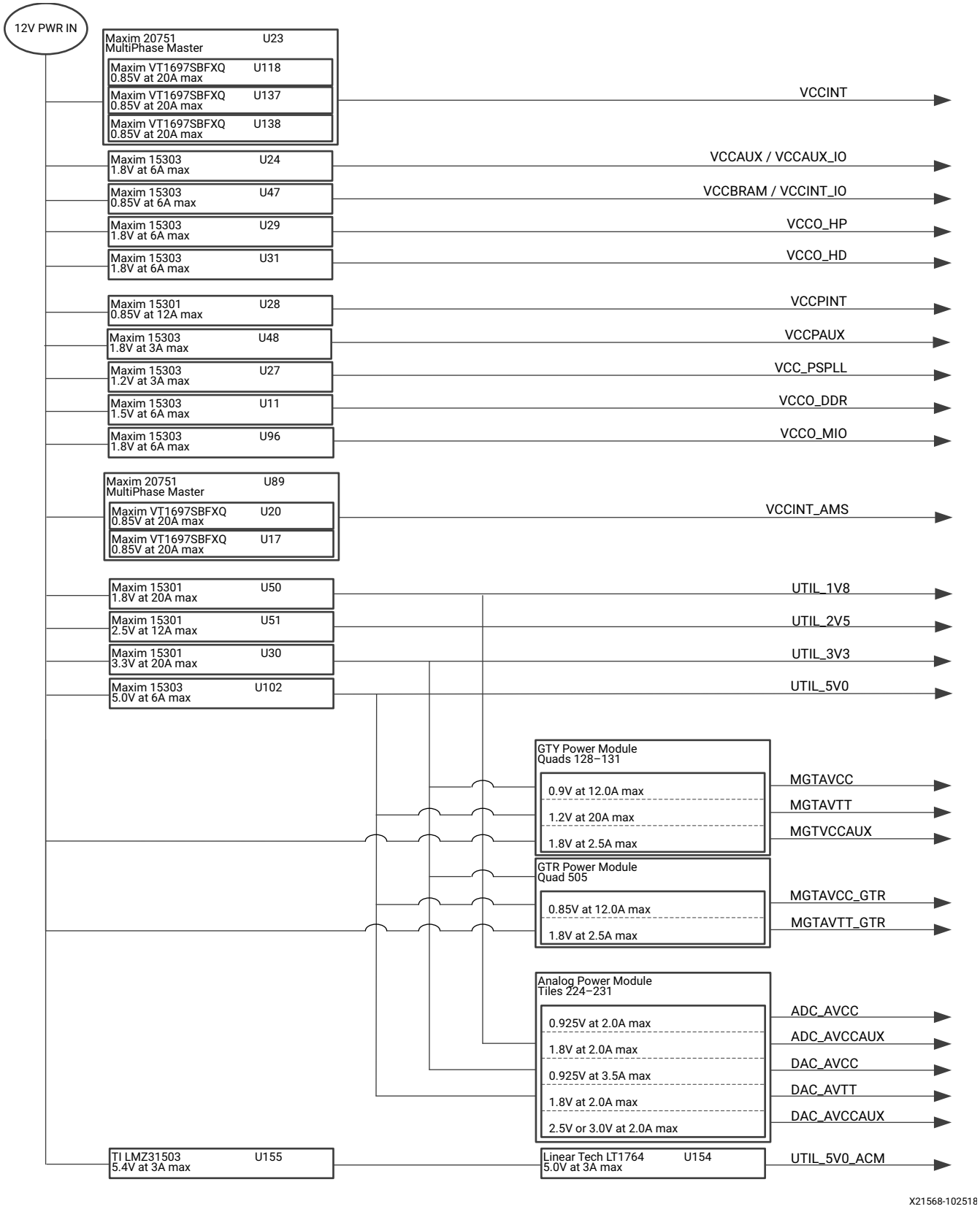

Figure 1-3: **ZCU1275 Board Power Supply Block Diagram**

The ZCU1275 board uses power regulators and PMBus-compliant pulse width modulation (PWM) digital controllers from Maxim Integrated to supply the RFSoC logic and utility voltages listed in Table 1-2. The board can also be configured to use an external bench power supply for each voltage. See Using External Power Sources.

The output voltages of the controllers in Table 1-2 can be reprogrammed using the Maxim InTune Digital PowerTool [Ref 1].

Note: The MAX20751EKX device has limited nonvolatile memory reprogramming saves (4 counts).

CAUTION! *Be extremely careful when attempting to modify any of the onboard regulators, because an incorrectly programmed regulator can damage onboard components.*

Table 1-2: **Onboard Power System Devices**

Device Part Number	Reference Designator(s)	Description	Power Rail Net Name	Voltage
RFSoC Logic				
Maxim MAX20751EKX (1)	U23	Multiphase master with PMBus interface controller (60A three phases at 20A/phase)	VCCINT	0.85V
Maxim MAX15303	U24	InTune digital point of load (PoL) controller, 6A	VCCAUX / VCCAUX_IO	1.8V
Maxim MAX15303	U47	InTune digital point of load (PoL) controller, 6A	VCCBRAM / VCCINT_IO	0.85V
Maxim MAX15303	U29	InTune digital point of load (PoL) controller, 6A	VCCO_HP	1.8V
Maxim MAX15303	U31	InTune digital point of load (PoL) controller, 6A	VCCO_HD	1.8V
Processor				
Maxim MAX15301	U28	InTune digital point of load (PoL) controller, 12A	VCCPINT	0.85V
Maxim MAX15303	U48	InTune digital point of load (PoL) controller, 3A	VCCPAUX	1.8V
Maxim MAX15303	U27	InTune digital point of load (PoL) controller, 3A	VCC_PSPLL	1.2V
Maxim MAX15303	U11	InTune digital point of load (PoL) controller, 6A	VCCO_DDR	1.5V
Maxim MAX15303	U96	InTune digital point of load (PoL) controller, 6A	VCCO_MIO	1.8V
RF Data Converters				
Maxim MAX20751EKX (1)	U89	Multiphase master with PMBus interface controller (40A two phases at 20A/phase)	VCCINT_AMS	0.85V
INA226	U60	Current shunt and power monitor with I2C interface	ADC_AVCC	0.925V

Table 1-2: **Onboard Power System Devices *(Cont'd)***

Device Part Number	Reference Designator(s)	Description	Power Rail Net Name	Voltage
INA226	U61	Current shunt and power monitor with I2C interface	ADC_AVCCAUX	1.8V
INA226	U63	Current shunt and power monitor with I2C interface	DAC_AVCC	0.925V
INA226	U64	Current shunt and power monitor with I2C interface	DAC_AVTT	1.8V
INA226	U65	Current shunt and power monitor with I2C interface	DAC_AVCCAUX	2.5V or 3.0V
GTY Transceivers				
INA226	U141	Current shunt and power monitor with I2C interface	MGTAVCC	0.9V
INA226	U142	Current shunt and power monitor with I2C interface	MGTAVTT	1.2V
INA226	U143	Current shunt and power monitor with I2C interface	MGTVCCAUX	1.8V
PS-GTR Transceivers				
INA226	U99	Current shunt and power monitor with I2C interface	MGTAVCC_GTR	0.85V
INA226	U97	Current shunt and power monitor with I2C interface	MGTAVTT_GTR	1.8V
Utility				
Maxim MAX15301	U50	InTune digital point of load (PoL) controller, 20A	UTIL_1V8	1.8V
Maxim MAX15301	U51	InTune digital point of load (PoL) controller, 12A	UTIL_2V5	2.5V
Maxim MAX15301	U30	InTune digital point of load (PoL) controller, 20A	UTIL_3V3	3.3V
Maxim MAX15301	U102	InTune digital point of load (PoL) controller, 12A	UTIL_5V0	5.0V
LMZ31503	U155	DC/DC converter, 3A	UTIL_5V4	5.4V
LT1764	U154	Fixed LDO regulator	UTIL_5V0_ACM	5.0V
System Controller				
Maxim MAX15053	U13	Fixed LDO regulator	SYS_1V0	1.0V
Maxim MAX15027	U25	Fixed LDO regulator	VCC_1V2	1.2V
Maxim MAX15027	U33	Fixed LDO regulator	VCC_1V8	1.8V

Notes:

1. The MAX20751EKX device has limited nonvolatile memory reprogramming saves (4 counts).

Using External Power Sources

Each voltage rail for the RFSoC logic, multi-gigabit transceivers (MGTs), and RF data converters has an associated Euro-Mag spring-clamp terminal block (callout 3, 14, 20, 26, 29, 30, 40, and 46, Figure 1-2), which can be used to provide power from an external source (Table 1-3).

CAUTION! *Do NOT apply power to any of the RFSoC logic external power supply connectors without first disabling the associated regulator or regulators. Failing to disable the regulator can damage the board.*

Each onboard RFSoC logic regulator can be disabled using its respective power regulation inhibit DIP switch (callout 22, Figure 1-2). A regulator is enabled when the power regulation inhibitor switch is set to the ENABLED position. Table 1-3 shows a list of external power connectors for the different power rails.

Table 1-3: **RFSoC Logic and Serial Transceiver Rails**

	Power Rail Net Name	External Supply Connector(s)	Remote Sense Header
RFSoC logic and processor	VCCINT	J181	J22
	VCCBRAM	J96	J74
	VCCAUX		J23
	VCCO_HP		J19
	VCCO_HD		J18
	VCCPINT		J177
	VCCPAUX	J151	J146
	VCC_PSPLL		J144
	VCCO_DDR		J143
	VCCO_MIO		J142
	VCCINT_AMS		J64
GTY transceivers	MGTAVCC	J150	J147
	MGTAVTT		J148
	MGTVCCAUX		J149
PS-GTR transceivers	MGTAVCC_GTR	J67	J62
	MGTAVTT_GTR		J63

Table 1-3: **RFSoC Logic and Serial Transceiver Rails *(Cont'd)***

	Power Rail Net Name	External Supply Connector(s)	Remote Sense Header
RF data converters	ADC_AVCC	J114	J79
	ADC_AVCCAUX	J115	J81
	DAC_AVCC	J116	J75
	DAC_AVTT	J107	J76
	DAC_AVCCAUX	J113	J78

Notes:

1. The serial transceiver or analog power module must be removed before providing external power to any of the transceiver or data converter rails (see Serial Transceiver Power Modules).

Monitoring Voltage and Current

Voltage and current monitoring and control for the Maxim power system is available through either the ZCU1275 System Controller or via the Maxim PowerTool software GUI.

The ZCU1275 System Controller is the simplest and most convenient way to monitor the voltage and current values for the power rails listed in Table 1-2. For details on how to use this built-in feature, see Power Tab in Appendix D.

The ZCU1275 board includes these PMBus connectors:

- J21 (callout 32, Figure 1-2), for use with the Maxim USB-to-PMBus interface dongle (Maxim part number MAXPOWERTOOL002) and the Maxim PowerTool GUI [Ref 1].
- J4 and J145 (callout 11, Figure 1-2) are used to connect to the serial transceiver power module's PMBus. The pinouts for J4 and J145 are shown in Figure 1-4.
- J25 (callout 39, Figure 1-2) is used to connect to the analog power module PMBus. The pinout for J25 is shown in Figure 1-4.

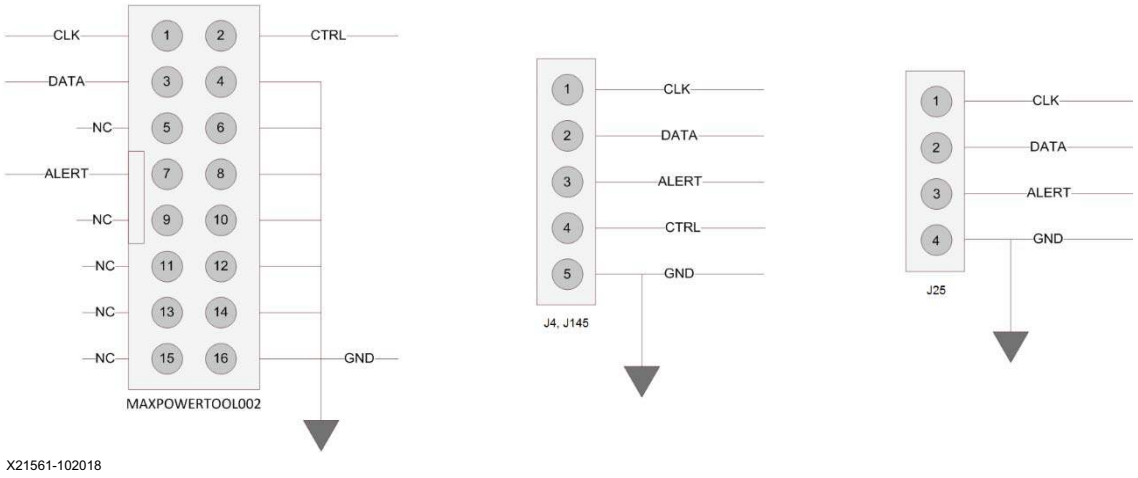

Figure 1-4: **PMBus Connector Pinouts**

The onboard Maxim power controllers by default are isolated from the serial transceiver power module's PMBus. However, the two interfaces can be linked by removing the shunt on J8 or J154 (serial transceiver PMBus isolation). This configuration is required when using Maxim PowerTool to monitor and control both the RFSoC power rails and the serial transceiver power rails using the Maxim InTune Digital PowerTool GUI.

Analog Power Module

There is one analog power module interface for connecting an analog power module (callout 41, Figure 1-2). The analog power module supplies power to the ADC_AVCC, ADC_AVCCAUX, DAC_AVCC, DAC_AVTT, and DAC_AVCCAUX rails, which power the RFSoC RF data converters. The analog power module connects to J131, J119, and J120. Two analog power modules are provided with the ZCU1275 board for evaluation—one made by Intersil, part

number ISL8024DEMO2Z (Figure 1-5) and one made by MPS, part number EVREF0102A (Figure 1-6).

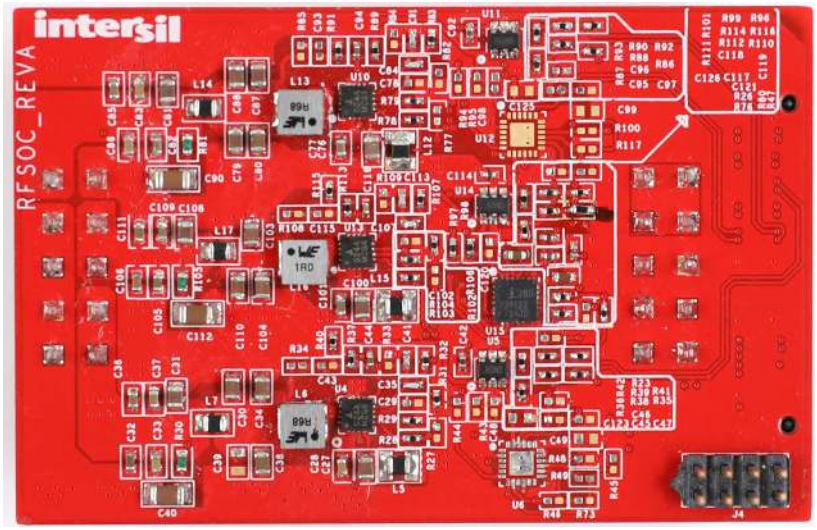

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Figure 1-5: **Intersil Analog Power Module**

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Figure 1-6: **MPS Analog Power Module**

Table 1-4 lists the nominal voltage values for the ADC_AVCC, ADC_AVCCAUX, DAC_AVCC, DAC_AVTT, and DAC_AVCCAUX power rails. It also lists the maximum current rating for each rail supplied by the analog power modules included with the ZCU1275 kit.

Table 1-4: **Analog Power Module**

Analog Rail Net Name	Nominal Voltage (V)	Maximum Current Rating (A)
ADC_AVCC	0.925	2.00
ADC_AVCCAUX	1.8	2.00
DAC_AVCC	0.925	3.5
DAC_AVCCAUX	1.8	2.00
DAC_AVTT	2.5 or 3.0	2.00

The analog power rails can also be supplied externally. The external supply connectors are listed in Table 1-3.

CAUTION! *The analog power module MUST be removed when providing external power to the RF data converter rails.*

Information about the analog power modules included with the ZCU1275 characterization kit is available from the vendor websites [Ref 3] [Ref 2].

Serial Transceiver Power Modules

There is one GTY transceiver power module interface (callout 25, Figure 1-2). The GTY transceiver power module supplies the MGTAVCC, MGTAVTT, and MGTVCCAUX power rails, which connect to the RFSoC GTY transceivers. In the ZCU1275 kit, there is one GTY transceiver power module from Maxim Integrated provided for evaluation, part number MAXREFDES87#. The GTY transceiver power module is labeled GTY and connects to J174 and J155.

There is one PS-GTR transceiver power module interface (callout 28, Figure 1-2). The PS-GTR transceiver power module supplies the MGTAVCC_GTR and MGTAVTT_GTR power rails, which connect the RFSoC PS-GTR transceivers. In the ZCU1275 kit, there is one PS-GTR transceiver power module from Maxim Integrated provided for evaluation, part number MAXREFDES87#. The PS-GTR power module is labeled PS-GTR and connects to J138 and J93.

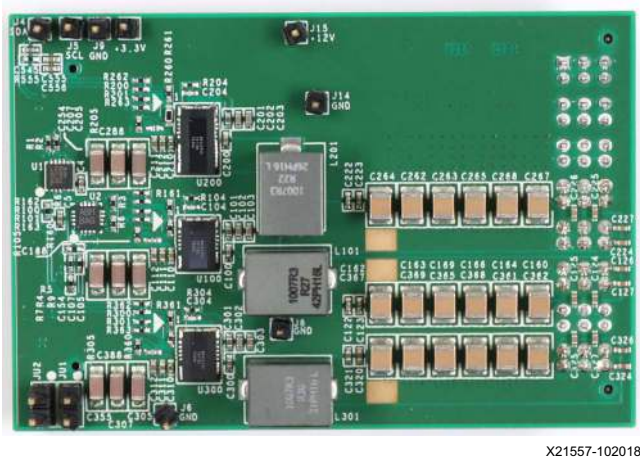

Figure 1-7: **Maxim Integrated Serial Transceiver Power Module**

Table 1-5 lists the nominal voltage values for the MGTAVCC, MGTAVTT, MGTVCCAUX, MGTAVCC_GTR, and MGTAVTT_GTR power rails. It also lists the maximum current rating for each rail supplied by serial transceiver modules included with the ZCU1275 board.

Table 1-5: **Serial Transceiver Power Modules**

Serial Transceiver Rail Net Name	Nominal Voltage (V)	Maximum Current Rating (A)
MGTAVCC	0.9	12
MGTAVTT	1.2	20
MGTVCCAUX	1.8	2.5
MGTAVCC_GTR	0.85	12
MGTAVTT_GTR	1.8	2.5

The serial transceiver power rails can also be supplied externally. The external supply connectors are listed in Table 1-3.

CAUTION! *The serial transceiver power module MUST be removed when providing external power to the GTY or PS-GTR transceiver rails.*

Note: For information about the serial transceiver power modules, contact Maxim technical support and ask about the MAXREFDES87#.

Zynq UltraScale+ RFSoC

The ZCU1275 board is populated with the XCZU29DR-2FFVF1760E Zynq UltraScale+ RFSoC at U1 (callout 35, Figure 1-2). For further information on Zynq UltraScale+ RFSoCs, see *UltraScale Architecture and Product Data Sheet: Overview* (DS890) [Ref 4].

RFSoC Configuration

The RFSoC is configured using one of the following options:

- Digilent embedded USB JTAG connector (callout 8, Figure 1-2)
- Xilinx Platform Cable USB II JTAG cable connector (callout 9, Figure 1-2)

The ZCU1275 board comes with an embedded USB-to-JTAG configuration module (Digilent, J69) which allows a host computer to access the board JTAG chain using a Standard A to Micro-B USB cable. Alternately, a JTAG connector (J2) is available to provide access to the JTAG chain using the Xilinx Platform Cable USB II or compatible configuration cable.

The JTAG chain of the board is illustrated in Figure 1-8. By default, only the RFSoC is in the chain. Installing a shunt at J6 adds the FMC interfaces to the chain.

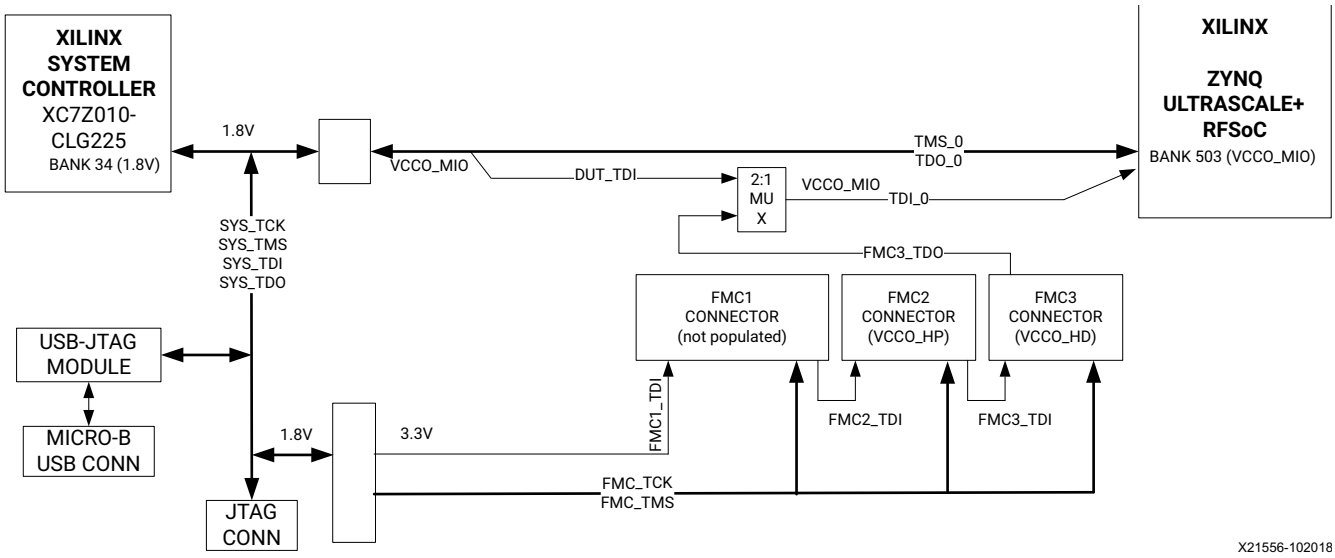

Figure 1-8: **JTAG Chain**

PROGRAM Pushbutton

Pressing the PROGRAM pushbutton SW7 (callout 44, Figure 1-2) asserts the active-Low program pin of the RFSoC.

DONE LED

The DONE LED DS17 (callout 45, Figure 1-2) indicates the state of the DONE pin of the RFSoC. When the DONE pin is High, DS17 lights up, indicating the RFSoC is successfully configured.

INIT LED

The dual-color INIT LED DS3 (callout 45, Figure 1-2) indicates the RFSoC initialization status. During RFSoC initialization the INIT LED illuminates red. When RFSoC initialization has completed, the LED illuminates green.

STATUS LED

The STATUS LED DS39 (callout 45, Figure 1-2) indicates a secure lockdown state. When the PS_ERROR_STATUS pin is High, DS39 lights up.

ERROR LED

The ERROR LED DS40 (callout 45, Figure 1-2) indicates an accidental loss of power, an error, or an exception in the RFSoC processor PMU. When the PS_ERROR_OUT pin is High, DS40 lights up.

PS_POR_B Pushbutton

Pressing the PS_POR_B pushbutton SW14 (callout 15, Figure 1-2) asserts the active-Low PS_POR_B pin of the RFSoC processor.

PS_SRST_B Pushbutton

Pressing the PS_SRST_B pushbutton SW15 (callout 15, Figure 1-2) asserts the active-Low PS_SRST_B pin of the RFSoC processor.

Boot Mode Selection Headers

Four 3-pin headers are provided for mode pin selection to set the boot mode for the RFSoC processor (callout 12, Figure 1-2). Install a jumper across pins 1–2 (MIO_BUS) to set a 1, and pins 2–3 (GND) to set a 0. See Table 1-6 for a complete list of boot mode settings.

Table 1-6: **Boot Mode Selection**

Boot Mode	MODE 3 (J163)	MODE 2 (J164)	MODE 1 (J166)	MODE 0 (J165)
JTAG	0	0	0	0
QSPI24	0	0	0	1
QSPI32	0	0	1	0
SD0 (1)	0	0	1	1
NAND (1)	0	1	0	0
SD1 (1)	0	1	0	1
eMMC_18 (1)	0	1	1	0

Table 1-6: **Boot Mode Selection *(Cont'd)***

Boot Mode	MODE 3 (J163)	MODE 2 (J164)	MODE 1 (J166)	MODE 0 (J165)
USB 0 (1)	0	1	1	1
PJTAG_0 (1)	1	0	0	0
PJTAG_1 (1)	1	0	0	1
SD1-LS	1	1	1	0

Notes:
1. These boot modes are not directly supported by the ZCU1275 board.

RFSoC Processor Reference Clock

A free-running 33.3333333 MHz clock (U12) is the clock source for the RFSoC processor (PS_REF_CLK).

300 MHz LVDS Oscillator

A 300 MHz LVDS oscillator U145 (SiTime SIT9107AI-243N25E300.0000) connects to global clock (GC) pins on the RFSoC. Table 1-7 lists the RFSoC pin connections to the LVDS oscillator.

Table 1-7: **LVDS Oscillator GC Connections**

RFSoC (U1)				Schematic Net Name	Device (U145)		
Pin	Function	Direction	I/O Standard		Pin	Function	Direction
AP22	SYSTEM CLOCK_P	Input	LVDS	LVDS_OSC_P	4	300 MHz LVDS oscillator	Output
AR22	SYSTEM CLOCK_N	Input	LVDS	LVDS_OSC_N	5	300 MHz LVDS oscillator	Output

Differential SMA Pin Inputs

Two pairs of SMA connectors (callout 49, Figure 1-2) provide access to global clock (GC) pins on the RFSoC. The GC pins are connected to the SMA connectors as shown in Table 1-8.

Table 1-8: **Differential SMA Clock Connections**

RFSoC (U1)				Schematic Net Name	SMA Connector
Pin	Function	Direction	IOSTANDARD		
AP26	USER CLOCK_1_P	Input	LVDS	CLK_DIFF_1_P	J84
AR26	USER CLOCK_1_N	Input	LVDS	CLK_DIFF_1_N	J85
AT23	USER CLOCK_2_P	Input	LVDS	CLK_DIFF_2_P	J83
AT24	USER CLOCK_2_N	Input	LVDS	CLK_DIFF_2_N	J86

User LEDs

Eight active-High LEDs, DS22 through DS26, and DS46 through DS48 (callout 43, Figure 1-2), are connected to GPIO pins on the RFSoC. These LEDs can be used to indicate status or other functions. Their pinout is listed in Table 1-9.

Table 1-9: **User LEDs**

RFSoC (U1)				Schematic Net Name	Reference Designator
Pin	Function	Direction	IOSTANDARD		
AM25	USER LED	Output	LVCMOS18	APP_LED1	DS26
AL24	USER LED	Output	LVCMOS18	APP_LED2	DS22
AK22	USER LED	Output	LVCMOS18	APP_LED3	DS23
AJ22	USER LED	Output	LVCMOS18	APP_LED4	DS24
AN25	USER LED	Output	LVCMOS18	APP_LED5	DS25
AN24	USER LED	Output	LVCMOS18	APP_LED6	DS46
AM23	USER LED	Output	LVCMOS18	APP_LED7	DS47
AL23	USER LED	Output	LVCMOS18	APP_LED8	DS48

User DIP Switches and I/O Header

The DIP switch SW3 (callout 43, Figure 1-2) provides a set of eight active-High switches that connect to user I/O pins on the RFSoC as shown in Table 1-10. Use these pins to set control pins or for any other purpose. The eight I/Os also map to test header J95 (callout 43, Figure 1-2), providing external access for these pins. The I/O pins can be connected to the onboard System Controller as additional GPIO between the two devices.

Note: Install J7 to connect the user DIP switches to the System Controller.

Table 1-10: **User DIP Switches**

RFSoC (U1)				Schematic Net Name	DIP Switch Reference Designator	J95 Test Header Pin	Device (U38) Pin
Pin	Function	Direction	IOSTANDARD				
AV25	User Switch	Input	LVCMOS18	USER_SW1	SW3	1	F12
AU25	User Switch	Input	LVCMOS18	USER_SW2		3	E13
AV23	User Switch	Input	LVCMOS18	USER_SW3		5	E11
AU23	User Switch	Input	LVCMOS18	USER_SW4		7	E12
AW24	User Switch	Input	LVCMOS18	USER_SW5		9	F13
AV24	User Switch	Input	LVCMOS18	USER_SW6		11	F14
BA22	User Switch	Input	LVCMOS18	USER_SW7		13	G15
AY22	User Switch	Input	LVCMOS18	USER_SW8		15	F15

Figure 1-9 shows the user I/O connector J95 (callout 43, Figure 1-2).

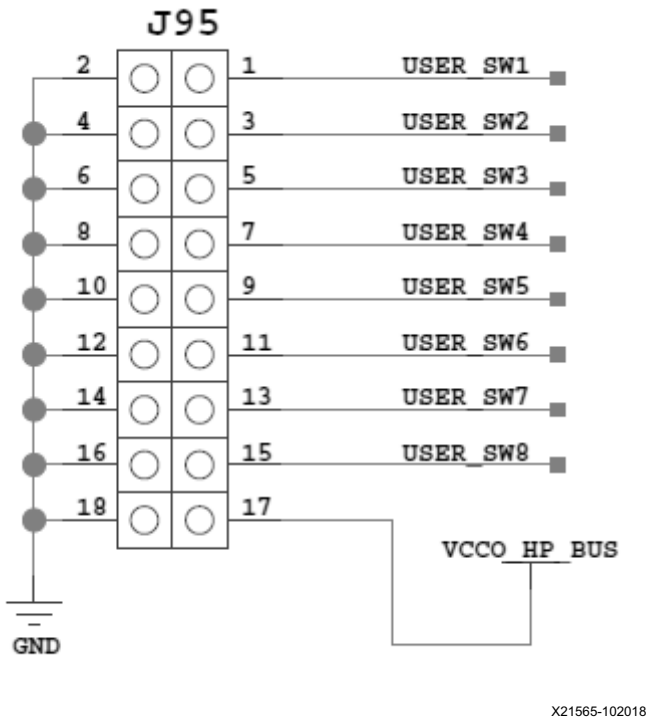

Figure 1-9: **User I/O Connector J95**

User Pushbuttons

SW16 and SW17 (callout 43, Figure 1-2) are active-High user pushbuttons that are connected to RFSoC I/O pins as shown in Table 1-11. These pushbuttons can be used for any user-determined purpose.

Table 1-11: **User Pushbuttons**

RFSoC (U1)				Schematic Net Name	Reference Designator
Pin	Function	Direction	IOSTANDARD		
AM22	User Pushbutton	Input	LVCMOS18	USER_PB1	SW16
AN26	User Pushbutton	Input	LVCMOS18	USER_PB2	SW17

System Monitor

The System Monitor (SYSMON) monitors the physical environment using on-chip temperature and supply sensors, up to 17 external analog inputs, and an integrated analog-to-digital converter (ADC). There is a separate SYSMON for the PL and the PS. The PS SYSMON is powered using the on-chip reference voltage (V_{REF}), and the PL SYSMON is

powered using an external 1.25V regulator. See Figure 1-10 for connection details. More information about the system monitor is available in *UltraScale Architecture System Monitor User Guide* (UG580) [Ref 5].

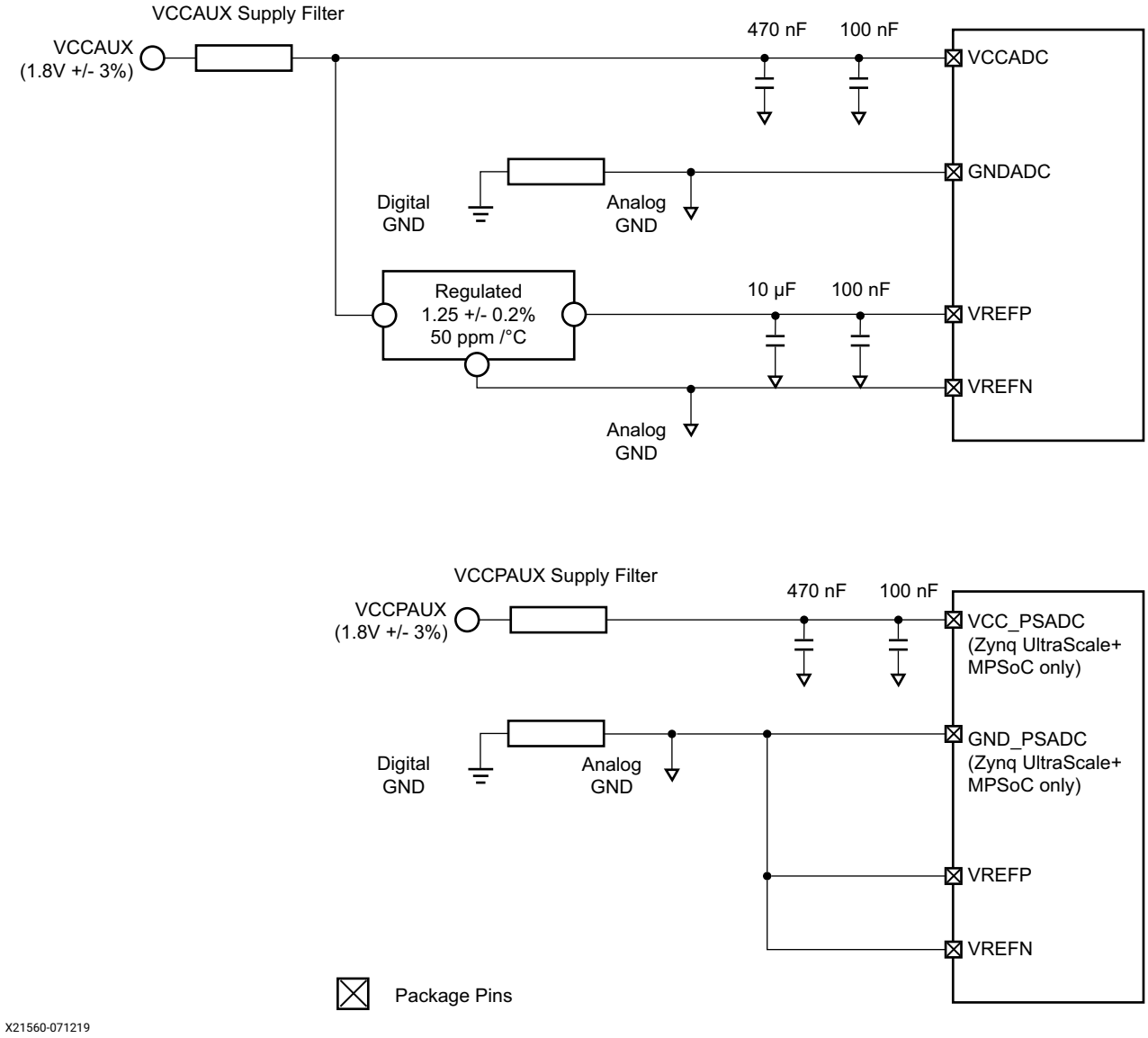

Figure 1-10: **PL and PS SYSMON Power Connections**

QSPI Flash Memory

A single QSPI device (MT25QU01GBBB8ESF-0SIT 1.8V) is available for booting the RFSoC. To enable QSPI, boot shunts must be installed as indicated in Table 1-6.

SD Card

An SD card slot is provided (callout 52, Figure 1-2) for booting the RFSoC. The ZCU1275 board supports SD 3.0 and has an SD 3.0 compliant voltage level shifter. To enable SD boot, shunts must be installed for SD1-LS boot mode as indicated in Table 1-6.

DDR3 Memory

The board provides 2 GB of DDR3 memory utilizing a 64-bit bus and running at 2133 Mb/s. The memory system is composed of four x16 Samsung 4 Gb, 1.5V K4B4G1646D-BCNB devices. The memory is accessible through the processing system (PS) of the Zynq UltraScale+ RFSoC.

RF Data Converters and Sampling Clocks

The ZCU1275 board provides access to all of the RFSoC RF-ADC and RF-DAC signal and clock pins. Each RF-ADC and RF-DAC is designed with –70 db isolation at 3 GHz. The four RF-ADC tiles (224, 225, 226, and 227) are brought out to two Bulls Eye connectors and a header for the VCM pins (callout 36 and 37, Figure 1-2). The four RF-DAC tiles (228, 229, 230, and 231) are brought out to two Bulls Eye connectors and an SMA pair for SYSREF (callout 36 and 48, Figure 1-2). The pinouts for the RF-ADC and RF-DAC Bulls Eye connectors are shown in Figure 1-11, and the pinout for the VCM connector is shown in Figure 1-12.

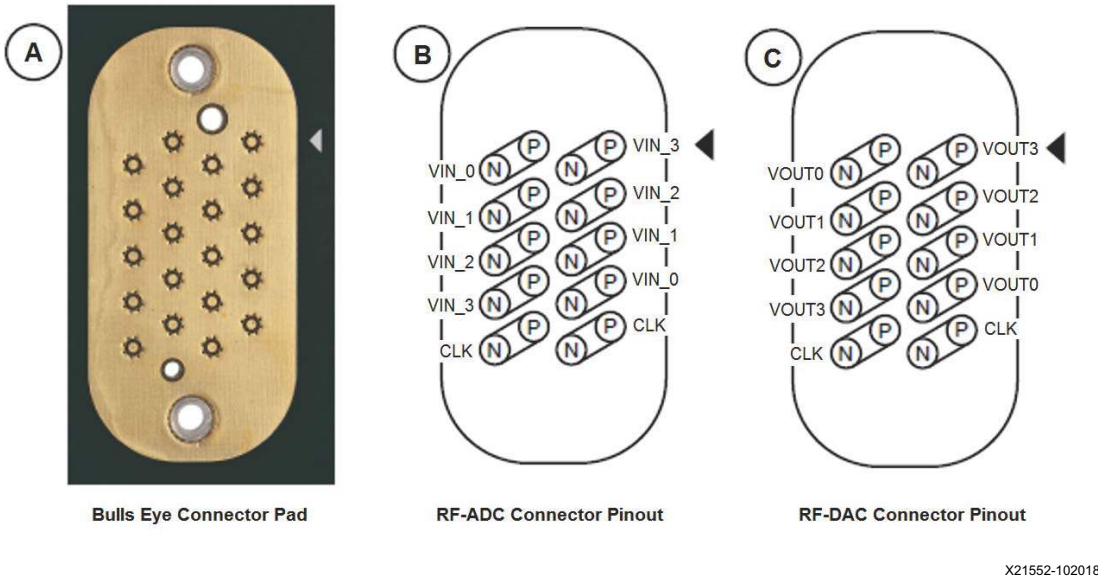

Figure 1-11: **A: Bulls Eye Connector Pad. B: RF-ADC Connector Pinout. C: RF-DAC Connector Pinout**

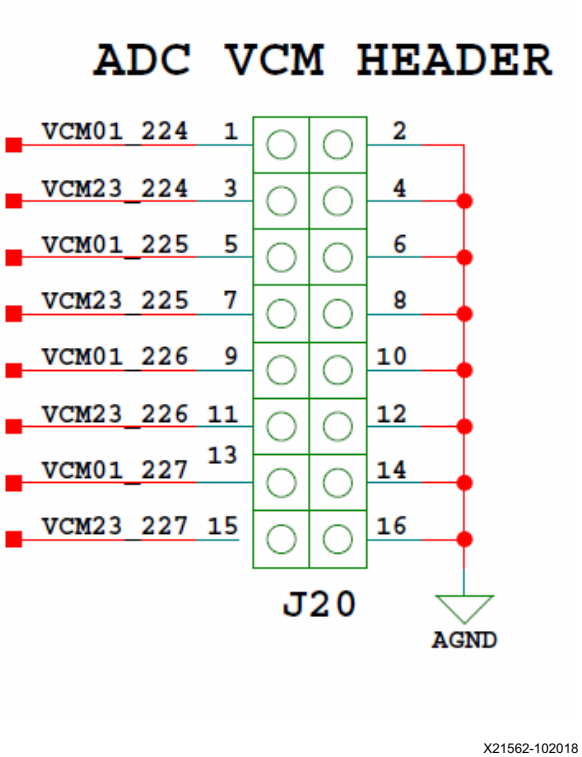

Figure 1-12: **RF-ADC VCM Header Pinout**

The information for each RF-ADC pin is listed in Table 1-12.

Table 1-12: **RF-ADC Pins**

RFSoC (U1)	Net Name	Tile	Connector	Trace Length (mils)
AU5	ADC_VIN0_224_P	224	J124	3283.024
AU4	ADC_VIN0_224_N	224	J124	3280.721
AU2	ADC_VIN1_224_P	224	J124	3138.125
AU1	ADC_VIN1_224_N	224	J124	3135.787
AR5	ADC_VIN2_224_P	224	J124	3277.759
AR4	ADC_VIN2_224_N	224	J124	3275.53
AR2	ADC_VIN3_224_P	224	J124	3164.561
AR1	ADC_VIN3_224_N	224	J124	3162.691
BA3	ADC_CLK_224_P	224	J124	3283.463
BB3	ADC_CLK_224_N	224	J124	3279.967
AJ11	VCM01_224	224	J20	-
AJ10	VCM23_224	224	J20	-
AF9	ADC_REXT_224	224	J127	-
AN5	ADC_VIN0_225_P	225	J124	3309.41
AN4	ADC_VIN0_225_N	225	J124	3307.012
AN2	ADC_VIN1_225_P	225	J124	3196.802
AN1	ADC_VIN1_225_N	225	J124	3194.401
AL5	ADC_VIN2_225_P	225	J124	3342.156
AL4	ADC_VIN2_225_N	225	J124	3339.779
AL2	ADC_VIN3_225_P	225	J124	3223.9
AL1	ADC_VIN3_225_N	225	J124	3221.624
AW4	ADC_CLK_225_P	225	J124	3280.453
AY4	ADC_CLK_225_N	225	J124	3279.826
AH11	VCM01_225	225	J20	-
AH10	VCM23_225	225	J20	-
AJ5	ADC_VIN0_226_P	226	J278	3360.63
AJ4	ADC_VIN0_226_N	226	J278	3358.274
AJ2	ADC_VIN1_226_P	226	J278	3242.988
AJ1	ADC_VIN1_226_N	226	J278	3240.685
AG5	ADC_VIN2_226_P	226	J278	3376.291
AG4	ADC_VIN2_226_N	226	J278	3374.059
AG2	ADC_VIN3_226_P	226	J278	3253.421
AG1	ADC_VIN3_226_N	226	J278	3253.248

Table 1-12: **RF-ADC Pins *(Cont'd)***

RFSoC (U1)	Net Name	Tile	Connector	Trace Length (mils)
BA5	ADC_CLK_226_P	226	J278	3091.053
BB5	ADC_CLK_226_N	226	J278	3088.424
AJ8	VCM01_226	226	J20	-
AJ7	VCM23_226	226	J20	-
AE5	ADC_VIN0_227_P	227	J278	3393.677
AE4	ADC_VIN0_227_N	227	J278	3391.355
AE2	ADC_VIN1_227_P	227	J278	3274.172
AE1	ADC_VIN1_227_N	227	J278	3272.253
AC5	ADC_VIN2_227_P	227	J278	3399.961
AC4	ADC_VIN2_227_N	227	J278	3397.632
AC2	ADC_VIN3_227_P	227	J278	3288.831
AC1	ADC_VIN3_227_N	227	J278	3286.82
AW6	ADC_CLK_227_P	227	J278	3095.716
AY6	ADC_CLK_227_N	227	J278	3099.089
AH8	VCM01_227	227	J20	-
AH7	VCM23_227	227	J20	-

The information for each RF-DAC pin is listed in Table 1-13.

Table 1-13: **RF-DAC Pins**

RFSoC (U1)	Net Name	Tile	Connector	Trace Length (mils)
Y5	DAC_VOUT0_228_P	228	J129	3366.712
Y4	DAC_VOUT0_228_N	228	J129	3364.991
Y2	DAC_VOUT1_228_P	228	J129	3209.197
Y1	DAC_VOUT1_228_N	228	J129	3207.209
V5	DAC_VOUT2_228_P	228	J129	3349.961
V4	DAC_VOUT2_228_N	228	J129	3347.9
V2	DAC_VOUT3_228_P	228	J129	3192.969
V1	DAC_VOUT3_228_N	228	J129	3190.879
B3	DAC_CLK_228_P	228	J129	3340.507
A3	DAC_CLK_228_N	228	J129	3343.285
D2	SYSREF_228_P	228	J242	-
D1	SYSREF_228_N	228	J243	-
U9	DAC_REXT_228	228	J128	-
T5	DAC_VOUT0_229_P	229	J129	3319.868
T4	DAC_VOUT0_229_N	229	J129	3317.681

Table 1-13: **RF-DAC Pins *(Cont'd)***

RFSoC (U1)	Net Name	Tile	Connector	Trace Length (mils)
T2	DAC_VOUT1_229_P	229	J129	3178.213
T1	DAC_VOUT1_229_N	229	J129	3176.101
P5	DAC_VOUT2_229_P	229	J129	3320.982
P4	DAC_VOUT2_229_N	229	J129	3319.001
P2	DAC_VOUT3_229_P	229	J129	3163.2
P1	DAC_VOUT3_229_N	229	J129	3165.4
D4	DAC_CLK_229_P	229	J129	3556.617
C4	DAC_CLK_229_N	229	J129	3560.447
M5	DAC_VOUT0_230_P	230	J279	3267.684
M4	DAC_VOUT0_230_N	230	J279	3265.525
M2	DAC_VOUT1_230_P	230	J279	3152.804
M1	DAC_VOUT1_230_N	230	J279	3150.782
K5	DAC_VOUT2_230_P	230	J279	3287.039
K4	DAC_VOUT2_230_N	230	J279	3284.711
K2	DAC_VOUT3_230_P	230	J279	3141.679
K1	DAC_VOUT3_230_N	230	J279	3139.098
B5	DAC_CLK_230_P	230	J279	3615.019
A5	DAC_CLK_230_N	230	J279	3619.695
H5	DAC_VOUT0_231_P	231	J279	3265.511
H4	DAC_VOUT0_231_N	231	J279	3263.254
H2	DAC_VOUT1_231_P	231	J279	3111.166
H1	DAC_VOUT1_231_N	231	J279	3108.992
F5	DAC_VOUT2_231_P	231	J279	3243.78
F4	DAC_VOUT2_231_N	231	J279	3241.56
F2	DAC_VOUT3_231_P	231	J279	3071.556
F1	DAC_VOUT3_231_N	231	J279	3069.35
D6	DAC_CLK_231_P	231	J279	3834.883
C6	DAC_CLK_231_N	231	J279	3835.078

Serial Transceivers and Reference Clocks

The ZCU1275 board provides access to all GTY and PS-GTR transceiver and reference clock pins of the RFSoC (callout 33 and 34, Figure 1-2). The serial transceivers are grouped into five sets of four TX-RX lanes, referred to as Quads. There are four GTY Quads (Q128 –Q131), and one PS-GTR Quad (bank 505).

All GTY and PS-GTR Quads and their associated reference clocks (CLK0 and CLK1) are brought out to a connector pad, which interfaces with Samtec Bulls Eye connectors used with the Samtec RSP-200723-02-BEYE cable assembly. Contact Samtec, Inc., for information about this or other cable assemblies [Ref 6]. Figure 1-13 A shows the connector pad. Figure 1-13 B shows the connector pinout.

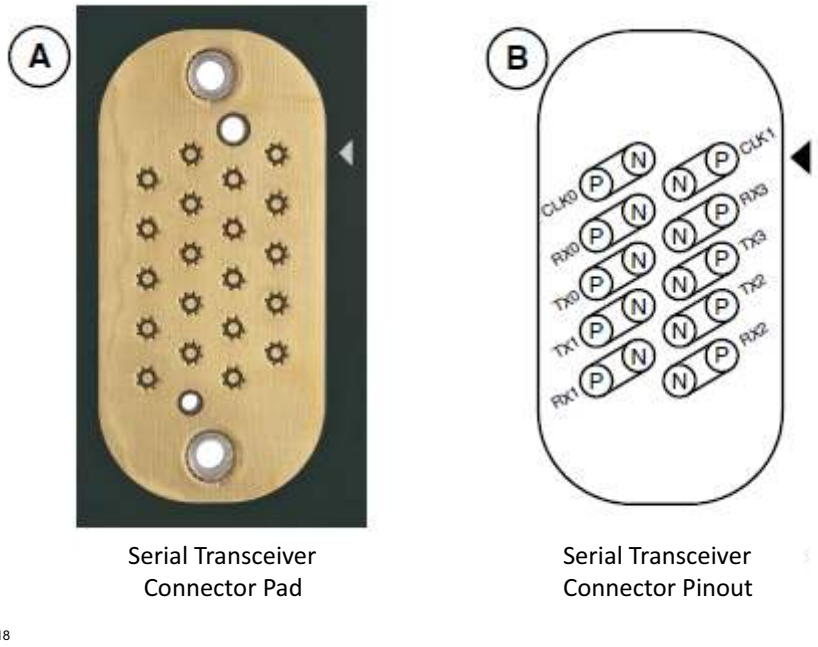

Figure 1-13: **Serial Transceiver Connector Pad and Pinout**

PS-GTR bank 505 has two additional reference clocks (CLK2 and CLK3) which are brought out to two pairs of SMA connectors (callout 18, Figure 1-2).

The information for each GTY transceiver pin is shown in Table 1-14.

Table 1-14: **GTY Transceiver Pins**

RFSoC (U1)	Net Name	Quad	Connector	Trace Length (mils)
AC42	128_RX0_N	128	J117	2707.458
AC41	128_RX0_P	128	J117	2707.296
AB40	128_RX1_N	128	J117	3507.681
AB39	128_RX1_P	128	J117	3508.445
AA42	128_RX2_N	128	J117	2940.702
AA41	128_RX2_P	128	J117	2938.24
Y40	128_RX3_N	128	J117	2644.503
Y39	128_RX3_P	128	J117	2647.811
V39	128_TX0_N	128	J117	3148.266

Table 1-14: **GTY Transceiver Pins *(Cont'd)***

RFSoC (U1)	Net Name	Quad	Connector	Trace Length (mils)
V38	128_TX0_P	128	J117	3147.413
U37	128_TX1_N	128	J117	3228.503
U36	128_TX1_P	128	J117	3229.157
T39	128_TX2_N	128	J117	3053.346
T38	128_TX2_P	128	J117	3057.162
R37	128_TX3_N	128	J117	2914.568
R36	128_TX3_P	128	J117	2917.948
W42	129_RX0_N	129	J118	2336.327
W41	129_RX0_P	129	J118	2336.177
U42	129_RX1_N	129	J118	2915.189
U41	129_RX1_P	129	J118	2915.033
R42	129_RX2_N	129	J118	2660.231
R41	129_RX2_P	129	J118	2663.549
N42	129_RX3_N	129	J118	2191.652
N41	129_RX3_P	129	J118	2194.96
P39	129_TX0_N	129	J118	2580.324
P38	129_TX0_P	129	J118	2579.92
N37	129_TX1_N	129	J118	2828.966
N36	129_TX1_P	129	J118	2829.422
M39	129_TX2_N	129	J118	2684.658
M38	129_TX2_P	129	J118	2688.416
L37	129_TX3_N	129	J118	2565.464
L36	129_TX3_P	129	J118	2564.925
L42	130_RX0_N	130	J280	2169.162
L41	130_RX0_P	130	J280	2168.011
J42	130_RX1_N	130	J280	2753.85
J41	130_RX1_P	130	J280	2753.847
G42	130_RX2_N	130	J280	2708.119
G41	130_RX2_P	130	J280	2710.988
F40	130_RX3_N	130	J280	2298.952
F39	130_RX3_P	130	J280	2302.779
K39	130_TX0_N	130	J280	2503.962
K38	130_TX0_P	130	J280	2502.727
J37	130_TX1_N	130	J280	2738.854
J36	130_TX1_P	130	J280	2738.821

Table 1-14: **GTY Transceiver Pins *(Cont'd)***

RFSoC (U1)	Net Name	Quad	Connector	Trace Length (mils)
H39	130_TX2_N	130	J280	2660.143
H38	130_TX2_P	130	J280	2659.72
G37	130_TX3_N	130	J280	2877.072
G36	130_TX3_P	130	J280	2877.059
E42	131_RX0_N	131	J281	2585.706
E41	131_RX0_P	131	J281	2585.352
D40	131_RX1_N	131	J281	3037.05
D39	131_RX1_P	131	J281	3034.196
C42	131_RX2_N	131	J281	3275.72
C41	131_RX2_P	131	J281	3274.21
B40	131_RX3_N	131	J281	2676.92
B39	131_RX3_P	131	J281	2675.781
F35	131_TX0_N	131	J281	2940.112
F34	131_TX0_P	131	J281	2939.226
E37	131_TX1_N	131	J281	3346.063
E36	131_TX1_P	131	J281	3345.916
C37	131_TX2_N	131	J281	3431.684
C36	131_TX2_P	131	J281	3432.171
A37	131_TX3_N	131	J281	3180.526
A36	131_TX3_P	131	J281	3181.286

Information for each GTY transceiver clock input is shown in Table 1-15.

Table 1-15: **GTY Transceiver Reference Clock Inputs**

RFSoC (U1)	Net Name	Quad	Connector
AA36	128_REFCLK0_N	128	J117
AA37	128_REFCLK0_P	128	J117
Y34	128_REFCLK1_N	128	J117
Y35	128_REFCLK1_P	128	J117
V34	129_REFCLK0_N	129	J118
V35	129_REFCLK0_P	129	J118
T34	129_REFCLK1_N	129	J118
T35	129_REFCLK1_P	129	J118
P34	130_REFCLK0_N	130	J280
P35	130_REFCLK0_P	130	J280
M34	130_REFCLK1_N	130	J280

Table 1-15: **GTY Transceiver Reference Clock Inputs *(Cont'd)***

RFSoC (U1)	Net Name	Quad	Connector
M35	130_REFCLK1_P	130	J280
K34	131_REFCLK0_N	131	J281
K35	131_REFCLK0_P	131	J281
H34	131_REFCLK1_N	131	J281
H35	131_REFCLK1_P	131	J281

Information for each PS-GTR transceiver pin is shown in Table 1-16.

Table 1-16: **PS-GTR Transceiver Pins**

RFSoC (U1)	Net Name	Bank	Connector	Trace Length (mils)
AJ42	PS_RX0_N	505	J39	3920.298
AJ41	PS_RX0_P	505	J39	3918.182
AH40	PS_RX1_N	505	J39	4537.184
AH39	PS_RX1_P	505	J39	4537.361
AG42	PS_RX2_N	505	J39	4299.2
AG41	PS_RX2_P	505	J39	4302.524
AE42	PS_RX3_N	505	J39	3174.371
AE41	PS_RX3_P	505	J39	3173.868
AH36	PS_TX0_N	505	J39	3400.509
AH35	PS_TX0_P	505	J39	3399.45
AG38	PS_TX1_N	505	J39	3468.187
AG37	PS_TX1_P	505	J39	3467.251
AF40	PS_TX2_N	505	J39	3721.249
AF39	PS_TX2_P	505	J39	3724.655
AE38	PS_TX3_N	505	J39	3301.206
AE37	PS_TX3_P	505	J39	3304.523

Information for each PS-GTR transceiver clock input is shown in Table 1-17.

Table 1-17: **PS-GTR Transceiver Reference Clock Inputs**

RFSoC (U1)	Net Name	Bank	Connector
AF34	PS_REFCLK0_P	505	J39
AF35	PS_REFCLK0_N	505	J39
AD34	PS_REFCLK1_P	505	J39
AD35	PS_REFCLK1_N	505	J39
AC36	PS_REFCLK2_P	505	J194
AC37	PS_REFCLK2_N	505	J156

Table 1-17: **PS-GTR Transceiver Reference Clock Inputs *(Cont'd)***

RFSoC (U1)	Net Name	Bank	Connector
AB34	PS_REFCLK3_P	505	J158
AB35	PS_REFCLK3_N	505	J159

SuperClock-2 Module

The SuperClock-2 Module (callout 6, Figure 1-2) connects to the clock module interface connector (J36) and provides a programmable, low-noise and low-jitter clock source intended for use with the GTY and PS-GTR transceivers. The clock module maps to the RFSoC by way of two I2C signals, two LVDS pairs, and one global clock pair. Table 1-18 shows the RFSoC mapping for the SuperClock-2 Module interface. To program the SuperClock-2 Module using the System Controller, see Appendix D, System Controller. To connect to the SuperClock-2 Module using the I2C bus, see I2C Bus Management.

Table 1-18: **SuperClock-2 Interface Connections**

RFSoC (U1)				Schematic Net Name	J36 Pin		
Pin	Function	Direction	IOSTANDARD		Pin	Function	Direction
L28	Clock Recovery	Input	LVDS	CM_LVDS1_P	1	Clock Recovery	Output
L29	Clock Recovery	Input	LVDS	CM_LVDS1_N	3	Clock Recovery	Output
H10	Clock Recovery	Input	LVDS	CM_LVDS2_P	9	Clock Recovery	Output
H9	Clock Recovery	Input	LVDS	CM_LVDS2_N	11	Clock Recovery	Output
AP24	Global Clock	Input	LVDS	CM_GCLK_P	25	Global Clock	Output
AR24	Global Clock	Input	LVDS	CM_GCLK_N	27	Global Clock	Output
AM26	Control I/O	Bidir	LVCMOS	CM_I2C_SCL/ DUT_PMBUS_CLK	62	I2C	Bidir
AP23	Control I/O	Bidir	LVCMOS	CM_I2C_SDA/ DUT_PMBUS_DATA	64	I2C	Bidir

SuperClock-RF2 Module

The SuperClock-RF2 Module (callout 42, Figure 1-2) connects to the clock module interface connector (J170) and provides a programmable, ultra low noise and low-jitter wideband RF clock source intended for use with the RFSoC RF data converters. It provides three phase-aligned LVDS reference clocks, one single-ended LVCMOS reference clock, four differential pair RF clocks for RF-ADCs, and four differential pair RF clocks for RF-DACs. The SuperClock-RF2 module schematic, BOM, and Allegro board files are in the XTP524

document package on the Zynq UltraScale+ RFSoC ZCU1275 Characterization Kit page. The SuperClock-RF2 Module block diagram is shown in Figure 1-14.

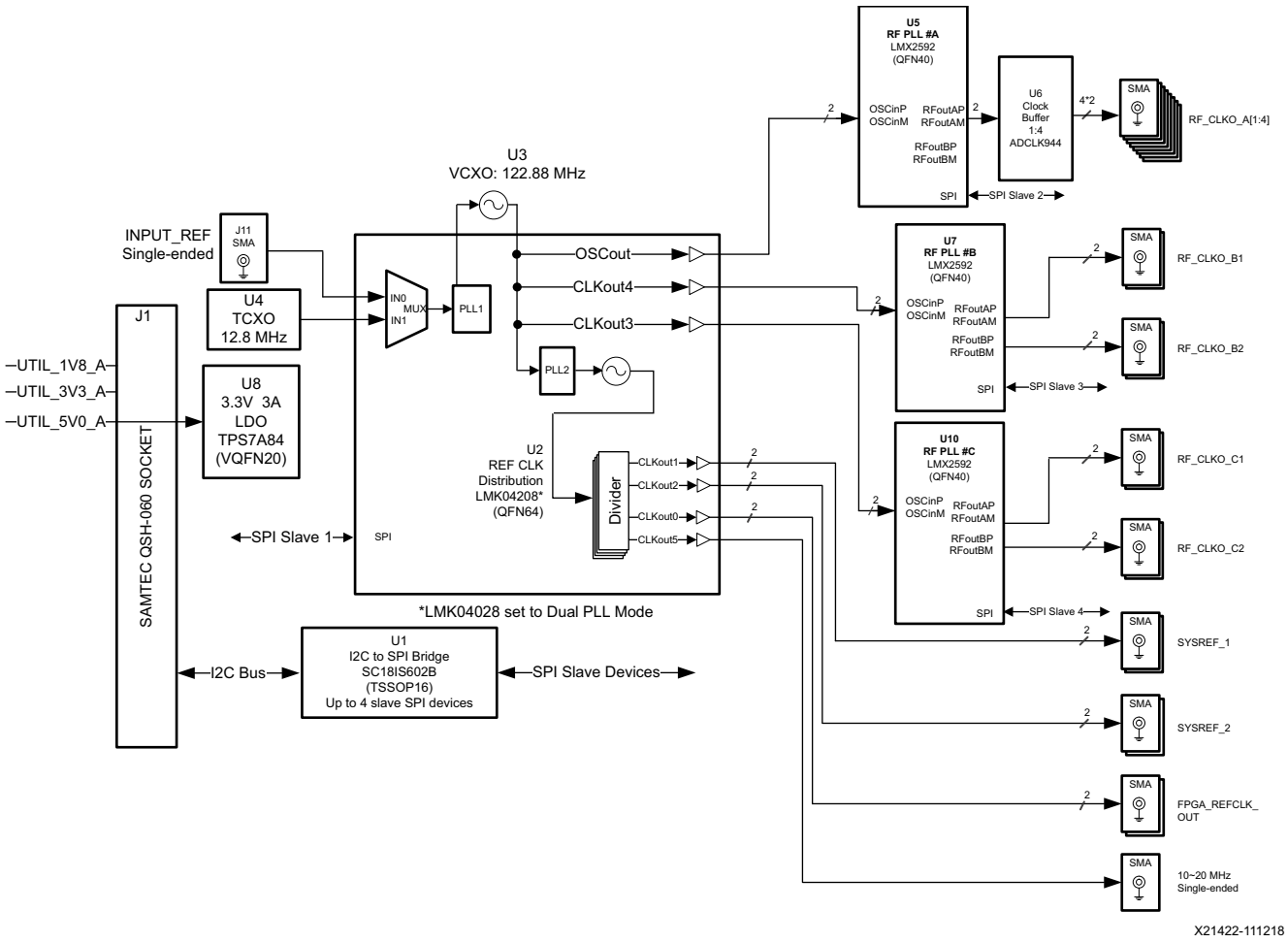

Figure 1-14: **SuperClock-RF2 Module Block Diagram**

Figure 1-15 shows the SuperClock-RF2 Module. Each numbered feature referenced in Figure 1-15 is described in Table 1-19 and the sections that follow.

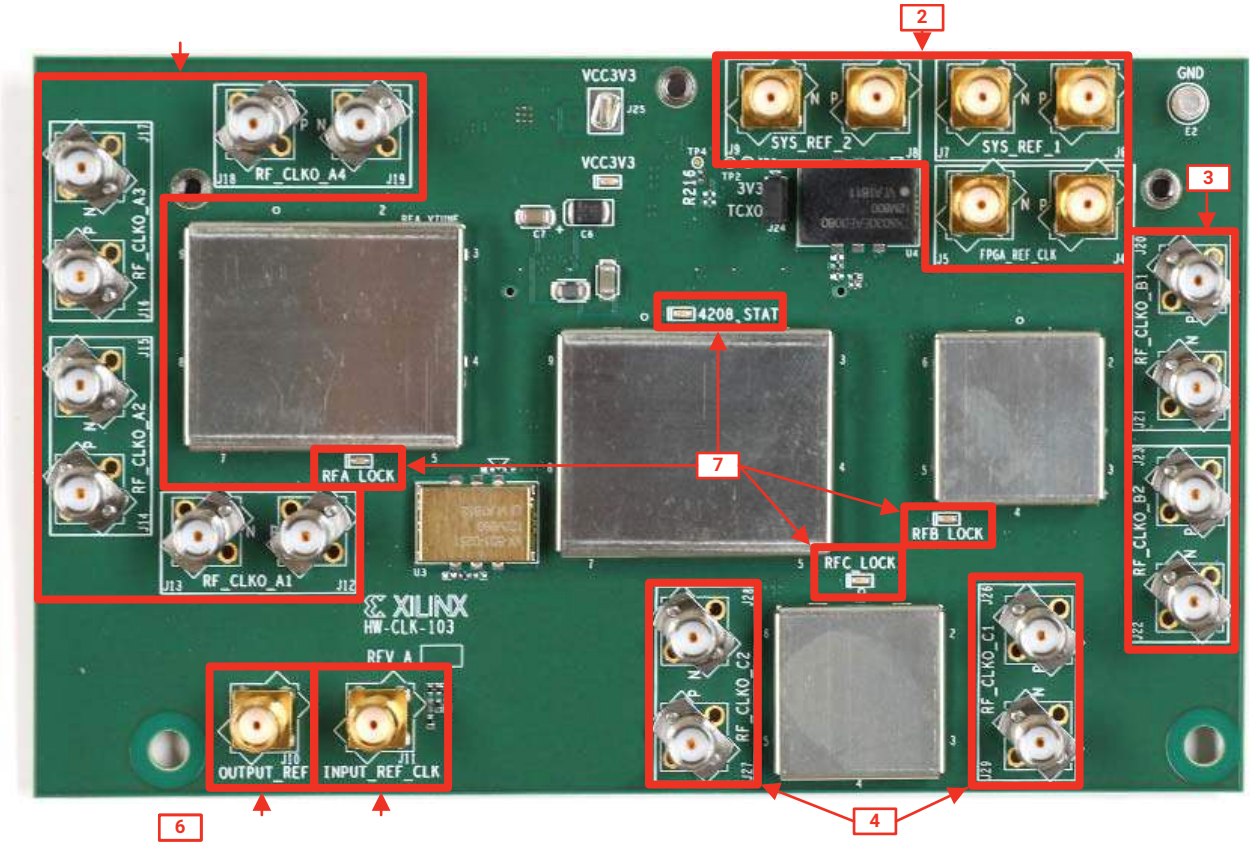

Figure 1-15: **SuperClock-RF2 Module Features**

Table 1-19: **SuperClock-2 Interface Connections**

Callouts	Reference Designators	Feature Description
1	J12, J13, J14, J15, J16, J17, J18, J19	PLL A RF sampling clock SMA pairs
2	J4, J5, J6, J7, J8, J9	General-purpose clock SMA pairs
3	J20, J21, J22, J23	PLL B RF sampling clock SMA pairs
4	J26, J27, J28, J29	PLL C RF sampling clock SMA pairs
5	J11	External reference clock input
6	J10	Single-ended reference clock output
7	DS1, DS2, DS3, DS5	PLL lock indicator LEDs

PLL A

PLL A has four differential output SMA pairs which are intended to be used as RF sampling clocks for RF-ADCs. They are programmable to any frequency up to 4.0 GHz with a phase noise performance of –133 dBc/Hz at 1 MHz offset from the carrier and a typical output power level of 3 dBm at 4 GHz. The default boot frequency for this PLL is 3.93216 GHz.

PLL B and C

PLL B and C have two differential output SMA pairs each, which are intended to be used as RF sampling clocks for RF-DACs. Each PLL is programmable to any frequency up to 6.4 GHz with a phase noise performance of –130 dBc/Hz at 1 MHz offset from the carrier and individually programmable output power levels up to 6 dBm. The default boot frequency for each of these PLLs is 4.9152 GHz and a typical output power level is 4 dBm.

General Purpose Clocks

The general-purpose clocks are three pairs of phase-aligned LVDS clocks (SYS_REF_1, SYS_REF_2, and FPGA_REF_CLK) programmable to any frequency up to 1.0 GHz. Each clock pair can be individually enabled or disabled. The default boot state for these clocks is disabled.

Single-Ended Reference Clock

The single-ended reference clock is an LVCMOS output that can be enabled or disabled, and is programmable to any frequency up to 250 MHz. The default boot frequency for this clock is 12.8 MHz.

Programming the Clocks

The clocks on the SuperClock-RF2 Module can be programmed using the System Controller user interface (SCUI). See Appendix D, System Controller. A set of clock files are provided along with the System Controller user interface. The clock files contain PLL register values used to program the clocks to a pre-set frequency. To create custom clock files, contact Texas Instruments [Ref 7].

SuperClock-RF2 Pin Mapping

The SuperClock-RF2 Module maps to RFSoC I/O by way of two I2C signals. Table 1-20 shows the RFSoC I/O mapping for the SuperClock-RF2 Module interface. To connect to the SuperClock-RF2 Module using the I2C bus, see I2C Bus Management.

Table 1-20: **RFSoC PS to UART Connection**

RFSoC (U1)				Schematic Net Name	J170 Pin		
Pin	Function	Direction	IOSTANDARD		Pin	Function	Direction
AM26	Control I/O	Bidir	LVCMOS	ACM_SCL/ DUT_PMBUS_CLK	62	I2C	Bidir
AP23	Control I/O	Bidir	LVCMOS	ACM_SDA/ DUT_PMBUS_DATA	64	I2C	Bidir

Balun Board

The balun board shown in Figure 1-16 and Figure 1-17 is included in the ZCU1275 kit. It has five baluns accessible through SMA connectors. Two baluns are high frequency, two are low frequency, and one is for a clock channel. The details of the baluns are listed in Table 1-21. The balun board schematic, BOM, and Allegro board files are in the XTP525 document package on the Zynq UltraScale+ RFSoC ZCU1275 Characterization Kit page.

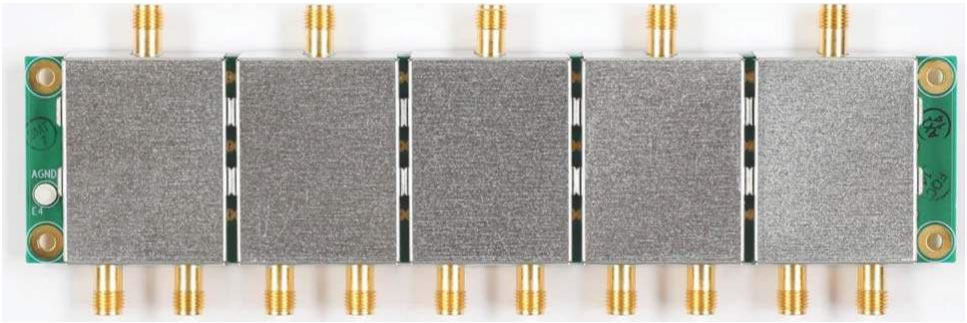

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Figure 1-16: **Balun Board—Top Side**

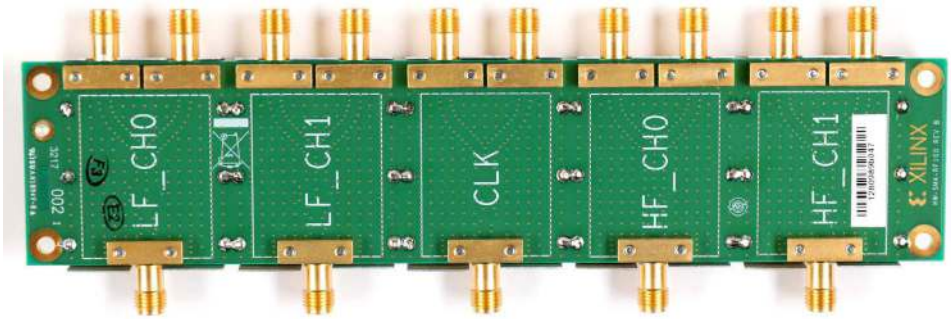

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Figure 1-17: **Balun Board—Bottom Side**

Table 1-21: **Balun Board Details**

Balun Board Label	Manufacturer	Part Number	Frequency Range
LF_CH0	Mini Circuits	TCM2-33WX+	10–3000 MHz
LF_CH1	Mini Circuits	TCM2-33WX+	10–3000 MHz
CLK	Mini Circuits	TCM1-83X+	10–8000 MHz
HF_CH0	Anaren	BD1631J50100AHF	1.6–3.1 GHz
HF_CH1	Anaren	BD1631J50100AHF	1.6–3.1 GHz

FPGA Mezzanine Card Interface

The ZCU1275 board features one high pin count (HPC) FPGA Mezzanine card (FMC) connector and one low pin count (LPC) FMC connector as defined by the VITA 57.1 FPGA Mezzanine card specification (callout 53 and 54, Figure 1-2). The FMC connector is a 10 x 40 position socket. See Appendix B, VITA 57.1 FMC Connector Pinouts for a cross-reference of signal names to pin coordinates. The FMC connectors are identified as FMC2 at JA3 and FMC3 at JA4.

FMC 2 HPC connector JA3 provides connectivity for:

- 80 differential user-defined pairs:
  - 34 LA pairs
  - 24 HA pairs
  - 22 HB pairs
- 4 differential clocks

FMC3 LPC connector JA4 provides connectivity for:

- 34 differential user-defined pairs:
  - 34 LA pairs
- 4 differential clocks

IMPORTANT: *The V_{ADJ} voltage on the FMC2 LPC connector tracks VCCO_HP, and on the FMC3 connector it tracks VCCO_HD.*

The connections for each of these connectors are listed in Table 1-22 and Table 1-23, respectively.

Table 1-22: **FMC2 HPC Connections at JA3**

RFSoC (U1) Pin	Net Name	FMC Pin
H28	FMC2_CLK0_M2C_P	H4
H29	FMC2_CLK0_M2C_N	H5
H30	FMC2_CLK1_M2C_P	G2
G30	FMC2_CLK1_M2C_N	G3
AP26	FMC2_CLK2_BIDIR_P	K4
AR26	FMC2_CLK2_BIDIR_N	K5
AT23	FMC2_CLK3_BIDIR_P	J2
AT24	FMC2_CLK3_BIDIR_N	J3
AP18	FMC2_HA00_CCP	F4
AP17	FMC2_HA00_CCN	F5
AN21	FMC2_HA01_CCP	E2
AN20	FMC2_HA01_CCN	E3
AH20	FMC2_HA02P	K7
AH19	FMC2_HA02N	K8
AH21	FMC2_HA03P	J6
AJ21	FMC2_HA03N	J7
AH18	FMC2_HA04P	F7
AJ18	FMC2_HA04N	F8
AK21	FMC2_HA05P	E6
AK20	FMC2_HA05N	E7
AJ17	FMC2_HA06P	K10
AK17	FMC2_HA06N	K11
AK19	FMC2_HA07P	J9
AL19	FMC2_HA07N	J10
AL18	FMC2_HA08P	F10
AL17	FMC2_HA08N	F11
AM21	FMC2_HA09P	E9
AM20	FMC2_HA09N	E10
AM18	FMC2_HA10P	K13
AN18	FMC2_HA10N	K14
AN19	FMC2_HA11P	J12
AP19	FMC2_HA11N	J13

Table 1-22: **FMC2 HPC Connections at JA3 *(Cont'd)***

RFSoC (U1) Pin	Net Name	FMC Pin
AP21	FMC2_HA12P	F13
AR21	FMC2_HA12N	F14
AT20	FMC2_HA13P	E12
AT19	FMC2_HA13N	E13
AU21	FMC2_HA14P	J15
AU20	FMC2_HA14N	J16
AT18	FMC2_HA15P	F16
AU18	FMC2_HA15N	F17
AW21	FMC2_HA16P	E15
AY21	FMC2_HA16N	E16
AR20	FMC2_HA17_CCP	K16
AR19	FMC2_HA17_CCN	K17
AV19	FMC2_HA18P	J18
AW19	FMC2_HA18N	J19
AY20	FMC2_HA19P	F19
BA20	FMC2_HA19N	F20
AV18	FMC2_HA20P	E18
AW18	FMC2_HA20N	E19
AY19	FMC2_HA21P	K19
BA19	FMC2_HA21N	K20
BA18	FMC2_HA22P	J21
BB18	FMC2_HA22N	J22
BB21	FMC2_HA23P	K22
BB20	FMC2_HA23N	K23
AT15	FMC2_HB00_CCP	K25
AU15	FMC2_HB00_CCN	K26
AJ14	FMC2_HB01_CCP	J24
AK14	FMC2_HB01_CCN	J25
AK16	FMC2_HB02P	F22
AK15	FMC2_HB02N	F23
AL15	FMC2_HB03P	E21
AM15	FMC2_HB03N	E22
AM16	FMC2_HB04P	F25
AN15	FMC2_HB04N	F26
AM16	FMC2_HB05P	E24

Table 1-22: **FMC2 HPC Connections at JA3 *(Cont'd)***

RFSoC (U1) Pin	Net Name	FMC Pin
AN15	FMC2_HB05N	E25
AU17	FMC2_HB06P	K28
AU16	FMC2_HB06N	K29
AN16	FMC2_HB07P	J27
AP16	FMC2_HB07N	J28
AN13	FMC2_HB08P	F28
AP13	FMC2_HB08N	F29
AR16	FMC2_HB09P	E27
AR15	FMC2_HB09N	E28
AR14	FMC2_HB10P	K31
AT14	FMC2_HB10N	K32
AR17	FMC2_HB11P	J30
AT17	FMC2_HB11N	J31
AV16	FMC2_HB12P	F31
AV15	FMC2_HB12N	F32
AV14	FMC2_HB13P	E30
AW14	FMC2_HB13N	E31
AW17	FMC2_HB14P	K34
AW16	FMC2_HB14N	K35
AV13	FMC2_HB15P	J33
AW13	FMC2_HB15N	J34
AY17	FMC2_HB16P	F34
AY16	FMC2_HB16N	F35
AT13	FMC2_HB17_CCP	K37
AU13	FMC2_HB17_CCN	K38
AY15	FMC2_HB18P	J36
AY14	FMC2_HB18N	J37
BA15	FMC2_HB19P	E33
BA14	FMC2_HB19N	E34
BB16	FMC2_HB20P	F37
BB15	FMC2_HB20N	F38
BA13	FMC2_HB21P	E36
BA12	FMC2_HB21N	E37
G27	FMC2_LA00_CCP	G6
G28	FMC2_LA00_CCN	G7

Table 1-22: **FMC2 HPC Connections at JA3 *(Cont'd)***

RFSoC (U1) Pin	Net Name	FMC Pin
F30	FMC2_LA01_CCP	D8
E30	FMC2_LA01_CCN	D9
A29	FMC2_LA02P	H7
A30	FMC2_LA02N	H8
B32	FMC2_LA03P	G9
A32	FMC2_LA03N	G10
B28	FMC2_LA04P	H10
A28	FMC2_LA04N	H11
B30	FMC2_LA05P	D11
B31	FMC2_LA05N	D12
B27	FMC2_LA06P	C10
A27	FMC2_LA06N	C11
C30	FMC2_LA07P	H13
C31	FMC2_LA07N	H14
E27	FMC2_LA08P	G12
D27	FMC2_LA08N	G13
D29	FMC2_LA09P	D14
C29	FMC2_LA09N	D15
F27	FMC2_LA10P	C14
F28	FMC2_LA10N	C15
F29	FMC2_LA11P	H16
E29	FMC2_LA11N	H17
J27	FMC2_LA12P	G15
J28	FMC2_LA12N	G16
K29	FMC2_LA13P	D17
J29	FMC2_LA13N	D18
K26	FMC2_LA14P	C18
J26	FMC2_LA14N	C19
L25	FMC2_LA15P	H19
K25	FMC2_LA15N	H20
M27	FMC2_LA16P	G18
M28	FMC2_LA16N	G19
F23	FMC2_LA17_CCP	D20
F24	FMC2_LA17_CCN	D21
H26	FMC2_LA18_CCP	C22

Table 1-22: **FMC2 HPC Connections at JA3 *(Cont'd)***

RFSoC (U1) Pin	Net Name	FMC Pin
G26	FMC2_LA18_CCN	C23
A22	FMC2_LA19P	H22
A23	FMC2_LA19N	H23
A24	FMC2_LA20P	G21
A25	FMC2_LA20N	G22
B22	FMC2_LA21P	H25
B23	FMC2_LA21N	H26
C25	FMC2_LA22P	G24
B25	FMC2_LA22N	G25
D24	FMC2_LA23P	D23
C24	FMC2_LA23N	D24
C26	FMC2_LA24P	H28
B26	FMC2_LA24N	H29
D23	FMC2_LA25P	G27
C23	FMC2_LA25N	G28
E26	FMC2_LA26P	D26
D26	FMC2_LA26N	D27
E22	FMC2_LA27P	C26
D22	FMC2_LA27N	C27
G25	FMC2_LA28P	H31
F25	FMC2_LA28N	H32
G22	FMC2_LA29P	G30
F22	FMC2_LA29N	G31
H24	FMC2_LA30P	H34
H25	FMC2_LA30N	H35
H23	FMC2_LA31P	G33
G23	FMC2_LA31N	G34
K24	FMC2_LA32P	H37
J24	FMC2_LA32N	H38
K22	FMC2_LA33P	G36
J22	FMC2_LA33N	G37
AL20	FMC2_PRSNT_M2C_L	H2

Table 1-23: **FMC3 HPC Connections at JA4**

RFSoC (U1) Pin	Net Name	FMC Pin
AV9	FMC3_CLK0_M2C_P	H4
AW9	FMC3_CLK0_M2C_N	H5
AV11	FMC3_CLK1_M2C_P	G2
AW11	FMC3_CLK1_M2C_N	G3
A13	FMC3_CLK2_BIDIR_P	K4
A12	FMC3_CLK2_BIDIR_N	K5
F15	FMC3_CLK3_BIDIR_P	J2
E14	FMC3_CLK3_BIDIR_N	J3
AU12	FMC3_LA00_CCP	G6
AU11	FMC3_LA00_CCN	G7
AU10	FMC3_LA01_CCP	D8
AV10	FMC3_LA01_CCN	D9
AP11	FMC3_LA02P	H7
AP10	FMC3_LA02N	H8
AP12	FMC3_LA03P	G9
AR11	FMC3_LA03N	G10
AR10	FMC3_LA04P	H10
AT10	FMC3_LA04N	H11
AR12	FMC3_LA05P	D11
AT12	FMC3_LA05N	D12
AY11	FMC3_LA06P	C10
AY10	FMC3_LA06N	C11
AY9	FMC3_LA07P	H13
BA9	FMC3_LA07N	H14
BA10	FMC3_LA08P	G12
BB9	FMC3_LA08N	G13
BB11	FMC3_LA09P	D14
BB10	FMC3_LA09N	D15
F14	FMC3_LA10P	C14
F13	FMC3_LA10N	C15
A15	FMC3_LA11P	H16
A14	FMC3_LA11N	H17
D16	FMC3_LA12P	G15
C16	FMC3_LA12N	G16
E16	FMC3_LA13P	D17

Table 1-23: **FMC3 HPC Connections at JA4 *(Cont'd)***

RFSoC (U1) Pin	Net Name	FMC Pin
E15	FMC3_LA13N	D18
B16	FMC3_LA14P	C18
B15	FMC3_LA14N	C19
C15	FMC3_LA15P	H19
C14	FMC3_LA15N	H20
B13	FMC3_LA16P	G18
B12	FMC3_LA16N	G19
J16	FMC3_LA17_CCP	D20
H16	FMC3_LA17_CCN	D21
K17	FMC3_LA18_CCP	C22
K16	FMC3_LA18_CCN	C23
G16	FMC3_LA19P	H22
G15	FMC3_LA19N	H23
H15	FMC3_LA20P	G21
H14	FMC3_LA20N	G22
H13	FMC3_LA21P	H25
G13	FMC3_LA21N	H26
J14	FMC3_LA22P	G24
J13	FMC3_LA22N	G25
K15	FMC3_LA23P	D23
K14	FMC3_LA23N	D24
L14	FMC3_LA24P	H28
K15	FMC3_LA24N	H29
M17	FMC3_LA25P	G27
L17	FMC3_LA25N	G28
N14	FMC3_LA26P	D26
M14	FMC3_LA26N	D27
N15	FMC3_LA27P	C26
M15	FMC3_LA27N	C27
N16	FMC3_LA28P	H31
M16	FMC3_LA28N	H32
D9	FMC3_LA29P	G30
C9	FMC3_LA29N	G31
E11	FMC3_LA30P	H34
D11	FMC3_LA30N	H35

Table 1-23: **FMC3 HPC Connections at JA4 *(Cont'd)***

RFSoC (U1) Pin	Net Name	FMC Pin
E10	FMC3_LA31P	G33
E9	FMC3_LA31N	G34
F10	FMC3_LA32P	H37
F9	FMC3_LA32N	H38
G12	FMC3_LA33P	G36
G11	FMC3_LA33N	G37
C13	FMC3_PRSNT_M2C_L	H2

System Controller

The ZCU1275 board uses a Xilinx XC7Z010-CLG225 Zynq-7000 SoC System Controller U38 that can be used to:

- Select the output frequencies of the SuperClock2 Module
- Select the output frequencies of the SuperClock-RF2 Module
- Monitor the onboard power system (PMBus)

See Appendix D, System Controller for information on the System Controller menu options.

System Controller Reset

The SYS_POR pushbutton SW4 (callout 10, Figure 1-2) asserts the System Controller's active-Low power-on-reset signal. When SYS_POR is reasserted, the System Controller is reconfigured from the design stored on its dedicated Quad SPI flash memory.

System Controller Status LEDs

DS1, DS12, DS16, and DS27 (callout 10, Figure 1-2) enunciate the System Controller's INIT_B, DONE, STATUS, and ERROR status, respectively.

I2C Bus Management

The I2C bus is routed through U22, an 8-channel I2C-bus multiplexer (NXP Semiconductor TCA9548A). The I2C address of the multiplexer is `0x75`. The multiplexer routes I2C/PMBus communication between the bus master (System Controller or RFSoC) and eight sub-systems:

- Onboard regulators and power monitoring for RFSoC logic, processor, and transceivers
- Onboard regulators and power monitoring for RF data converters
- SuperClock-2 Module
- SuperClock-RF2 Module
- System Controller EEPROM
- FMC1 connector (not populated)
- FMC2 connector
- FMC3 connector

Table 1-24 shows I2C channel assignments.

Table 1-24: **I2C Channel Assignments**

U22 Channel	I2C Component
0	RFSoC and serial transceiver regulators and power monitoring bus (PMBus)
1	SuperClock-2 Module
2	System Controller EEPROM
3	FMC1 (N/A)
4	FMC2
5	RF data converter regulators and power monitoring bus (PMBus)
6	SuperClock-RF2 Module
7	FMC3

The upstream port of the multiplexer connects to two pairs of PCA9306 bidirectional I2C/PMBus level translators (U46, U53, U55, and U58 in Figure 1-18). J121 and J125 (callout 13, Figure 1-2) are used to enable or disable the bus repeaters and isolate the System Controller or the RFSoC I2C bus.

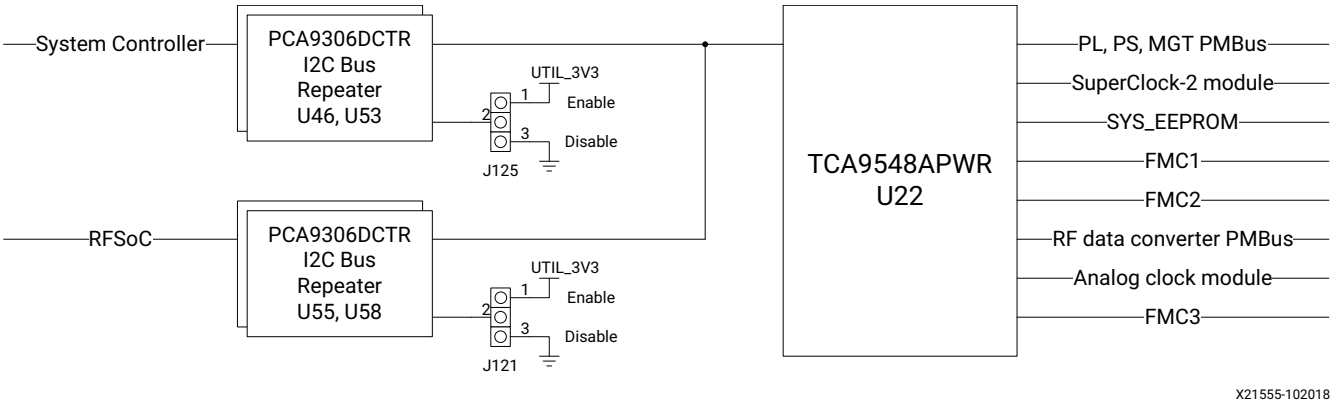

Figure 1-18: **I2C Bus Multiplexer and Upstream Repeater**

USB to Quad-UART Bridge

A USB to Quad-UART bridge (U32, Silicon Laboratories CP2108) is used for simultaneous serial communication between a host terminal (115200-8-N-1) and the RFSoC PL and PS, and the System Controller. The onboard USB Micro-B receptacle USB connector J1 (callout 5, Figure 1-2) is connected to the quad-UART bridge.

Each UART port has four signals: transmit (TX), receive (RX), request-to-send (RTS), and clear-to-send (CTS). RTS and CTS are only connected on the UART interface 0 port and are not connected on the other two ports.

The UART ports are connected as follows:

- UART interface 0 is connected to RFSoC bank 66.
- UART interface 1 is connected to the System Controller.
- UART interface 2 is connected to RFSoC bank 501.
- UART interface 3 is not connected.

Silicon Labs provides royalty-free virtual COM port (VCP) drivers for the host computer. These drivers permit the CP2108 to appear as four COM ports to communications application software (for example, Tera Term or Hyper Terminal) that runs on the host computer.

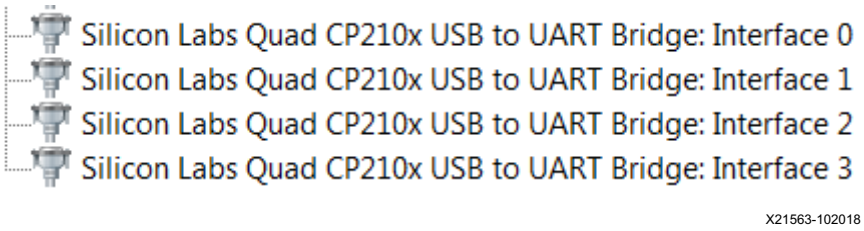

Figure 1-19: **Silicon Labs USB-to-UART Bridge Standard COM Port**

IMPORTANT: *Install the VCP device drivers on the host PC before establishing communications with the ZCU1275 board.*

The connections between the RFSoC PL bank 66 and the Silicon Labs CP2108 are listed in Table 1-25.

Table 1-25: **RFSoC PL to UART Connection**

RFSoC (U1)				Schematic Net Name	Device (U32)		
Pin	Function	Direction	IOSTANDARD		Pin	Function	Direction
BB25	RTS	OUTPUT	LVCMOS18	UART_CTS_I_B	54	CTS	INPUT
BA25	CTS	INPUT	LVCMOS18	UART_RTS_O_B	55	RTS	OUTPUT
BB23	TX	OUTPUT	LVCMOS18	UART_TXD_O	56	RX	INPUT
BB22	RX	INPUT	LVCMOS18	UART_RXD_I	57	TX	OUTPUT

The Silicon Labs CP2108 also provides as many as four user-defined GPIO signals for status and control information (Table 1-26).

Table 1-26: **CP2108 USB-to-UART Bridge User GPIO**

RFSoC (U1)				Schematic Net Name	Device (U32)		
Pin	Function	Direction	IOSTANDARD		Pin	Function	Direction
AY25	SelectIO	IN/OUT	LVCMOS18	UART_GPIO_0	41	GPIO	IN/OUT
AY24	SelectIO	IN/OUT	LVCMOS18	UART_GPIO_1	40	GPIO	IN/OUT
BA24	SelectIO	IN/OUT	LVCMOS18	UART_GPIO_2	38	GPIO	IN/OUT
BA23	SelectIO	IN/OUT	LVCMOS18	UART_GPIO_3	37	GPIO	IN/OUT

The connections between the RFSoC processor and the Silicon Labs CP2108 are listed in Table 1-27. This connection is a UART 0 controller on the processor.

Table 1-27: **RFSoC PS to UART Connection**

RFSoC (U1)				Schematic Net Name	Device (U32)		
Pin	Function	Direction	IOSTANDARD		Pin	Function	Direction
C33	MIO35	TX	OUTPUT	MIO35_UART_TX	15	RX	INPUT
D31	MIO34	RX	INPUT	MIO34_UART_RX	16	TX	OUTPUT

The second port of the CP2108 USB to Quad-UART is connected to the onboard System Controller. See Appendix D, System Controller.

Default Jumper and Switch Positions

A list of jumpers and switches and their required positions for normal board operation is provided in Appendix A, Default Jumper Settings.

Active Heat Sink and Power Connector

An active heat sink (Figure 1-20) is provided for the RFSoC. A 12V fan is affixed to the heat sink and is powered from the 3-pin friction lock header J99 (callout 19, Figure 1-2).

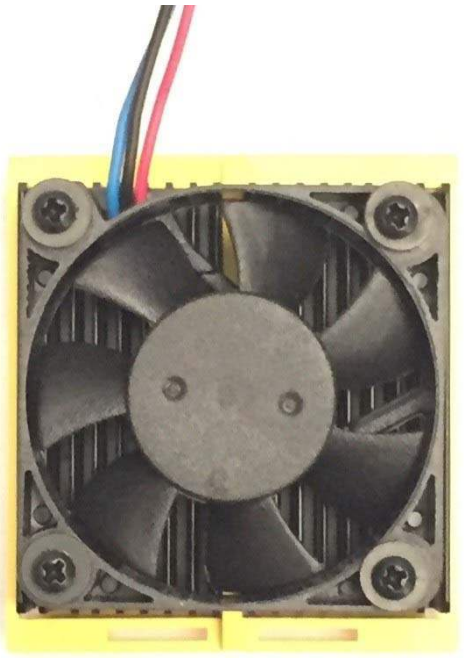

Figure 1-20: **Active Heat Sink**

The fan power connections are listed in Table 1-28.

Table 1-28: **Fan Power Connections**

Fan Wire	Header Pin
Black	J99.1 - FAN_NEG
Red	J99.2 - VCC12_SW
Blue	J99.3 - NC

Figure 1-21 shows the heat sink fan power connector J99.

Figure 1-21: **Heat Sink Fan Power Connector J99**

Default Jumper Settings

Table A-1 lists the jumpers that must be installed on the ZCU1275 board for proper operation. These jumpers must be installed except where specifically noted in this user guide.

IMPORTANT: *Any jumper not listed in Table A-1 should be left open for normal operation.*

Table A-1: **Default Jumper Settings**

Reference Designator	Name	Board Location	Jumper/DIP-Switch Position	Comments
SW2.2	VCCINT	Upper left	ENABLED	
SW2.3	VCCAUX	Upper left	ENABLED	
SW2.4	VCCBRAM	Upper left	ENABLED	
SW2.5	VCCO_HP	Upper left	ENABLED	
SW2.6	VCCO_HD	Upper left	ENABLED	
SW2.7	VCCPINT	Upper left	ENABLED	
SW2.8	VCCPAUX	Upper left	ENABLED	
SW2.9	VCC_PSPLL	Upper left	ENABLED	
SW2.10	VCCO_DDR	Upper left	ENABLED	
SW2.11	VCCO_MIO	Upper left	ENABLED	
SW2.12	VCCINT_AMS	Upper left	ENABLED	
J87	GTY PMBUS CTRL	Upper left	GND (2-3)	
J215	PMBUS CTRL	Center Left	GND (2-3)	
J40	POR_OVERRIDE	Center middle	GND (2-3)	
J121	DUT I2C	Upper right	GND (2-3) DIS	Disabled
J125	SYS I2C	Upper right	PWR (1-2) EN	Enabled
J154	GTY PMBUS ISO	Upper right	Installed	
J8	PMBUS ISO	Upper right	Installed	
J165	PS Mode Pin 0	Upper right	GND (2-3)	JTAG mode
J166	PS Mode Pin 1	Upper right	GND (2-3)	JTAG mode
J164	PS Mode Pin 2	Upper right	GND (2-3)	JTAG mode
J163	PS Mode Pin 3	Upper right	GND (2-3)	JTAG mode
J275	VTT_HP SOURCE	Upper right	VTT_HP (1-2)	

Table A-1: **Default Jumper Settings *(Cont'd)***

Reference Designator	Name	Board Location	Jumper/DIP-Switch Position	Comments
J216	VTT_HD SOURCE	Lower Right	VTT_HD (1-2)	
J60	APM PMBUS CTRL	Center Right	Installed	
J11	CLK_DIFF_1_P	Lower Middle	Installed	
J12	CLK_DIFF_1_N	Lower Middle	Installed	
J13	CLK_DIFF_2_P	Lower Middle	Installed	
J14	CLK_DIFF_2_N	Lower Middle	Installed	

VITA 57.1 FMC Connector Pinouts

Figure B-1 provides a cross-reference of signal names to pin coordinates for the VITA 57.1 FMC high pin count (HPC) connector.

Table B-1: **FMC HPC Connector Pinout**

	K	J	H	G	F	E	D	C	B	A
1	VREF_B_M2C	GND	VREF_A_M2C	GND	PG_M2C	GND	PG_C2M	GND	RES1	GND
2	GND	CLK3_M2C_P	PRSNT_M2C_L	CLK1_M2C_P	GND	HA01_P_CC	GND	DP0_C2M_P	GND	DP1_M2C_P
3	GND	CLK3_M2C_N	GND	CLK1_M2C_N	GND	HA01_N_CC	GND	DP0_C2M_N	GND	DP1_M2C_N
4	CLK2_M2C_P	GND	CLK0_M2C_P	GND	HA00_P_CC	GND	GBTCLK0_M2C_P	GND	DP9_M2C_P	GND
5	CLK2_M2C_N	GND	CLK0_M2C_N	GND	HA00_N_CC	GND	GBTCLK0_M2C_N	GND	DP9_M2C_N	GND
6	GND	HA03_P	GND	LA00_P_CC	GND	HA05_P	GND	DP0_M2C_P	GND	DP2_M2C_P
7	HA02_P	HA03_N	LA02_P	LA00_N_CC	HA04_P	HA05_N	GND	DP0_M2C_N	GND	DP2_M2C_N
8	HA02_N	GND	LA02_N	GND	HA04_N	GND	LA01_P_CC	GND	DP8_M2C_P	GND
9	GND	HA07_P	GND	LA03_P	GND	HA09_P	LA01_N_CC	GND	DP8_M2C_N	GND
10	HA06_P	HA07_N	LA04_P	LA03_N	HA08_P	HA09_N	GND	LA06_P	GND	DP3_M2C_P
11	HA06_N	GND	LA04_N	GND	HA08_N	GND	LA05_P	LA06_N	GND	DP3_M2C_N
12	GND	HA11_P	GND	LA08_P	GND	HA13_P	LA05_N	GND	DP7_M2C_P	GND
13	HA10_P	HA11_N	LA07_P	LA08_N	HA12_P	HA13_N	GND	GND	DP7_M2C_N	GND
14	HA10_N	GND	LA07_N	GND	HA12_N	GND	LA09_P	LA10_P	GND	DP4_M2C_P
15	GND	HA14_P	GND	LA12_P	GND	HA16_P	LA09_N	LA10_N	GND	DP4_M2C_N
16	HA17_P_CC	HA14_N	LA11_P	LA12_N	HA15_P	HA16_N	GND	GND	DP6_M2C_P	GND
17	HA17_N_CC	GND	LA11_N	GND	HA15_N	GND	LA13_P	GND	DP6_M2C_N	GND
18	GND	HA18_P	GND	LA16_P	GND	HA20_P	LA13_N	LA14_P	GND	DP5_M2C_P
19	HA21_P	HA18_N	LA15_P	LA16_N	HA19_P	HA20_N	GND	LA14_N	GND	DP5_M2C_N
20	HA21_N	GND	LA15_N	GND	HA19_N	GND	LA17_P_CC	GND	GBTCLK1_M2C_P	GND
21	GND	HA22_P	GND	LA20_P	GND	HB03_P	LA17_N_CC	GND	GBTCLK1_M2C_N	GND
22	HA23_P	HA22_N	LA19_P	LA20_N	HB02_P	HB03_N	GND	LA18_P_CC	GND	DP1_C2M_P
23	HA23_N	GND	LA19_N	GND	HB02_N	GND	LA23_P	LA18_N_CC	GND	DP1_C2M_N
24	GND	HB01_P	GND	LA22_P	GND	HB05_P	LA23_N	GND	DP9_C2M_P	GND
25	HB00_P_CC	HB01_N	LA21_P	LA22_N	HB04_P	HB05_N	GND	GND	DP9_C2M_N	GND
26	HB00_N_CC	GND	LA21_N	GND	HB04_N	GND	LA26_P	LA27_P	GND	DP2_C2M_P
27	GND	HB07_P	GND	LA25_P	GND	HB09_P	LA26_N	LA27_N	GND	DP2_C2M_N
28	HB06_P_CC	HB07_N	LA24_P	LA25_N	HB08_P	HB09_N	GND	GND	DP8_C2M_P	GND
29	HB06_N_CC	GND	LA24_N	GND	HB08_N	GND	TCK	GND	DP8_C2M_N	GND
30	GND	HB11_P	GND	LA29_P	GND	HB13_P	TDI	SCL	GND	DP3_C2M_P
31	HB10_P	HB11_N	LA28_P	LA29_N	HB12_P	HB13_N	TDO	SDA	GND	DP3_C2M_N
32	HB10_N	GND	LA28_N	GND	HB12_N	GND	3P3VAUX	GND	DP7_C2M_P	GND

Table B-1: **FMC HPC Connector Pinout *(Cont'd)***

	K	J	H	G	F	E	D	C	B	A
33	GND	HB15_P	GND	LA31_P	GND	HB19_P	TMS	GND	DP7_C2M_N	GND
34	HB14_P	HB15_N	LA30_P	LA31_N	HB16_P	HB19_N	TRST_L	GA0	GND	DP4_C2M_P
35	HB14_N	GND	LA30_N	GND	HB16_N	GND	GA1	12P0V	GND	DP4_C2M_N
36	GND	HB18_P	GND	LA33_P	GND	HB21_P	3P3V	GND	DP6_C2M_P	GND
37	HB17_P_CC	HB18_N	LA32_P	LA33_N	HB20_P	HB21_N	GND	12P0V	DP6_C2M_N	GND
38	HB17_N_CC	GND	LA32_N	GND	HB20_N	GND	3P3V	GND	GND	DP5_C2M_P
39	GND	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	DP5_C2M_N
40	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	RES0	GND

Master Constraints File Listing

The Xilinx design constraints (XDC) file template for the ZCU1275 board provides for designs targeting the Zynq® UltraScale+™ RFSoC ZCU1275 characterization kit. Net names in the listed constraints correlate with net names on the ZCU1275 board schematic. Identify the appropriate pins and replace the following net names with net names in the user RTL. See the *Vivado Design Suite User Guide: Using Constraints* (UG903) [Ref 8] for more information.

ZCU1275 Board XDC Listing

```
#FMC2
set_property PACKAGE_PIN AL20     [get_ports "FMC2_PRSNT_M2C_L"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_PRSNT_M2C_L"]
set_property PACKAGE_PIN H29      [get_ports "FMC2_CLK0_M2C_N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_CLK0_M2C_N"]
set_property PACKAGE_PIN H28      [get_ports "FMC2_CLK0_M2C_P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_CLK0_M2C_P"]
set_property PACKAGE_PIN G30      [get_ports "FMC2_CLK1_M2C_N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_CLK1_M2C_N"]
set_property PACKAGE_PIN H30      [get_ports "FMC2_CLK1_M2C_P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_CLK1_M2C_P"]
set_property PACKAGE_PIN AR26     [get_ports "FMC2_CLK2_BIDIR_N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_CLK2_BIDIR_N"]
set_property PACKAGE_PIN AP26     [get_ports "FMC2_CLK2_BIDIR_P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_CLK2_BIDIR_P"]
set_property PACKAGE_PIN AT24     [get_ports "FMC2_CLK3_BIDIR_N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_CLK3_BIDIR_N"]
set_property PACKAGE_PIN AT23     [get_ports "FMC2_CLK3_BIDIR_P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_CLK3_BIDIR_P"]
#FMC2 LA
set_property PACKAGE_PIN G28      [get_ports "FMC2_LA00_CCN"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA00_CCN"]
set_property PACKAGE_PIN G27      [get_ports "FMC2_LA00_CCP"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA00_CCP"]
set_property PACKAGE_PIN E30      [get_ports "FMC2_LA01_CCN"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA01_CCN"]
set_property PACKAGE_PIN F30      [get_ports "FMC2_LA01_CCP"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA01_CCP"]
set_property PACKAGE_PIN A30      [get_ports "FMC2_LA02N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA02N"]
set_property PACKAGE_PIN A29      [get_ports "FMC2_LA02P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA02P"]
set_property PACKAGE_PIN A32      [get_ports "FMC2_LA03N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA03N"]
```

```
set_property PACKAGE_PIN B32      [get_ports "FMC2_LA03P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA03P"]
set_property PACKAGE_PIN A28      [get_ports "FMC2_LA04N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA04N"]
set_property PACKAGE_PIN B28      [get_ports "FMC2_LA04P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA04P"]
set_property PACKAGE_PIN B31      [get_ports "FMC2_LA05N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA05N"]
set_property PACKAGE_PIN B30      [get_ports "FMC2_LA05P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA05P"]
set_property PACKAGE_PIN A27      [get_ports "FMC2_LA06N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA06N"]
set_property PACKAGE_PIN B27      [get_ports "FMC2_LA06P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA06P"]
set_property PACKAGE_PIN C31      [get_ports "FMC2_LA07N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA07N"]
set_property PACKAGE_PIN C30      [get_ports "FMC2_LA07P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA07P"]
set_property PACKAGE_PIN D27      [get_ports "FMC2_LA08N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA08N"]
set_property PACKAGE_PIN E27      [get_ports "FMC2_LA08P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA08P"]
set_property PACKAGE_PIN C29      [get_ports "FMC2_LA09N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA09N"]
set_property PACKAGE_PIN D29      [get_ports "FMC2_LA09P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA09P"]
set_property PACKAGE_PIN F28      [get_ports "FMC2_LA10N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA10N"]
set_property PACKAGE_PIN F27      [get_ports "FMC2_LA10P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA10P"]
set_property PACKAGE_PIN E29      [get_ports "FMC2_LA11N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA11N"]
set_property PACKAGE_PIN F29      [get_ports "FMC2_LA11P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA11P"]
set_property PACKAGE_PIN J28      [get_ports "FMC2_LA12N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA12N"]
set_property PACKAGE_PIN J27      [get_ports "FMC2_LA12P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA12P"]
set_property PACKAGE_PIN J29      [get_ports "FMC2_LA13N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA13N"]
set_property PACKAGE_PIN K29      [get_ports "FMC2_LA13P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA13P"]
set_property PACKAGE_PIN J26      [get_ports "FMC2_LA14N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA14N"]
set_property PACKAGE_PIN K26      [get_ports "FMC2_LA14P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA14P"]
set_property PACKAGE_PIN K25      [get_ports "FMC2_LA15N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA15N"]
set_property PACKAGE_PIN L25      [get_ports "FMC2_LA15P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA15P"]
set_property PACKAGE_PIN M28      [get_ports "FMC2_LA16N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA16N"]
set_property PACKAGE_PIN M27      [get_ports "FMC2_LA16P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA16P"]
set_property PACKAGE_PIN F24      [get_ports "FMC2_LA17_CCN"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA17_CCN"]
set_property PACKAGE_PIN F23      [get_ports "FMC2_LA17_CCP"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA17_CCP"]
set_property PACKAGE_PIN G26      [get_ports "FMC2_LA18_CCN"]
```

```
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA18_CCN"]
set_property PACKAGE_PIN H26      [get_ports "FMC2_LA18_CCP"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA18_CCP"]
set_property PACKAGE_PIN A23      [get_ports "FMC2_LA19N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA19N"]
set_property PACKAGE_PIN A22      [get_ports "FMC2_LA19P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA19P"]
set_property PACKAGE_PIN A25      [get_ports "FMC2_LA20N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA20N"]
set_property PACKAGE_PIN A24      [get_ports "FMC2_LA20P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA20P"]
set_property PACKAGE_PIN B23      [get_ports "FMC2_LA21N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA21N"]
set_property PACKAGE_PIN B22      [get_ports "FMC2_LA21P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA21P"]
set_property PACKAGE_PIN B25      [get_ports "FMC2_LA22N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA22N"]
set_property PACKAGE_PIN C25      [get_ports "FMC2_LA22P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA22P"]
set_property PACKAGE_PIN C24      [get_ports "FMC2_LA23N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA23N"]
set_property PACKAGE_PIN D24      [get_ports "FMC2_LA23P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA23P"]
set_property PACKAGE_PIN B26      [get_ports "FMC2_LA24N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA24N"]
set_property PACKAGE_PIN C26      [get_ports "FMC2_LA24P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA24P"]
set_property PACKAGE_PIN C23      [get_ports "FMC2_LA25N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA25N"]
set_property PACKAGE_PIN D23      [get_ports "FMC2_LA25P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA25P"]
set_property PACKAGE_PIN D26      [get_ports "FMC2_LA26N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA26N"]
set_property PACKAGE_PIN E26      [get_ports "FMC2_LA26P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA26P"]
set_property PACKAGE_PIN D22      [get_ports "FMC2_LA27N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA27N"]
set_property PACKAGE_PIN E22      [get_ports "FMC2_LA27P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA27P"]
set_property PACKAGE_PIN F25      [get_ports "FMC2_LA28N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA28N"]
set_property PACKAGE_PIN G25      [get_ports "FMC2_LA28P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA28P"]
set_property PACKAGE_PIN F22      [get_ports "FMC2_LA29N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA29N"]
set_property PACKAGE_PIN G22      [get_ports "FMC2_LA29P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA29P"]
set_property PACKAGE_PIN H25      [get_ports "FMC2_LA30N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA30N"]
set_property PACKAGE_PIN H24      [get_ports "FMC2_LA30P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA30P"]
set_property PACKAGE_PIN G23      [get_ports "FMC2_LA31N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA31N"]
set_property PACKAGE_PIN H23      [get_ports "FMC2_LA31P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA31P"]
set_property PACKAGE_PIN J24      [get_ports "FMC2_LA32N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA32N"]
set_property PACKAGE_PIN K24      [get_ports "FMC2_LA32P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA32P"]
```

```
set_property PACKAGE_PIN J22      [get_ports "FMC2_LA33N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA33N"]
set_property PACKAGE_PIN K22      [get_ports "FMC2_LA33P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_LA33P"]
#FMC2 HA
set_property PACKAGE_PIN AP17     [get_ports "FMC2_HA00_CCN"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HA00_CCN"]
set_property PACKAGE_PIN AP18     [get_ports "FMC2_HA00_CCP"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HA00_CCP"]
set_property PACKAGE_PIN AN20     [get_ports "FMC2_HA01_CCN"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HA01_CCN"]
set_property PACKAGE_PIN AN21     [get_ports "FMC2_HA01_CCP"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HA01_CCP"]
set_property PACKAGE_PIN AH19     [get_ports "FMC2_HA02N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HA02N"]
set_property PACKAGE_PIN AH20     [get_ports "FMC2_HA02P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HA02P"]
set_property PACKAGE_PIN AJ21     [get_ports "FMC2_HA03N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HA03N"]
set_property PACKAGE_PIN AH21     [get_ports "FMC2_HA03P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HA03P"]
set_property PACKAGE_PIN AJ18     [get_ports "FMC2_HA04N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HA04N"]
set_property PACKAGE_PIN AH18     [get_ports "FMC2_HA04P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HA04P"]
set_property PACKAGE_PIN AK20     [get_ports "FMC2_HA05N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HA05N"]
set_property PACKAGE_PIN AK21     [get_ports "FMC2_HA05P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HA05P"]
set_property PACKAGE_PIN AK17     [get_ports "FMC2_HA06N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HA06N"]
set_property PACKAGE_PIN AJ17     [get_ports "FMC2_HA06P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HA06P"]
set_property PACKAGE_PIN AL19     [get_ports "FMC2_HA07N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HA07N"]
set_property PACKAGE_PIN AK19     [get_ports "FMC2_HA07P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HA07P"]
set_property PACKAGE_PIN AL17     [get_ports "FMC2_HA08N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HA08N"]
set_property PACKAGE_PIN AL18     [get_ports "FMC2_HA08P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HA08P"]
set_property PACKAGE_PIN AM20     [get_ports "FMC2_HA09N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HA09N"]
set_property PACKAGE_PIN AM21     [get_ports "FMC2_HA09P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HA09P"]
set_property PACKAGE_PIN AN18     [get_ports "FMC2_HA10N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HA10N"]
set_property PACKAGE_PIN AM18     [get_ports "FMC2_HA10P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HA10P"]
set_property PACKAGE_PIN AP19     [get_ports "FMC2_HA11N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HA11N"]
set_property PACKAGE_PIN AN19     [get_ports "FMC2_HA11P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HA11P"]
set_property PACKAGE_PIN AR21     [get_ports "FMC2_HA12N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HA12N"]
set_property PACKAGE_PIN AP21     [get_ports "FMC2_HA12P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HA12P"]
set_property PACKAGE_PIN AT19     [get_ports "FMC2_HA13N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HA13N"]
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```
set_property PACKAGE_PIN AT20     [get_ports "FMC2_HA13P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HA13P"]
set_property PACKAGE_PIN AU20     [get_ports "FMC2_HA14N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HA14N"]
set_property PACKAGE_PIN AU21     [get_ports "FMC2_HA14P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HA14P"]
set_property PACKAGE_PIN AU18     [get_ports "FMC2_HA15N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HA15N"]
set_property PACKAGE_PIN AT18     [get_ports "FMC2_HA15P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HA15P"]
set_property PACKAGE_PIN AY21     [get_ports "FMC2_HA16N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HA16N"]
set_property PACKAGE_PIN AW21     [get_ports "FMC2_HA16P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HA16P"]
set_property PACKAGE_PIN AR19     [get_ports "FMC2_HA17_CCN"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HA17_CCN"]
set_property PACKAGE_PIN AR20     [get_ports "FMC2_HA17_CCP"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HA17_CCP"]
set_property PACKAGE_PIN AW19     [get_ports "FMC2_HA18N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HA18N"]
set_property PACKAGE_PIN AV19     [get_ports "FMC2_HA18P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HA18P"]
set_property PACKAGE_PIN BA20     [get_ports "FMC2_HA19N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HA19N"]
set_property PACKAGE_PIN AY20     [get_ports "FMC2_HA19P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HA19P"]
set_property PACKAGE_PIN AW18     [get_ports "FMC2_HA20N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HA20N"]
set_property PACKAGE_PIN AV18     [get_ports "FMC2_HA20P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HA20P"]
set_property PACKAGE_PIN BA19     [get_ports "FMC2_HA21N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HA21N"]
set_property PACKAGE_PIN AY19     [get_ports "FMC2_HA21P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HA21P"]
set_property PACKAGE_PIN BB18     [get_ports "FMC2_HA22N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HA22N"]
set_property PACKAGE_PIN BA18     [get_ports "FMC2_HA22P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HA22P"]
set_property PACKAGE_PIN BB20     [get_ports "FMC2_HA23N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HA23N"]
set_property PACKAGE_PIN BB21     [get_ports "FMC2_HA23P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HA23P"]
#FMC2 HB
set_property PACKAGE_PIN AU15     [get_ports "FMC2_HB00_CCN"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HB00_CCN"]
set_property PACKAGE_PIN AT15     [get_ports "FMC2_HB00_CCP"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HB00_CCP"]
set_property PACKAGE_PIN AK14     [get_ports "FMC2_HB01N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HB01N"]
set_property PACKAGE_PIN AJ14     [get_ports "FMC2_HB01P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HB01P"]
set_property PACKAGE_PIN AK15     [get_ports "FMC2_HB02N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HB02N"]
set_property PACKAGE_PIN AK16     [get_ports "FMC2_HB02P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HB02P"]
set_property PACKAGE_PIN AM15     [get_ports "FMC2_HB03N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HB03N"]
set_property PACKAGE_PIN AL15     [get_ports "FMC2_HB03P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HB03P"]
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```
set_property PACKAGE_PIN AN15     [get_ports "FMC2_HB04N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HB04N"]
set_property PACKAGE_PIN AM16     [get_ports "FMC2_HB04P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HB04P"]
set_property PACKAGE_PIN AM13     [get_ports "FMC2_HB05N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HB05N"]
set_property PACKAGE_PIN AL14     [get_ports "FMC2_HB05P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HB05P"]
set_property PACKAGE_PIN AU16     [get_ports "FMC2_HB06_CCN"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HB06_CCN"]
set_property PACKAGE_PIN AU17     [get_ports "FMC2_HB06_CCP"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HB06_CCP"]
set_property PACKAGE_PIN AP16     [get_ports "FMC2_HB07N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HB07N"]
set_property PACKAGE_PIN AN16     [get_ports "FMC2_HB07P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HB07P"]
set_property PACKAGE_PIN AP13     [get_ports "FMC2_HB08N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HB08N"]
set_property PACKAGE_PIN AN13     [get_ports "FMC2_HB08P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HB08P"]
set_property PACKAGE_PIN AR15     [get_ports "FMC2_HB09N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HB09N"]
set_property PACKAGE_PIN AR16     [get_ports "FMC2_HB09P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HB09P"]
set_property PACKAGE_PIN AT14     [get_ports "FMC2_HB10N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HB10N"]
set_property PACKAGE_PIN AR14     [get_ports "FMC2_HB10P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HB10P"]
set_property PACKAGE_PIN AT17     [get_ports "FMC2_HB11N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HB11N"]
set_property PACKAGE_PIN AR17     [get_ports "FMC2_HB11P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HB11P"]
set_property PACKAGE_PIN AV15     [get_ports "FMC2_HB12N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HB12N"]
set_property PACKAGE_PIN AV16     [get_ports "FMC2_HB12P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HB12P"]
set_property PACKAGE_PIN AW14     [get_ports "FMC2_HB13N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HB13N"]
set_property PACKAGE_PIN AV14     [get_ports "FMC2_HB13P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HB13P"]
set_property PACKAGE_PIN AW16     [get_ports "FMC2_HB14N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HB14N"]
set_property PACKAGE_PIN AW17     [get_ports "FMC2_HB14P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HB14P"]
set_property PACKAGE_PIN AW13     [get_ports "FMC2_HB15N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HB15N"]
set_property PACKAGE_PIN AV13     [get_ports "FMC2_HB15P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HB15P"]
set_property PACKAGE_PIN AY16     [get_ports "FMC2_HB16N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HB16N"]
set_property PACKAGE_PIN AY17     [get_ports "FMC2_HB16P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HB16P"]
set_property PACKAGE_PIN AU13     [get_ports "FMC2_HB17_CCN"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HB17_CCN"]
set_property PACKAGE_PIN AT13     [get_ports "FMC2_HB17_CCP"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HB17_CCP"]
set_property PACKAGE_PIN AY14     [get_ports "FMC2_HB18N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HB18N"]
set_property PACKAGE_PIN AY15     [get_ports "FMC2_HB18P"]
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```
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HB18P"]
set_property PACKAGE_PIN BA14     [get_ports "FMC2_HB19N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HB19N"]
set_property PACKAGE_PIN BA15     [get_ports "FMC2_HB19P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HB19P"]
set_property PACKAGE_PIN BB15     [get_ports "FMC2_HB20N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HB20N"]
set_property PACKAGE_PIN BB16     [get_ports "FMC2_HB20P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HB20P"]
set_property PACKAGE_PIN BA12     [get_ports "FMC2_HB21N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HB21N"]
set_property PACKAGE_PIN BA13     [get_ports "FMC2_HB21P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC2_HB21P"]
#FMC3
set_property PACKAGE_PIN C13      [get_ports "FMC3_PRSNT_M2C_L"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_PRSNT_M2C_L"]
set_property PACKAGE_PIN AW9      [get_ports "FMC3_CLK0_M2C_N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_CLK0_M2C_N"]
set_property PACKAGE_PIN AV9      [get_ports "FMC3_CLK0_M2C_P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_CLK0_M2C_P"]
set_property PACKAGE_PIN AW11     [get_ports "FMC3_CLK1_M2C_N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_CLK1_M2C_N"]
set_property PACKAGE_PIN AV11     [get_ports "FMC3_CLK1_M2C_P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_CLK1_M2C_P"]
set_property PACKAGE_PIN E14      [get_ports "FMC3_CLK2_BIDIR_N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_CLK2_BIDIR_N"]
set_property PACKAGE_PIN F15      [get_ports "FMC3_CLK2_BIDIR_P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_CLK2_BIDIR_P"]
set_property PACKAGE_PIN A12      [get_ports "FMC3_CLK3_BIDIR_N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_CLK3_BIDIR_N"]
set_property PACKAGE_PIN A13      [get_ports "FMC3_CLK3_BIDIR_P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_CLK3_BIDIR_P"]
#FMC3 LA
set_property PACKAGE_PIN AU11     [get_ports "FMC3_LA00_CCN"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA00_CCN"]
set_property PACKAGE_PIN AU12     [get_ports "FMC3_LA00_CCP"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA00_CCP"]
set_property PACKAGE_PIN AV10     [get_ports "FMC3_LA01_CCN"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA01_CCN"]
set_property PACKAGE_PIN AU10     [get_ports "FMC3_LA01_CCP"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA01_CCP"]
set_property PACKAGE_PIN AP10     [get_ports "FMC3_LA02N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA02N"]
set_property PACKAGE_PIN AP11     [get_ports "FMC3_LA02P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA02P"]
set_property PACKAGE_PIN AR11     [get_ports "FMC3_LA03N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA03N"]
set_property PACKAGE_PIN AP12     [get_ports "FMC3_LA03P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA03P"]
set_property PACKAGE_PIN AT10     [get_ports "FMC3_LA04N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA04N"]
set_property PACKAGE_PIN AR10     [get_ports "FMC3_LA04P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA04P"]
set_property PACKAGE_PIN AT12     [get_ports "FMC3_LA05N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA05N"]
set_property PACKAGE_PIN AR12     [get_ports "FMC3_LA05P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA05P"]
set_property PACKAGE_PIN AY10     [get_ports "FMC3_LA06N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA06N"]
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```
set_property PACKAGE_PIN AY11     [get_ports "FMC3_LA06P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA06P"]
set_property PACKAGE_PIN BA9      [get_ports "FMC3_LA07N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA07N"]
set_property PACKAGE_PIN AY9      [get_ports "FMC3_LA07P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA07P"]
set_property PACKAGE_PIN BB9      [get_ports "FMC3_LA08N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA08N"]
set_property PACKAGE_PIN BA10     [get_ports "FMC3_LA08P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA08P"]
set_property PACKAGE_PIN BB10     [get_ports "FMC3_LA09N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA09N"]
set_property PACKAGE_PIN BB11     [get_ports "FMC3_LA09P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA09P"]
set_property PACKAGE_PIN F13      [get_ports "FMC3_LA10N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA10N"]
set_property PACKAGE_PIN F14      [get_ports "FMC3_LA10P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA10P"]
set_property PACKAGE_PIN A14      [get_ports "FMC3_LA11N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA11N"]
set_property PACKAGE_PIN A15      [get_ports "FMC3_LA11P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA11P"]
set_property PACKAGE_PIN C16      [get_ports "FMC3_LA12N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA12N"]
set_property PACKAGE_PIN D16      [get_ports "FMC3_LA12P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA12P"]
set_property PACKAGE_PIN E15      [get_ports "FMC3_LA13N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA13N"]
set_property PACKAGE_PIN E16      [get_ports "FMC3_LA13P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA13P"]
set_property PACKAGE_PIN B15      [get_ports "FMC3_LA14N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA14N"]
set_property PACKAGE_PIN B16      [get_ports "FMC3_LA14P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA14P"]
set_property PACKAGE_PIN C14      [get_ports "FMC3_LA15N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA15N"]
set_property PACKAGE_PIN C15      [get_ports "FMC3_LA15P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA15P"]
set_property PACKAGE_PIN B12      [get_ports "FMC3_LA16N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA16N"]
set_property PACKAGE_PIN B13      [get_ports "FMC3_LA16P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA16P"]
set_property PACKAGE_PIN H16      [get_ports "FMC3_LA17_CCN"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA17_CCN"]
set_property PACKAGE_PIN J16      [get_ports "FMC3_LA17_CCP"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA17_CCP"]
set_property PACKAGE_PIN K16      [get_ports "FMC3_LA18_CCN"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA18_CCN"]
set_property PACKAGE_PIN K17      [get_ports "FMC3_LA18_CCP"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA18_CCP"]
set_property PACKAGE_PIN G15      [get_ports "FMC3_LA19N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA19N"]
set_property PACKAGE_PIN G16      [get_ports "FMC3_LA19P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA19P"]
set_property PACKAGE_PIN H14      [get_ports "FMC3_LA20N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA20N"]
set_property PACKAGE_PIN H15      [get_ports "FMC3_LA20P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA20P"]
set_property PACKAGE_PIN G13      [get_ports "FMC3_LA21N"]
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```
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA21N"]
set_property PACKAGE_PIN H13      [get_ports "FMC3_LA21P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA21P"]
set_property PACKAGE_PIN J13      [get_ports "FMC3_LA22N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA22N"]
set_property PACKAGE_PIN J14      [get_ports "FMC3_LA22P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA22P"]
set_property PACKAGE_PIN K14      [get_ports "FMC3_LA23N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA23N"]
set_property PACKAGE_PIN K15      [get_ports "FMC3_LA23P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA23P"]
set_property PACKAGE_PIN L14      [get_ports "FMC3_LA24N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA24N"]
set_property PACKAGE_PIN L15      [get_ports "FMC3_LA24P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA24P"]
set_property PACKAGE_PIN L17      [get_ports "FMC3_LA25N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA25N"]
set_property PACKAGE_PIN M17      [get_ports "FMC3_LA25P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA25P"]
set_property PACKAGE_PIN M14      [get_ports "FMC3_LA26N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA26N"]
set_property PACKAGE_PIN N14      [get_ports "FMC3_LA26P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA26P"]
set_property PACKAGE_PIN M15      [get_ports "FMC3_LA27N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA27N"]
set_property PACKAGE_PIN N15      [get_ports "FMC3_LA27P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA27P"]
set_property PACKAGE_PIN M16      [get_ports "FMC3_LA28N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA28N"]
set_property PACKAGE_PIN N16      [get_ports "FMC3_LA28P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA28P"]
set_property PACKAGE_PIN C9       [get_ports "FMC3_LA29N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA29N"]
set_property PACKAGE_PIN D9       [get_ports "FMC3_LA29P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA29P"]
set_property PACKAGE_PIN D11      [get_ports "FMC3_LA30N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA30N"]
set_property PACKAGE_PIN E11      [get_ports "FMC3_LA30P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA30P"]
set_property PACKAGE_PIN E9       [get_ports "FMC3_LA31N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA31N"]
set_property PACKAGE_PIN E10      [get_ports "FMC3_LA31P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA31P"]
set_property PACKAGE_PIN F9       [get_ports "FMC3_LA32N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA32N"]
set_property PACKAGE_PIN F10      [get_ports "FMC3_LA32P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA32P"]
set_property PACKAGE_PIN G11      [get_ports "FMC3_LA33N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA33N"]
set_property PACKAGE_PIN G12      [get_ports "FMC3_LA33P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA33P"]
#SUPERCLOCK-2 MODULE
set_property PACKAGE_PIN L29      [get_ports "CM_LVDS1_N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "CM_LVDS1_N"]
set_property PACKAGE_PIN L28      [get_ports "CM_LVDS1_P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "CM_LVDS1_P"]
set_property PACKAGE_PIN H9       [get_ports "CM_LVDS2_N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "CM_LVDS2_N"]
set_property PACKAGE_PIN H10      [get_ports "CM_LVDS2_P"]
```

```
set_property IOSTANDARD  LVCMOS18 [get_ports "CM_LVDS2_P"]
set_property PACKAGE_PIN AR24     [get_ports "CM_GCLK_N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "CM_GCLK_N"]
set_property PACKAGE_PIN AP24     [get_ports "CM_GCLK_P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "CM_GCLK_P"]
#SWITCHES
set_property PACKAGE_PIN AV25     [get_ports "USER_SW1"]
set_property IOSTANDARD  LVCMOS18 [get_ports "USER_SW1"]
set_property PACKAGE_PIN AU25     [get_ports "USER_SW2"]
set_property IOSTANDARD  LVCMOS18 [get_ports "USER_SW2"]
set_property PACKAGE_PIN AV23     [get_ports "USER_SW3"]
set_property IOSTANDARD  LVCMOS18 [get_ports "USER_SW3"]
set_property PACKAGE_PIN AU23     [get_ports "USER_SW4"]
set_property IOSTANDARD  LVCMOS18 [get_ports "USER_SW4"]
set_property PACKAGE_PIN AW24     [get_ports "USER_SW5"]
set_property IOSTANDARD  LVCMOS18 [get_ports "USER_SW5"]
set_property PACKAGE_PIN AV24     [get_ports "USER_SW6"]
set_property IOSTANDARD  LVCMOS18 [get_ports "USER_SW6"]
set_property PACKAGE_PIN BA22     [get_ports "USER_SW7"]
set_property IOSTANDARD  LVCMOS18 [get_ports "USER_SW7"]
set_property PACKAGE_PIN AY22     [get_ports "USER_SW8"]
set_property IOSTANDARD  LVCMOS18 [get_ports "USER_SW8"]
#PUSH BUTTONS
set_property PACKAGE_PIN AM22     [get_ports "USER_PB1"]
set_property IOSTANDARD  LVCMOS18 [get_ports "USER_PB1"]
set_property PACKAGE_PIN AN26     [get_ports "USER_PB2"]
set_property IOSTANDARD  LVCMOS18 [get_ports "USER_PB2"]
#LEDs
set_property PACKAGE_PIN AM25     [get_ports "APP_LED1"]
set_property IOSTANDARD  LVCMOS18 [get_ports "APP_LED1"]
set_property PACKAGE_PIN AL24     [get_ports "APP_LED2"]
set_property IOSTANDARD  LVCMOS18 [get_ports "APP_LED2"]
set_property PACKAGE_PIN AK22     [get_ports "APP_LED3"]
set_property IOSTANDARD  LVCMOS18 [get_ports "APP_LED3"]
set_property PACKAGE_PIN AJ22     [get_ports "APP_LED4"]
set_property IOSTANDARD  LVCMOS18 [get_ports "APP_LED4"]
set_property PACKAGE_PIN AN25     [get_ports "APP_LED5"]
set_property IOSTANDARD  LVCMOS18 [get_ports "APP_LED5"]
set_property PACKAGE_PIN AN24     [get_ports "APP_LED6"]
set_property IOSTANDARD  LVCMOS18 [get_ports "APP_LED6"]
set_property PACKAGE_PIN AM23     [get_ports "APP_LED7"]
set_property IOSTANDARD  LVCMOS18 [get_ports "APP_LED7"]
set_property PACKAGE_PIN AL23     [get_ports "APP_LED8"]
set_property IOSTANDARD  LVCMOS18 [get_ports "APP_LED8"]
#SMAs
set_property PACKAGE_PIN AR26     [get_ports "CLK_DIFF_1_N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "CLK_DIFF_1_N"]
set_property PACKAGE_PIN AP26     [get_ports "CLK_DIFF_1_P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "CLK_DIFF_1_P"]
set_property PACKAGE_PIN AT24     [get_ports "CLK_DIFF_2_N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "CLK_DIFF_2_N"]
set_property PACKAGE_PIN AT23     [get_ports "CLK_DIFF_2_P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "CLK_DIFF_2_P"]
#SYSTEM CLOCK
set_property PACKAGE_PIN AR22     [get_ports "LVDS_OSC_N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "LVDS_OSC_N"]
set_property PACKAGE_PIN AP22     [get_ports "LVDS_OSC_P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "LVDS_OSC_P"]
#USER JTAG
```

```
set_property PACKAGE_PIN AK26     [get_ports "USER_JTAG_TCK"]
set_property IOSTANDARD  LVCMOS18 [get_ports "USER_JTAG_TCK"]
set_property PACKAGE_PIN AJ26     [get_ports "USER_JTAG_TMS"]
set_property IOSTANDARD  LVCMOS18 [get_ports "USER_JTAG_TMS"]
set_property PACKAGE_PIN AL25     [get_ports "USER_JTAG_TDI"]
set_property IOSTANDARD  LVCMOS18 [get_ports "USER_JTAG_TDI"]
set_property PACKAGE_PIN AK25     [get_ports "USER_JTAG_TDO"]
set_property IOSTANDARD  LVCMOS18 [get_ports "USER_JTAG_TDO"]
#PMBUS
set_property PACKAGE_PIN AM26     [get_ports "DUT_PMBUS_CLK"]
set_property IOSTANDARD  LVCMOS18 [get_ports "DUT_PMBUS_CLK"]
set_property PACKAGE_PIN AP23     [get_ports "DUT_PMBUS_DATA"]
set_property IOSTANDARD  LVCMOS18 [get_ports "DUT_PMBUS_DATA"]
set_property PACKAGE_PIN AN23     [get_ports "DUT_PMBUS_ALERT"]
set_property IOSTANDARD  LVCMOS18 [get_ports "DUT_PMBUS_ALERT"]
#UART
set_property PACKAGE_PIN BB23     [get_ports "UART_TXD_O"]
set_property IOSTANDARD  LVCMOS18 [get_ports "UART_TXD_O"]
set_property PACKAGE_PIN BB22     [get_ports "UART_RXD_I"]
set_property IOSTANDARD  LVCMOS18 [get_ports "UART_RXD_I"]
set_property PACKAGE_PIN BB25     [get_ports "UART_CTS_I_B"]
set_property IOSTANDARD  LVCMOS18 [get_ports "UART_CTS_I_B"]
set_property PACKAGE_PIN BA25     [get_ports "UART_RTS_O_B"]
set_property IOSTANDARD  LVCMOS18 [get_ports "UART_RTS_O_B"]
#USB_GPIOs
set_property PACKAGE_PIN AY25     [get_ports "UART_GPIO_0"]
set_property IOSTANDARD  LVCMOS18 [get_ports "UART_GPIO_0"]
set_property PACKAGE_PIN AY24     [get_ports "UART_GPIO_1"]
set_property IOSTANDARD  LVCMOS18 [get_ports "UART_GPIO_1"]
set_property PACKAGE_PIN BA24     [get_ports "UART_GPIO_2"]
set_property IOSTANDARD  LVCMOS18 [get_ports "UART_GPIO_2"]
set_property PACKAGE_PIN BA23     [get_ports "UART_GPIO_3"]
set_property IOSTANDARD  LVCMOS18 [get_ports "UART_GPIO_3"]
#RF-ADCs
set_property PACKAGE_PIN AH7      [get_ports "VCM23_227"]
set_property PACKAGE_PIN AC1      [get_ports "ADC_VIN3_227_N"]
set_property PACKAGE_PIN AC2      [get_ports "ADC_VIN3_227_P"]
set_property PACKAGE_PIN AC4      [get_ports "ADC_VIN2_227_N"]
set_property PACKAGE_PIN AC5      [get_ports "ADC_VIN2_227_P"]
set_property PACKAGE_PIN AH8      [get_ports "VCM01_227"]
set_property PACKAGE_PIN AE1      [get_ports "ADC_VIN1_227_N"]
set_property PACKAGE_PIN AE2      [get_ports "ADC_VIN1_227_P"]
set_property PACKAGE_PIN AE4      [get_ports "ADC_VIN0_227_N"]
set_property PACKAGE_PIN AE5      [get_ports "ADC_VIN0_227_P"]
set_property PACKAGE_PIN AY6      [get_ports "ADC_CLK_227_N"]
set_property PACKAGE_PIN AW6      [get_ports "ADC_CLK_227_P"]
set_property PACKAGE_PIN AJ7      [get_ports "VCM23_226"]
set_property PACKAGE_PIN AG1      [get_ports "ADC_VIN3_226_N"]
set_property PACKAGE_PIN AG2      [get_ports "ADC_VIN3_226_P"]
set_property PACKAGE_PIN AG4      [get_ports "ADC_VIN2_226_N"]
set_property PACKAGE_PIN AG5      [get_ports "ADC_VIN2_226_P"]
set_property PACKAGE_PIN AJ8      [get_ports "VCM01_226"]
set_property PACKAGE_PIN AJ1      [get_ports "ADC_VIN1_226_N"]
set_property PACKAGE_PIN AJ2      [get_ports "ADC_VIN1_226_P"]
set_property PACKAGE_PIN AJ4      [get_ports "ADC_VIN0_226_N"]
set_property PACKAGE_PIN AJ5      [get_ports "ADC_VIN0_226_P"]
set_property PACKAGE_PIN BB5      [get_ports "ADC_CLK_226_N"]
set_property PACKAGE_PIN BA5      [get_ports "ADC_CLK_226_P"]
set_property PACKAGE_PIN AH10     [get_ports "VCM23_225"]
```

```
set_property PACKAGE_PIN AL1      [get_ports "ADC_VIN3_225_N"]
set_property PACKAGE_PIN AL2      [get_ports "ADC_VIN3_225_P"]
set_property PACKAGE_PIN AL4      [get_ports "ADC_VIN2_225_N"]
set_property PACKAGE_PIN AL5      [get_ports "ADC_VIN2_225_P"]
set_property PACKAGE_PIN AH11     [get_ports "VCM01_225"]
set_property PACKAGE_PIN AN1      [get_ports "ADC_VIN1_225_N"]
set_property PACKAGE_PIN AN2      [get_ports "ADC_VIN1_225_P"]
set_property PACKAGE_PIN AN4      [get_ports "ADC_VIN0_225_N"]
set_property PACKAGE_PIN AN5      [get_ports "ADC_VIN0_225_P"]
set_property PACKAGE_PIN AY4      [get_ports "ADC_CLK_225_N"]
set_property PACKAGE_PIN AW4      [get_ports "ADC_CLK_225_P"]
set_property PACKAGE_PIN AJ10     [get_ports "VCM23_224"]
set_property PACKAGE_PIN AR1      [get_ports "ADC_VIN3_224_N"]
set_property PACKAGE_PIN AR2      [get_ports "ADC_VIN3_224_P"]
set_property PACKAGE_PIN AR4      [get_ports "ADC_VIN2_224_N"]
set_property PACKAGE_PIN AR5      [get_ports "ADC_VIN2_224_P"]
set_property PACKAGE_PIN AJ11     [get_ports "VCM01_224"]
set_property PACKAGE_PIN AU1      [get_ports "ADC_VIN1_224_N"]
set_property PACKAGE_PIN AU2      [get_ports "ADC_VIN1_224_P"]
set_property PACKAGE_PIN AU4      [get_ports "ADC_VIN0_224_N"]
set_property PACKAGE_PIN AU5      [get_ports "ADC_VIN0_224_P"]
set_property PACKAGE_PIN BB3      [get_ports "ADC_CLK_224_N"]
set_property PACKAGE_PIN BA3      [get_ports "ADC_CLK_224_P"]
set_property PACKAGE_PIN AF9      [get_ports "ADC_REXT_224"]
#RF-DAC
set_property PACKAGE_PIN C6      [get_ports "DAC_CLK_231_N"]
set_property PACKAGE_PIN D6      [get_ports "DAC_CLK_231_P"]
set_property PACKAGE_PIN F1      [get_ports "DAC_VOUT3_231_N"]
set_property PACKAGE_PIN F2      [get_ports "DAC_VOUT3_231_P"]
set_property PACKAGE_PIN F4      [get_ports "DAC_VOUT2_231_N"]
set_property PACKAGE_PIN F5      [get_ports "DAC_VOUT2_231_P"]
set_property PACKAGE_PIN H1      [get_ports "DAC_VOUT1_231_N"]
set_property PACKAGE_PIN H2      [get_ports "DAC_VOUT1_231_P"]
set_property PACKAGE_PIN H4      [get_ports "DAC_VOUT0_231_N"]
set_property PACKAGE_PIN H5      [get_ports "DAC_VOUT0_231_P"]
set_property PACKAGE_PIN A5      [get_ports "DAC_CLK_230_N"]
set_property PACKAGE_PIN B5      [get_ports "DAC_CLK_230_P"]
set_property PACKAGE_PIN K1      [get_ports "DAC_VOUT3_230_N"]
set_property PACKAGE_PIN K2      [get_ports "DAC_VOUT3_230_P"]
set_property PACKAGE_PIN K4      [get_ports "DAC_VOUT2_230_N"]
set_property PACKAGE_PIN K5      [get_ports "DAC_VOUT2_230_P"]
set_property PACKAGE_PIN M1      [get_ports "DAC_VOUT1_230_N"]
set_property PACKAGE_PIN M2      [get_ports "DAC_VOUT1_230_P"]
set_property PACKAGE_PIN M4      [get_ports "DAC_VOUT0_230_N"]
set_property PACKAGE_PIN M5      [get_ports "DAC_VOUT0_230_P"]
set_property PACKAGE_PIN C4      [get_ports "DAC_CLK_229_N"]
set_property PACKAGE_PIN D4      [get_ports "DAC_CLK_229_P"]
set_property PACKAGE_PIN P1      [get_ports "DAC_VOUT3_229_N"]
set_property PACKAGE_PIN P2      [get_ports "DAC_VOUT3_229_P"]
set_property PACKAGE_PIN P4      [get_ports "DAC_VOUT2_229_N"]
set_property PACKAGE_PIN P5      [get_ports "DAC_VOUT2_229_P"]
set_property PACKAGE_PIN T1      [get_ports "DAC_VOUT1_229_N"]
set_property PACKAGE_PIN T2      [get_ports "DAC_VOUT1_229_P"]
set_property PACKAGE_PIN T4      [get_ports "DAC_VOUT0_229_N"]
set_property PACKAGE_PIN T5      [get_ports "DAC_VOUT0_229_P"]
set_property PACKAGE_PIN D1      [get_ports "SYSREF_228_N"]
set_property PACKAGE_PIN D2      [get_ports "SYSREF_228_P"]
set_property PACKAGE_PIN A3      [get_ports "DAC_CLK_228_N"]
set_property PACKAGE_PIN B3      [get_ports "DAC_CLK_228_P"]
```

```
set_property PACKAGE_PIN U9      [get_ports "DAC_REXT_228"]
set_property PACKAGE_PIN V1      [get_ports "DAC_VOUT3_228_N"]
set_property PACKAGE_PIN V2      [get_ports "DAC_VOUT3_228_P"]
set_property PACKAGE_PIN V4      [get_ports "DAC_VOUT2_228_N"]
set_property PACKAGE_PIN V5      [get_ports "DAC_VOUT2_228_P"]
set_property PACKAGE_PIN Y1      [get_ports "DAC_VOUT1_228_N"]
set_property PACKAGE_PIN Y2      [get_ports "DAC_VOUT1_228_P"]
set_property PACKAGE_PIN Y4      [get_ports "DAC_VOUT0_228_N"]
set_property PACKAGE_PIN Y5      [get_ports "DAC_VOUT0_228_P"]
#MGTs
set_property PACKAGE_PIN AA37     [get_ports "128_REFCLK0_N"]
set_property PACKAGE_PIN AA36     [get_ports "128_REFCLK0_P"]
set_property PACKAGE_PIN Y35      [get_ports "128_REFCLK1_N"]
set_property PACKAGE_PIN Y34      [get_ports "128_REFCLK1_P"]
set_property PACKAGE_PIN AC42     [get_ports "128_RX0_N"]
set_property PACKAGE_PIN AB40     [get_ports "128_RX1_N"]
set_property PACKAGE_PIN AA42     [get_ports "128_RX2_N"]
set_property PACKAGE_PIN Y40      [get_ports "128_RX3_N"]
set_property PACKAGE_PIN AC41     [get_ports "128_RX0_P"]
set_property PACKAGE_PIN AB39     [get_ports "128_RX1_P"]
set_property PACKAGE_PIN AA41     [get_ports "128_RX2_P"]
set_property PACKAGE_PIN Y39      [get_ports "128_RX3_P"]
set_property PACKAGE_PIN V39      [get_ports "128_TX0_N"]
set_property PACKAGE_PIN U37      [get_ports "128_TX1_N"]
set_property PACKAGE_PIN T39      [get_ports "128_TX2_N"]
set_property PACKAGE_PIN R37      [get_ports "128_TX3_N"]
set_property PACKAGE_PIN V38      [get_ports "128_TX0_P"]
set_property PACKAGE_PIN U36      [get_ports "128_TX1_P"]
set_property PACKAGE_PIN T38      [get_ports "128_TX2_P"]
set_property PACKAGE_PIN R36      [get_ports "128_TX3_P"]
set_property PACKAGE_PIN V35      [get_ports "129_REFCLK0_N"]
set_property PACKAGE_PIN V34      [get_ports "129_REFCLK0_P"]
set_property PACKAGE_PIN T35      [get_ports "129_REFCLK1_N"]
set_property PACKAGE_PIN T34      [get_ports "129_REFCLK1_P"]
set_property PACKAGE_PIN W36      [get_ports "129_MREF"]
set_property PACKAGE_PIN W42      [get_ports "129_RX0_N"]
set_property PACKAGE_PIN U42      [get_ports "129_RX1_N"]
set_property PACKAGE_PIN R42      [get_ports "129_RX2_N"]
set_property PACKAGE_PIN N42      [get_ports "129_RX3_N"]
set_property PACKAGE_PIN W41      [get_ports "129_RX0_P"]
set_property PACKAGE_PIN U41      [get_ports "129_RX1_P"]
set_property PACKAGE_PIN R41      [get_ports "129_RX2_P"]
set_property PACKAGE_PIN N41      [get_ports "129_RX3_P"]
set_property PACKAGE_PIN P39      [get_ports "129_TX0_N"]
set_property PACKAGE_PIN N37      [get_ports "129_TX1_N"]
set_property PACKAGE_PIN M39      [get_ports "129_TX2_N"]
set_property PACKAGE_PIN L37      [get_ports "129_TX3_N"]
set_property PACKAGE_PIN P38      [get_ports "129_TX0_P"]
set_property PACKAGE_PIN N36      [get_ports "129_TX1_P"]
set_property PACKAGE_PIN M38      [get_ports "129_TX2_P"]
set_property PACKAGE_PIN L36      [get_ports "129_TX3_P"]
set_property PACKAGE_PIN P35      [get_ports "130_REFCLK0_N"]
set_property PACKAGE_PIN P34      [get_ports "130_REFCLK0_P"]
set_property PACKAGE_PIN M35      [get_ports "130_REFCLK1_N"]
set_property PACKAGE_PIN M34      [get_ports "130_REFCLK1_P"]
set_property PACKAGE_PIN L42      [get_ports "130_RX0_N"]
set_property PACKAGE_PIN J42      [get_ports "130_RX1_N"]
set_property PACKAGE_PIN G42      [get_ports "130_RX2_N"]
set_property PACKAGE_PIN F40      [get_ports "130_RX3_N"]
```

```
set_property PACKAGE_PIN L41      [get_ports "130_RX0_P"]
set_property PACKAGE_PIN J41      [get_ports "130_RX1_P"]
set_property PACKAGE_PIN G41      [get_ports "130_RX2_P"]
set_property PACKAGE_PIN F39      [get_ports "130_RX3_P"]
set_property PACKAGE_PIN K39      [get_ports "130_TX0_N"]
set_property PACKAGE_PIN J37      [get_ports "130_TX1_N"]
set_property PACKAGE_PIN H39      [get_ports "130_TX2_N"]
set_property PACKAGE_PIN G37      [get_ports "130_TX3_N"]
set_property PACKAGE_PIN K38      [get_ports "130_TX0_P"]
set_property PACKAGE_PIN J36      [get_ports "130_TX1_P"]
set_property PACKAGE_PIN H38      [get_ports "130_TX2_P"]
set_property PACKAGE_PIN G36      [get_ports "130_TX3_P"]
set_property PACKAGE_PIN K35      [get_ports "131_REFCLK0_N"]
set_property PACKAGE_PIN K34      [get_ports "131_REFCLK0_P"]
set_property PACKAGE_PIN H35      [get_ports "131_REFCLK1_N"]
set_property PACKAGE_PIN H34      [get_ports "131_REFCLK1_P"]
set_property PACKAGE_PIN E42      [get_ports "131_RX0_N"]
set_property PACKAGE_PIN D40      [get_ports "131_RX1_N"]
set_property PACKAGE_PIN C42      [get_ports "131_RX2_N"]
set_property PACKAGE_PIN B40      [get_ports "131_RX3_N"]
set_property PACKAGE_PIN E41      [get_ports "131_RX0_P"]
set_property PACKAGE_PIN D39      [get_ports "131_RX1_P"]
set_property PACKAGE_PIN C41      [get_ports "131_RX2_P"]
set_property PACKAGE_PIN B39      [get_ports "131_RX3_P"]
set_property PACKAGE_PIN F35      [get_ports "131_TX0_N"]
set_property PACKAGE_PIN E37      [get_ports "131_TX1_N"]
set_property PACKAGE_PIN C37      [get_ports "131_TX2_N"]
set_property PACKAGE_PIN A37      [get_ports "131_TX3_N"]
set_property PACKAGE_PIN F34      [get_ports "131_TX0_P"]
set_property PACKAGE_PIN E36      [get_ports "131_TX1_P"]
set_property PACKAGE_PIN C36      [get_ports "131_TX2_P"]
set_property PACKAGE_PIN A36      [get_ports "131_TX3_P"]?
```

System Controller

The Xilinx system controller is an application that runs on a Zynq®-7000 SoC at power-up on the ZCU1275 board. The System Controller user interface (SCUI) can be downloaded from the Zynq UltraScale+ RFSoC ZCU1275 Characterization Kit documentation page. The SCUI file `rdf0477-zcu1275-system-controller-2018-3.zip` is associated with this user guide. The SCUI communicates with the Zynq-7000 SoC using the Interface 1 port of the Silicon Labs USB to Quad-UART described in the USB to Quad-UART Bridge. See Figure D-1.

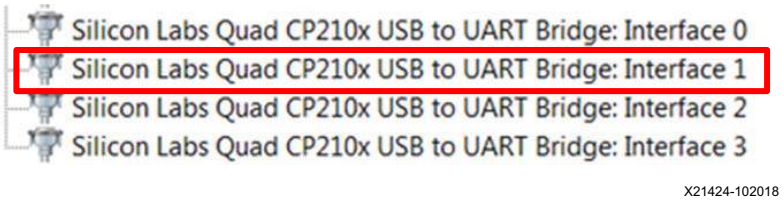


Figure D-1: **Silicon Labs Interface 1 COM Port**

Connecting the System Controller User Interface

Upon invoking the SCUI, a window opens with fields to enter information about the board being used (Figure D-2). These values can later be stored into EEPROM in the EEPROM Data tab. If the EEPROM data has already been stored, only the Board and Revision fields need to be selected.

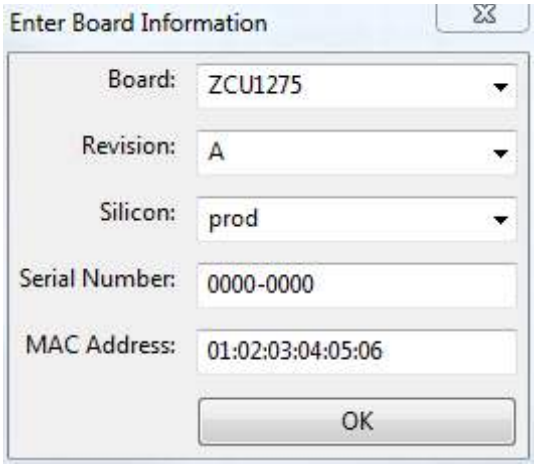


Figure D-2: **SCUI Board Information Window**

After entering the board information and pressing OK, the main window of the SCUI comes up (Figure D-3). On the left side of the window is the system controller controls and on the right side is a log of the operations.

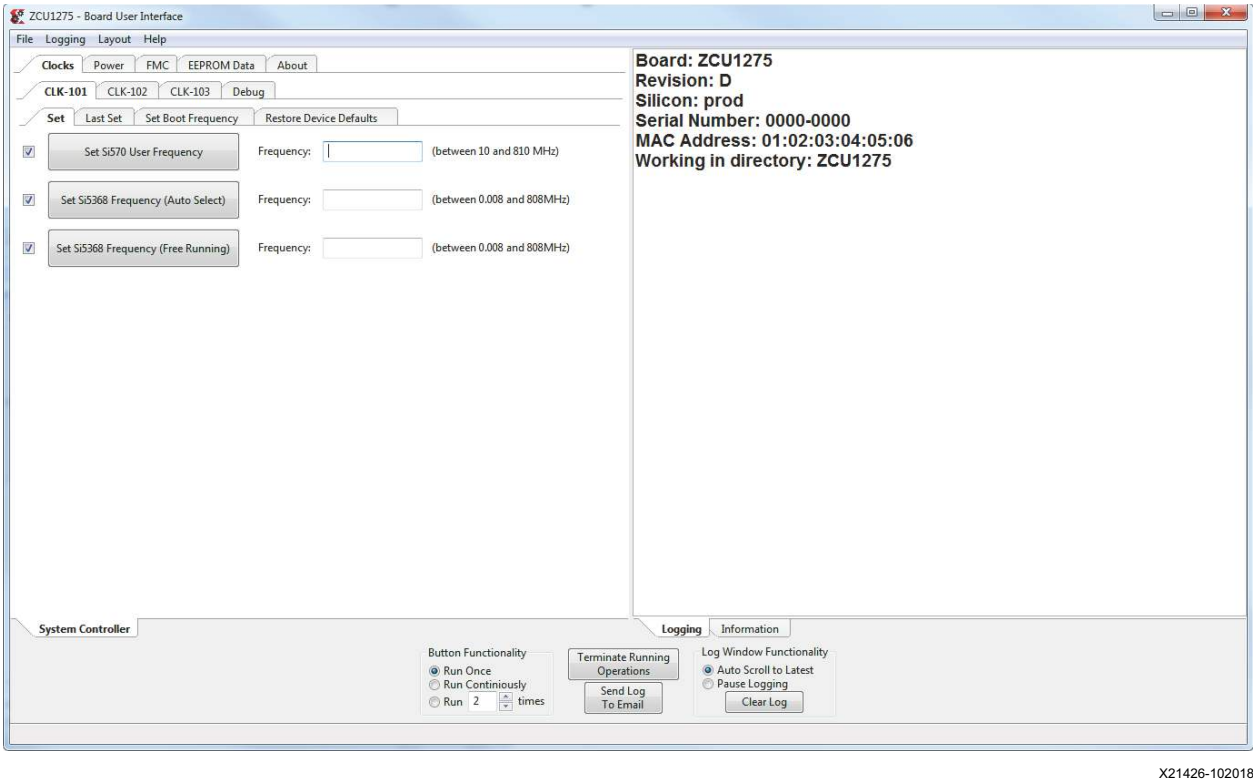


Figure D-3: **SCUI Main Window**

Connect a USB A to Micro-B USB cable from the host PC to the ZCU1275 USB/UART connector (callout 5, Figure 1-2). In the SCUI click **File > Change the System Controller**

Port. In the Select the system controller port window, select the COM port associated with Silicon Labs Quad CP210x USB to UART Bridge: Interface 1, and press **OK**. The SCUI is now connected to the ZCU1275 board.

IMPORTANT: *Make sure J121 is set to position (2-3) DUT PMBUS DIS to isolate the DUT PMBUS/I2C signals and prevent bus contention. If contention occurs, the system controller cannot execute commands.*

Programmable Clocks Tab

The Clocks tab (Figure D-4) is used to set the frequency of the SuperClock-2 Module clock sources (See SuperClock-2 Module) and the SuperClock-RF2 Module clock sources (see SuperClock-RF2 Module).

Figure D-4: **Clocks Tab**

Under the Clocks tab is another row of tabs to select either the SuperClock-2 Module (CLK-101) or the SuperClock-RF2 Module (CLK-103) (Figure D-5).

CLK-101 Tab

This section includes a description of the CLK-101 tab options which are used to control the SuperClock-2 Module. Arbitrary field value entries are used to illustrate the operations. The CLK-101 tab is shown in Figure D-5.

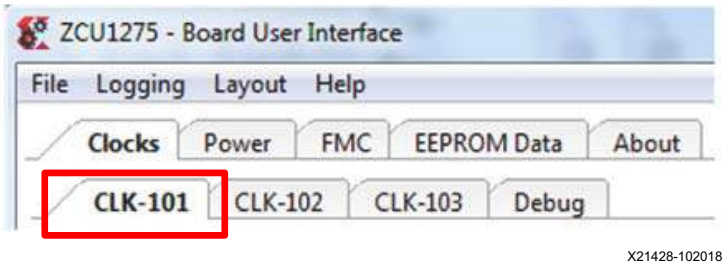


Figure D-5: **CLK-101 Tab**

Note: For each of the operations listed below, several seconds might elapse before the operation completes.

Set CLK-101 Si570 Frequency

In the Set tab, enter the desired Si570 frequency in MHz in the field next to the **Set Si570 User Frequency** button and press Enter or click the button (Figure D-6). Upon successful completion of setting the frequency, the Logging pane shows no errors and prints **Finished**.

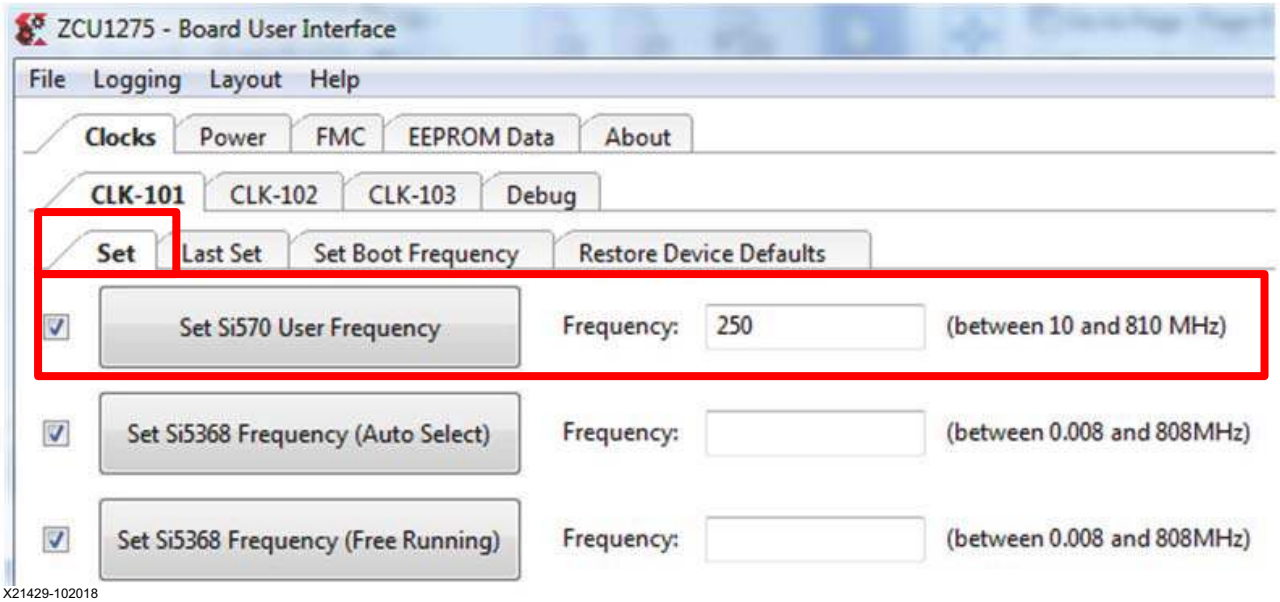


Figure D-6: **CLK-101 Set Si570 User Frequency**

Set CLK-101 Si5368 Frequency

There are two buttons in the Set tab that can be used to program the Si5368 clock source: **Set Si5368 Frequency (Auto Select)** and **Set Si5368 Frequency (Free Running)**. The free-running option uses the onboard XA-XB crystal as the active clock routed to the Si5368 internal PLL. The auto select option uses one of the recovery clocks routed to the SuperClock-2 Module interface as the active clock. Enter the desired Si5368 frequency in MHz in the field next to either the auto select or free-running buttons and press Enter or click the related button (Figure D-7). Upon successful completion of setting the frequency, the Logging pane shows no errors and prints **Finished**.

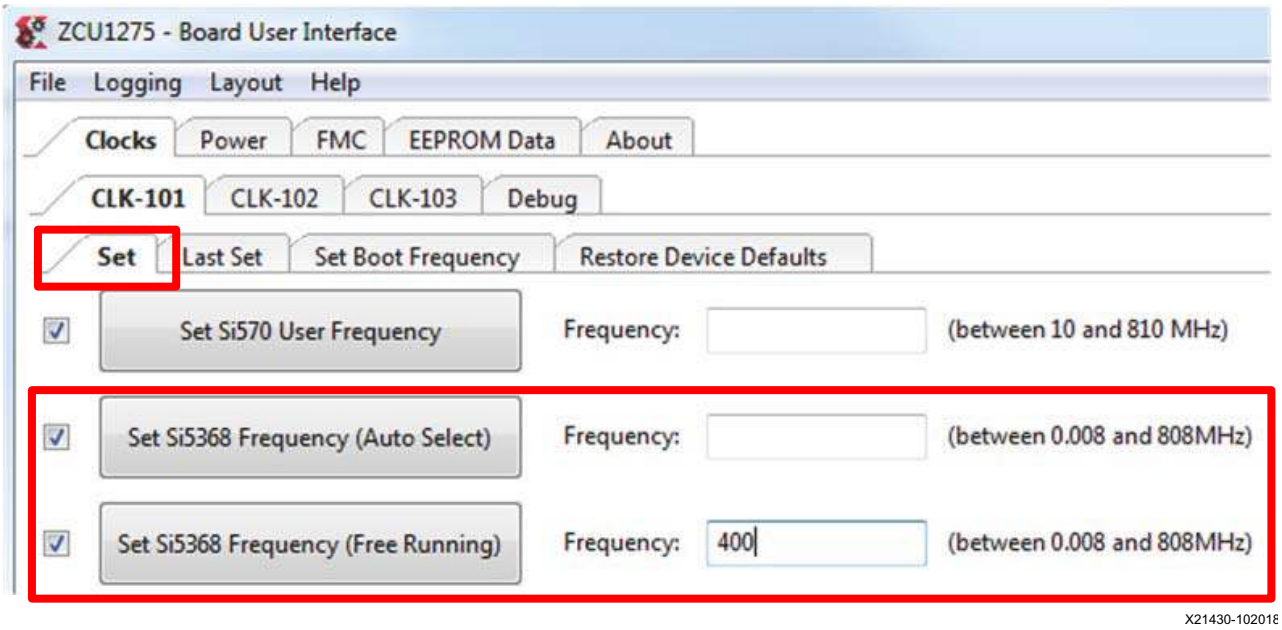


Figure D-7: **CLK-101 Set Si5368 Frequency**

Save CLK-101 Boot Frequency to EEPROM

Default boot frequency settings can be stored in EEPROM, which are programmed into each clock source at power-up. Enter the desired boot frequencies in the **Set Boot Frequency** tab and press Enter to save the boot frequency to EEPROM (Figure D-8). Upon successful completion of setting the boot frequencies, the Logging pane shows no errors and prints **Finished**.

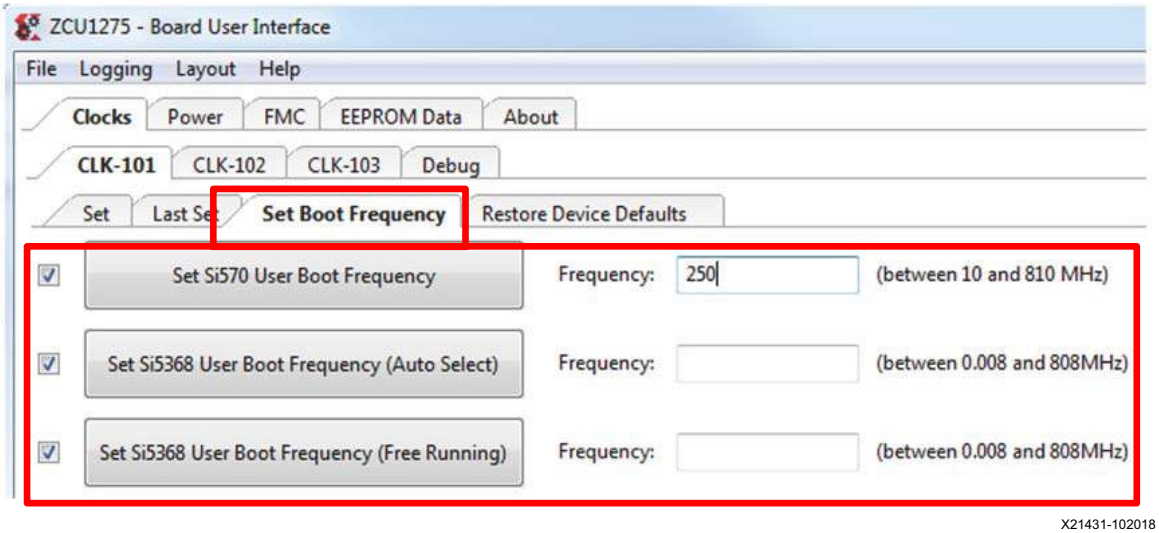


Figure D-8: **CLK-101 Set Boot Frequency Tab**

Restore CLK-101 Boot Frequency from EEPROM

The boot frequencies saved in EEPROM can be restored at any time using the Restore Device Defaults tab. Click **Restore Si570 User** to restore the Si570 frequency stored in EEPROM, and click **Restore Si5368 User** to restore the Si5368 frequency stored in EEPROM (Figure D-9).

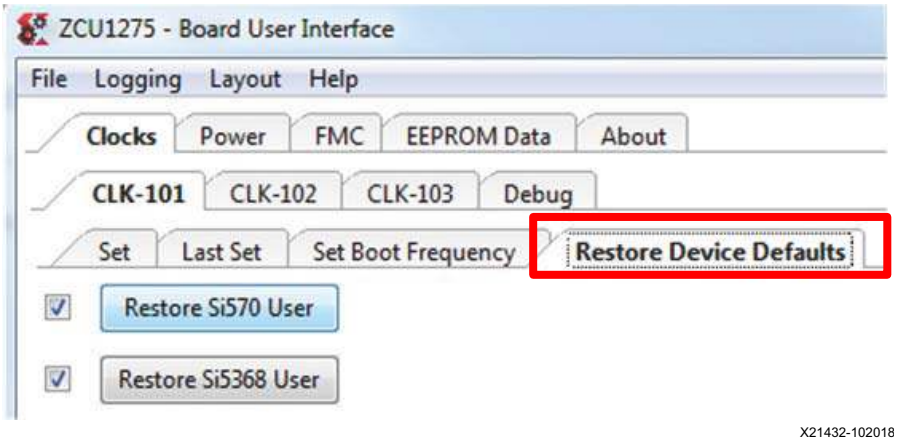


Figure D-9: **CLK-101 Restore Device Defaults Tab**

View Last Set CLK-101 Frequencies

The last frequencies that were written to the CLK-101 Module can be viewed using the **Last Set** tab. Click the **Read Si570 User Frequency** to view the Si570 frequency and **Last Set Si5368 User Frequency** to view the Si5368 frequency (Figure D-10).

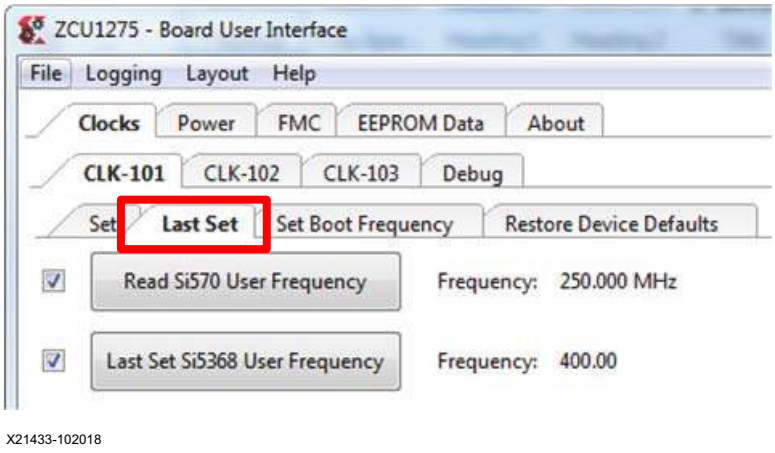


Figure D-10: **CLK-101 Last Set Tab**

CLK-103 Tab

This section includes a description of the CLK-103 tab options used to control the SuperClock-RF2 Module. Arbitrary field value entries are used to illustrate the operations. The CLK-103 tab is shown in Figure D-11.

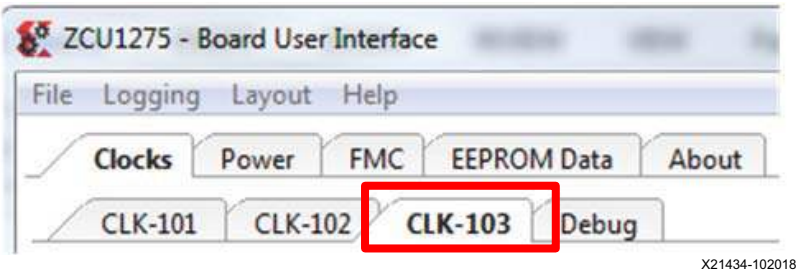


Figure D-11: **CLK-103 Tab**

The SCUI is packaged with a set of clock files that contain register values for preset frequencies used by the SuperClock-RF2 clock sources. Each clock source has its own folder where the clock files are stored. The location of these folders is `BoardUI\tests\ZCU1275\clockFiles` (Figure D-12). Do not move or rename any of the folders in that directory structure because the SCUI relies on that directory structure to find the clock files.

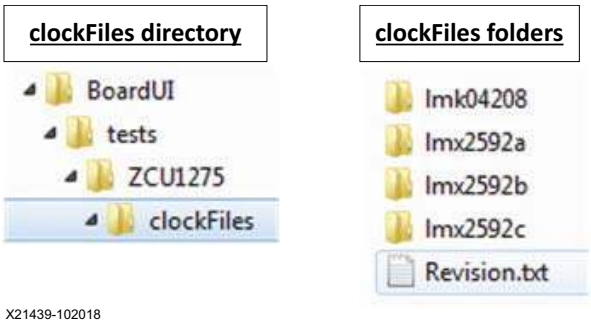


Figure D-12: **CLK-103 Clock Files**

Note: For each of the following operations, several seconds might elapse before the operation completes.

Set CLK-103 LMK04208 (General Purpose Clock) Frequency

In the Set tab, enter the full file name of the clock file with the desired LMK04208 frequency in the field next to **Type file name in the clockFiles/lmk04208 folder** and press Enter or click the **Set LMK04208 Frequency** button (Figure D-13). Upon successful completion of setting the frequency, the Logging pane shows no errors and prints **Finished**.

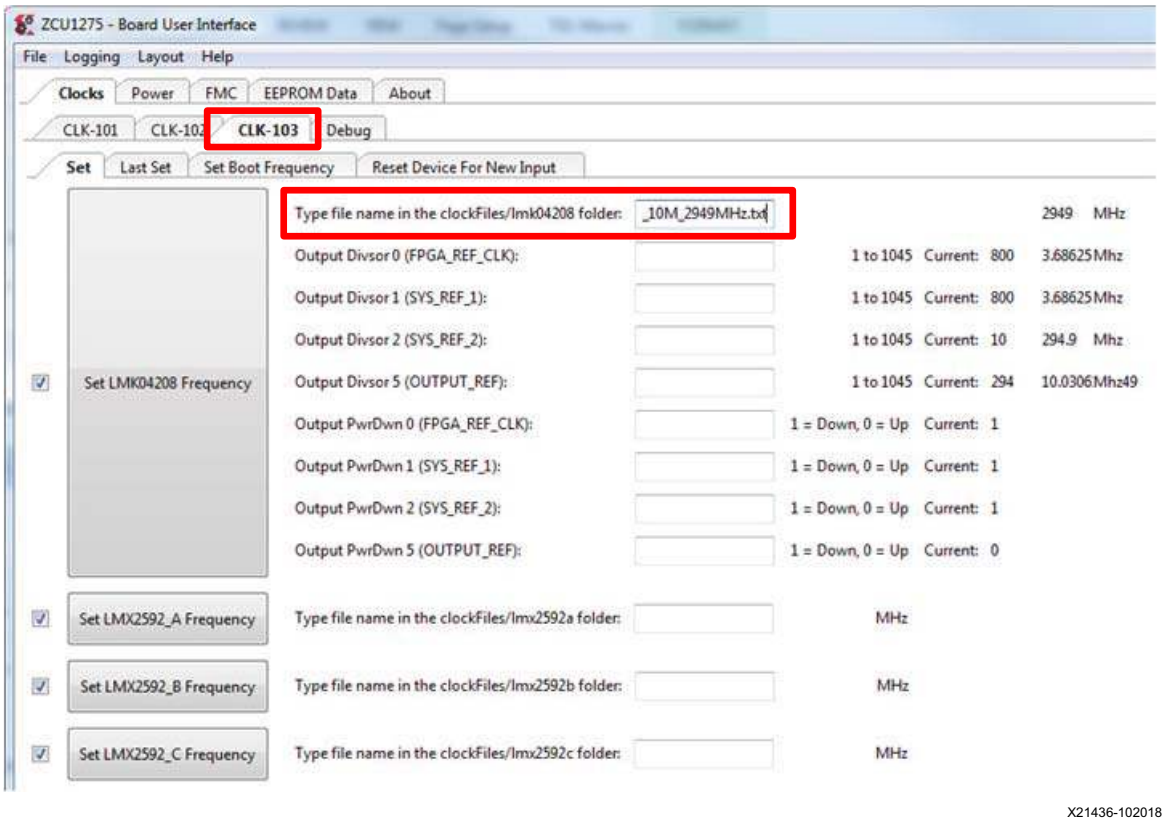


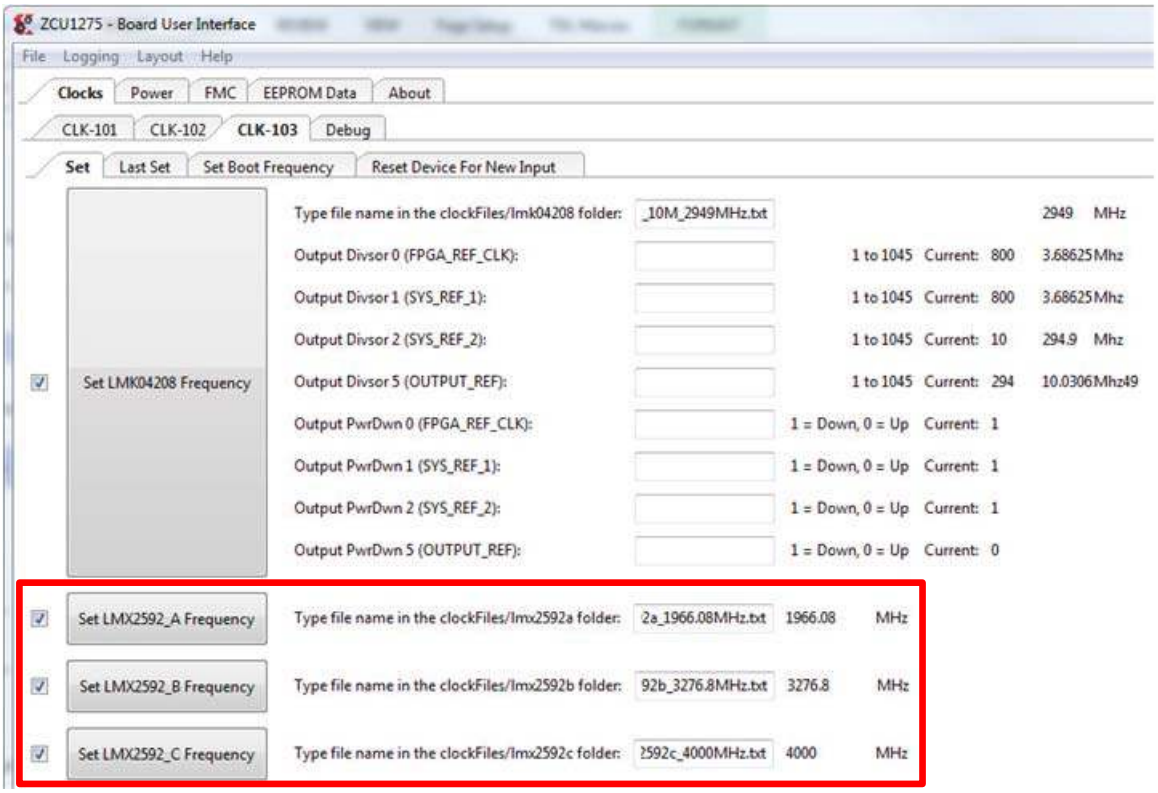
Figure D-13: **CLK-103 Set LMK04208 Frequency**

After entering a clock file, the current settings and frequencies are listed to the right of the relevant fields. To change the output divisors of an LMK04208 clock source, enter the new divisor in the Output Divisor field and press Enter. To disable or enable an output, use the Output PwrDwn field. A 0 enables the output and a 1 disables it.

Set CLK-103 LMX2592 PLL A, B, and C Frequency

Enter the full file name of the clock file with the desired frequency for PLL A in the field next to **Type file name in the clockFiles/lmx2592a folder** and press Enter or click the **Set LMX2592_A Frequency** button (Figure D-14). The same can be done for PLL B and

C in the next two fields down. Be sure to enter the exact file names from the associated folders. Upon successful completion of setting the frequency, the Logging pane shows no errors and prints **Finished**.



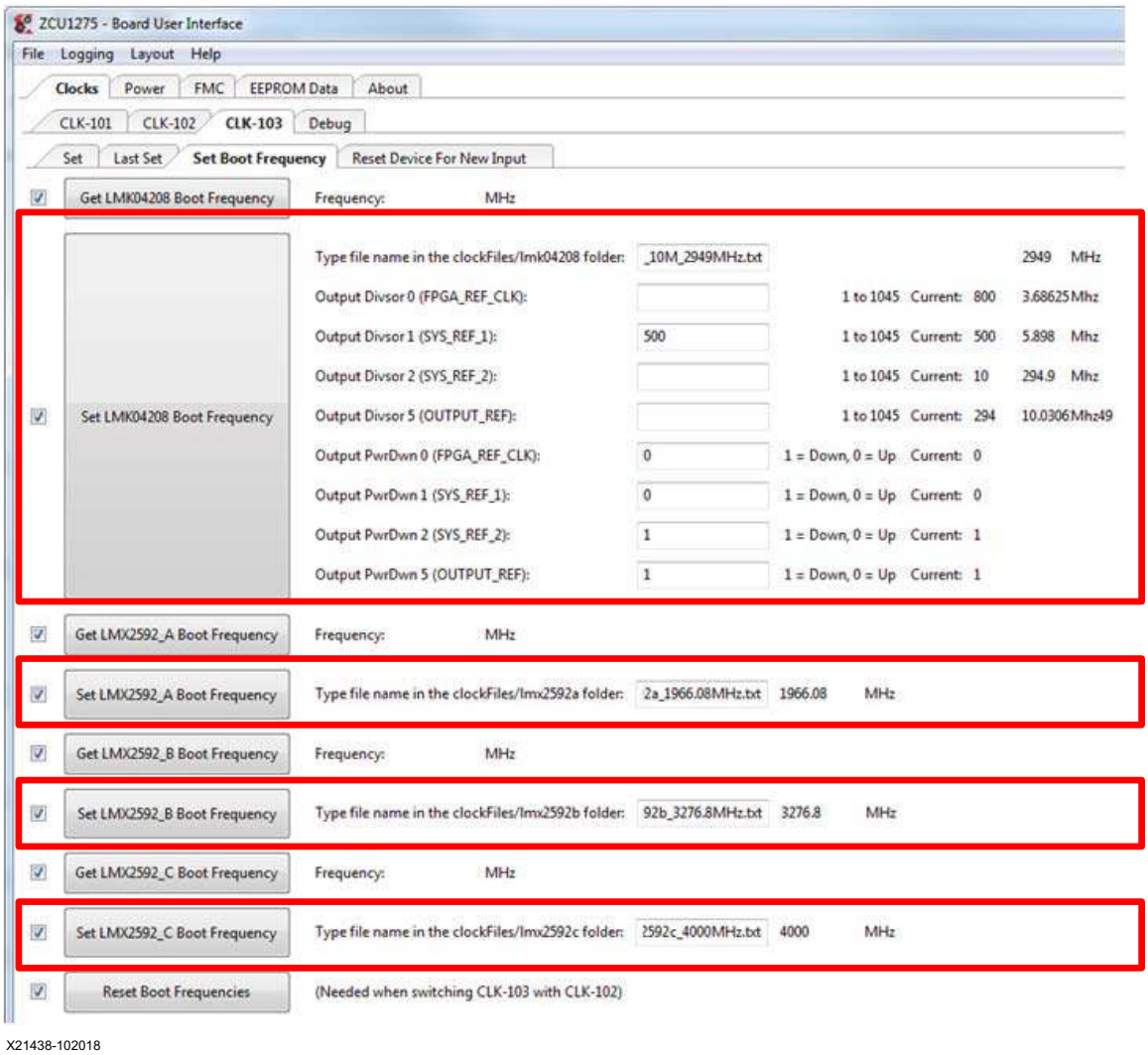
X21437-102018

Figure D-14: **CLK-103 Set LMX2592 Frequency**

Save CLK-103 Boot Frequency to EEPROM

Default boot frequency settings can be stored in EEPROM, which are programmed into each clock source at power-up. In the **Set Boot Frequency** tab, enter the full name of the clock files for the desired boot frequencies in each file name field. In addition, LMK04208 output divisors and enable/disable settings can also be entered and stored. After clock files and values are entered, click the related set boot frequency button to

store (Figure D-15). Upon successful completion of setting the boot frequencies, the Logging pane shows no errors and prints **Finished**.



X21438-102018

Figure D-15: **CLK-103 Set Boot Frequency Tab**

To view the boot frequency saved in EEPROM, click the related get boot frequency button in the **Set Boot Frequency** tab.

View Last Set CLK-103 Frequencies

The last frequencies that were written to the CLK-103 Module can be viewed using the **Last Set** tab. Click the relevant last set button to view the last frequency written to the PLL by the SCUI (Figure D-16).

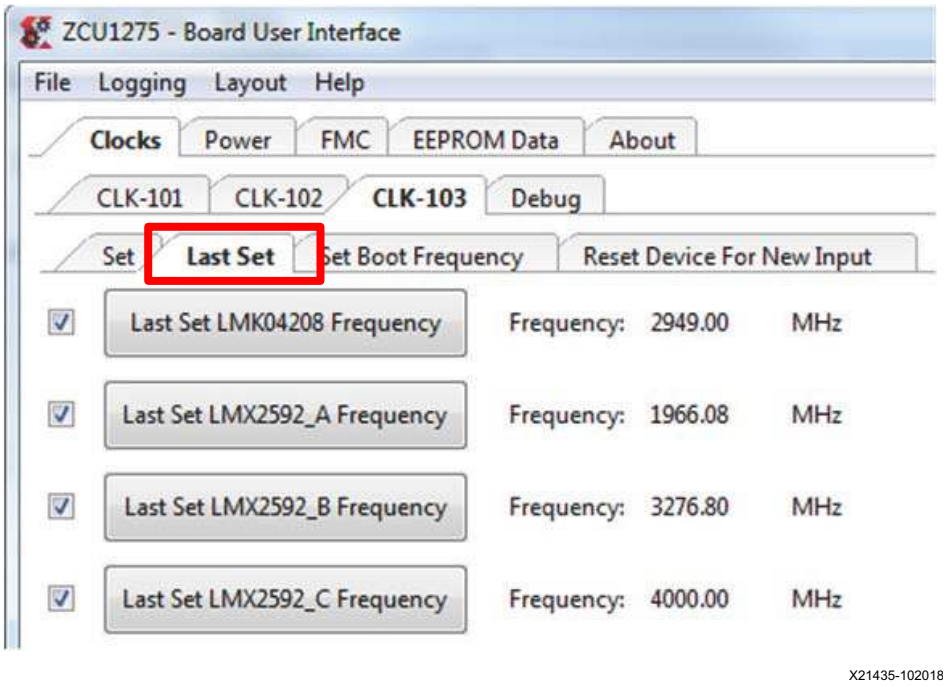


Figure D-16: **CLK-103 Last Set Tab**

Reset CLK-103 Clocks

The SuperClock-RF2 clocks can be reset from the **Reset Device For New Input** tab. Click the corresponding reset button to restore the PLL registers to the default values (Figure D-17).

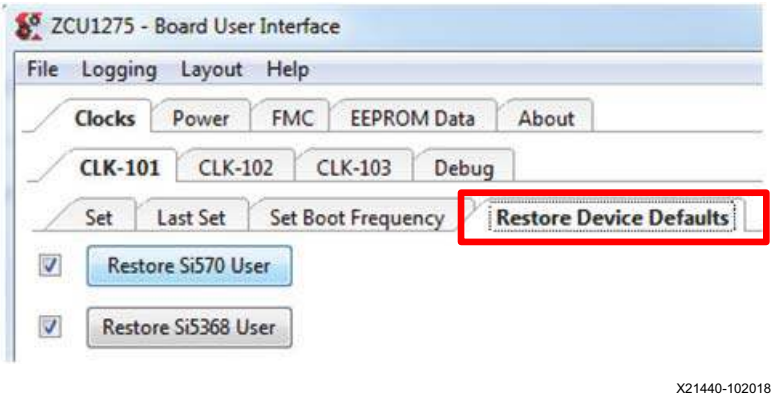


Figure D-17: **CLK-103 Reset Device For New Input Tab**

Power Tab

The SCUI can read the onboard INA226 power rail measurements for each of the power rails listed in Table D-1. The measurements can be read once or scanned continuously.

Table D-1: **Monitored Power Rails**

	Power Rail
RFSoC logic and processor	VCCINT
	VCCBRAM
	VCCAUX
	VCCO_HP
	VCCO_HD
	VCCPINT
	VCCPAUX
	VCC_PSPLL
	VCCO_DDR
	VCCO_MIO
	VCCINT_AMS
GTY transceiver	MGTAVCC
	MGTAVTT
	MGTVCCAUX
PS-GTR transceiver	MGTRAVCC
	MGTRAVTT

Read a Single Power Rail

To read a single power rail measurement, click the corresponding button with the power rail name on it and the Power, Voltage, and Current measurements are printed to the right of the button (Figure D-18).

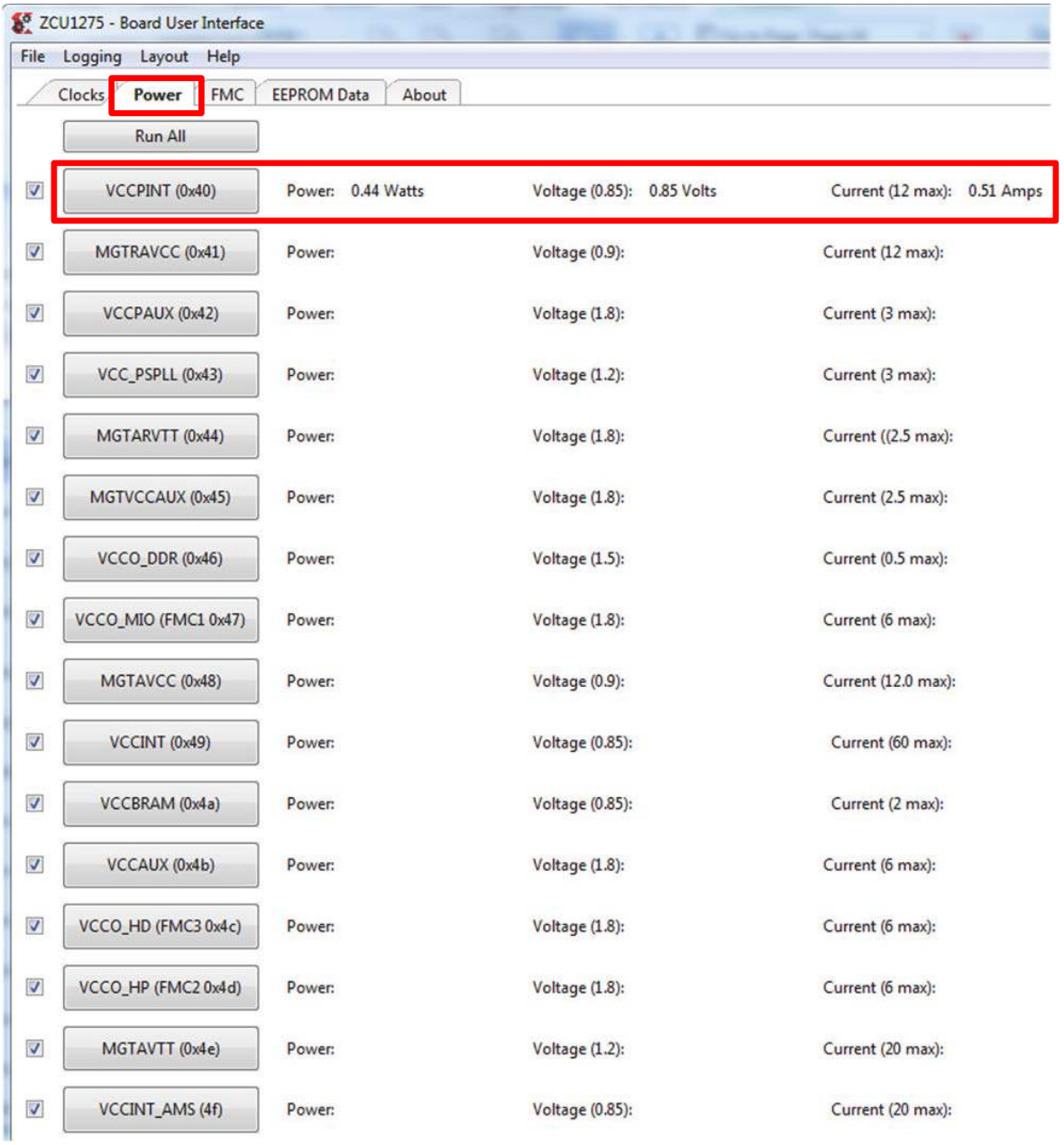


Figure D-18: **Read a Single Power Rail**

Read Multiple Power Rails

To read multiple power rail measurements at once, check the box to the left of each power rail button and click the **Run All** button at the top (Figure D-19).

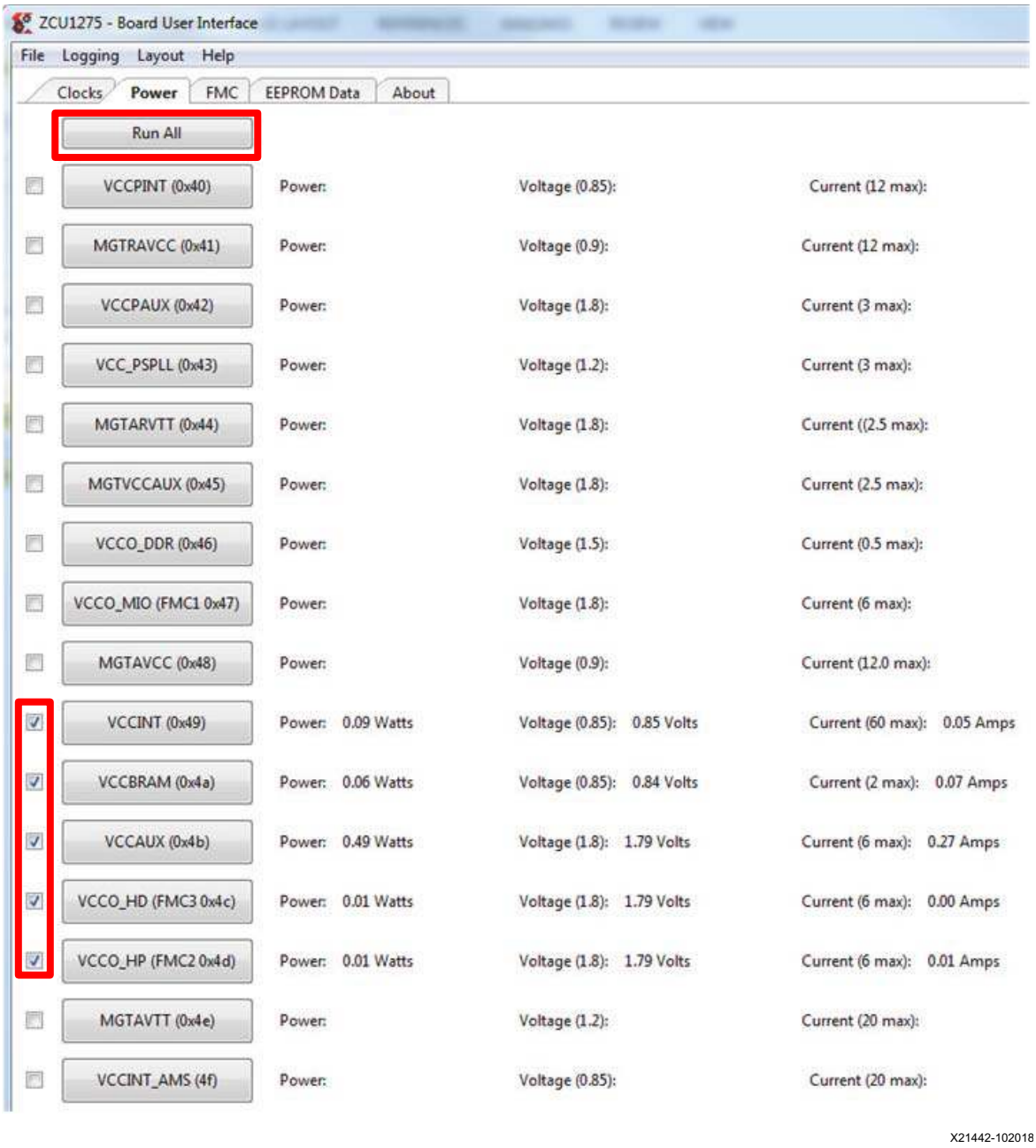


Figure D-19: **Read Multiple Power Rails**

Read Power Rails Continuously

To continuously read power rails, use the Button Functionality options at the bottom of the SCUI. Select either the **Run Continuously** radio button or the **Run x times** radio button, then click the power rail button to read the measurements. To stop the reading, click the **Terminate Running Operations** button (Figure 37).

Note: The Button Functionality options apply to all buttons in the System Controller pane, not just the Power tab. Be sure to switch back to **Run Once** when using other tabs in the SCUI.

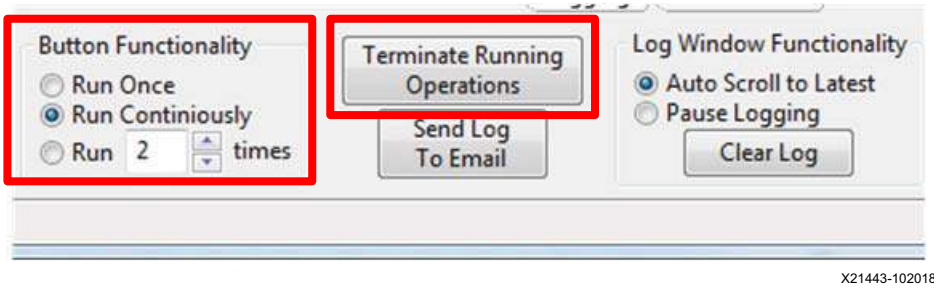


Figure D-20: **Read Power Rails Continuously**

FMC Tab

The ZCU1275 board provides two FPGA mezzanine card (FMC) ANSI/VITA 57.1 expansion interfaces, JA3 and JA4 (callout 53 and 54, Figure 1-2). Table D-2 shows the FMC cards supported by the System Controller and the programmable clock resources on each card.

Table D-2: **FMC Card Clock Sources**

Xilinx FMC Card	Description	Clock Source #1	Clock Source #2
XM101	LVDS QSE card	Si570	SI570
XM104	Serial transceiver connectivity card	Si570	Si5368
XM105	Debug card	Si570	N/A
XM107	Loopback card	Si570	N/A

Notes:

1. These FMC cards are not included in the ZCU1275 kit.

The FMC tab has options for viewing FMC card EEPROM data, changing the VADJ voltage for each FMC interface, and programming clock sources (Figure D-21).

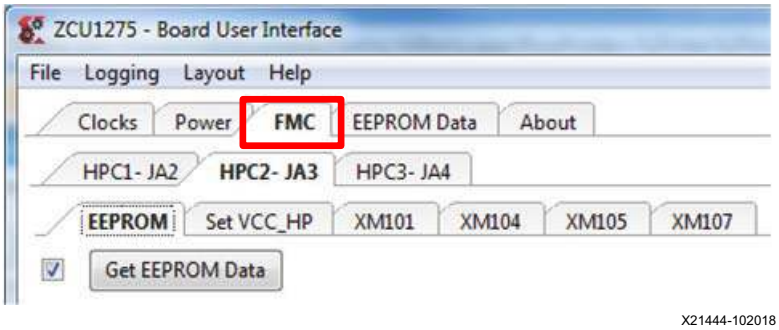


Figure D-21: **FMC Tab**

View FMC EEPROM Data

All FMC mezzanine cards host an I2C EEPROM which can be read out through the FMC menu. A raw hexadecimal display and a formatted version of the FMC EEPROM data are provided through the FMC menu. The VITA 57.1 standard identifies the data fields of the intelligent platform management interface (IPMI) specification used for the FMC EEPROM.

Select the FMC interface tab with the target FMC card, then select the EEPROM tab and click **Get EEPROM Data**. A window pops up displaying the contents of the EEPROM. The example shown in Figure D-22 is for an XM107 card connected to JA3.

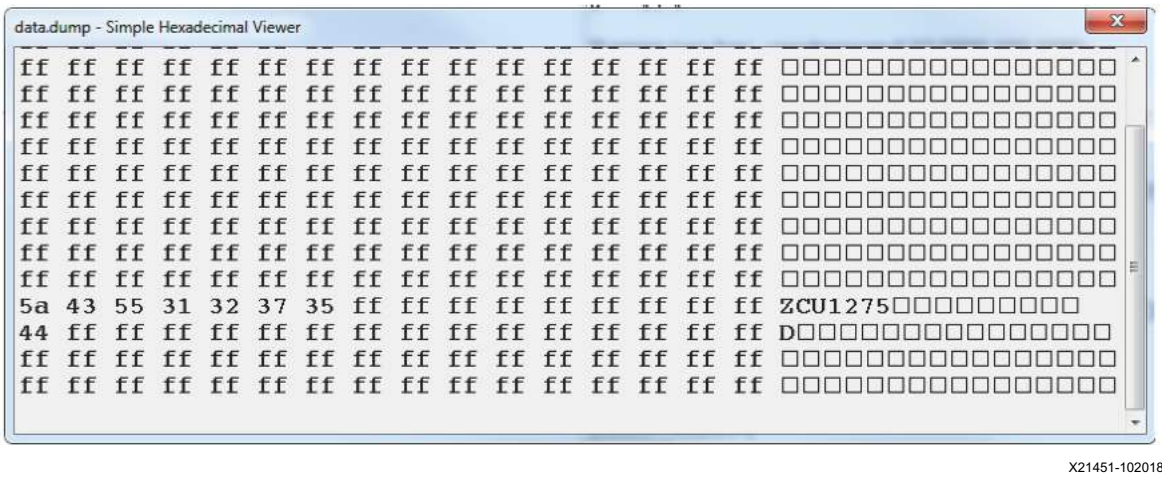


Figure D-22: **Get EEPROM Data Window**

Set FMC VADJ

Each FMC interface connects to a set of I/O banks on the RFSoC. The RFSoC bank voltage is connected to VADJ on the FMC interface to allow the FMC card to track the bank voltage

that it is connected to. The system controller can change the bank voltage that is connected to each FMC interface. JA3 is connected to VCCO_HP bank I/O pins and JA4 is connected to VCCO_HD bank I/O pins.

Select the FMC interface tab with the target FMC card, select the **Set VCC_HP** or **Set VCC_HD** tab, depending on the interface. Click the button with the desired bank voltage (Figure D-23).

IMPORTANT: *Changing the bank voltage affects all banks connected to that bank voltage, not just the FMC interface. Confirm that any other I/Os being used on the ZCU1275 board are compatible with the new bank voltage.*

Note: Power cycling ZCU1275 reverts all bank voltage changes back to the default voltage levels.

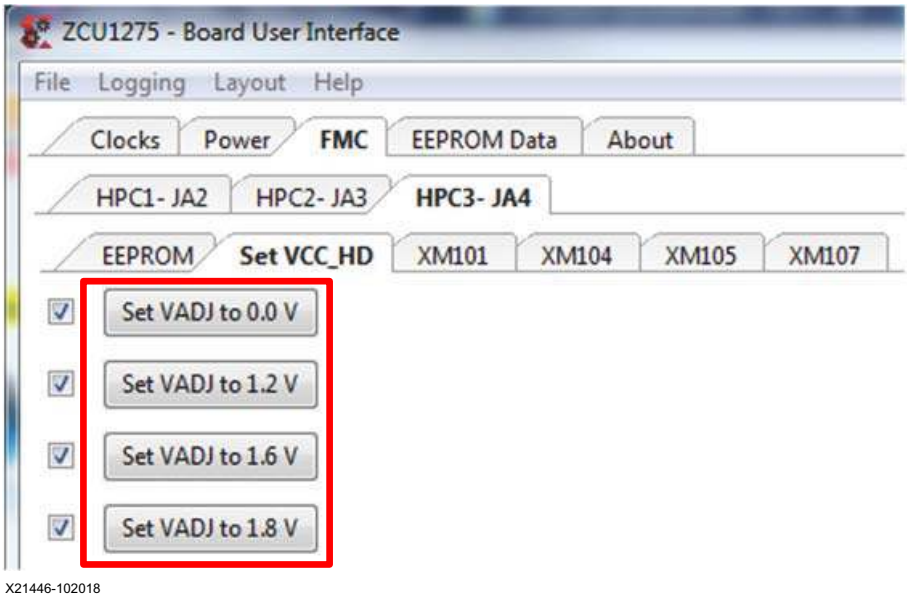


Figure D-23: **Set VADJ**

Set FMC Clocks

Select the FMC interface tab with the target FMC card, then select the tab with the FMC card part number (XM101, XM104, XM105, or XM107). Each tab has options to set the clocks on available clock sources. Enter the frequency in MHz and click the **Set SI570** or **Set SI5368** button to program the clock. The example shown in Figure D-24 sets the SI570 clock to 200 MHz on an XM104 card connected to JA3.

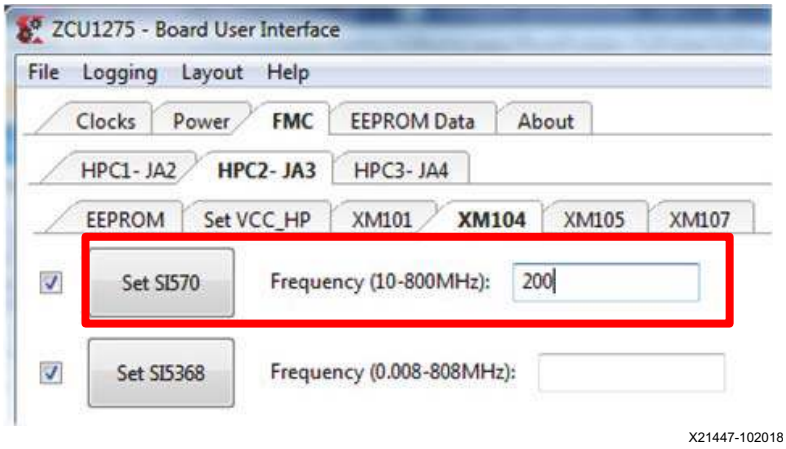


Figure D-24: **Set Clocks**

EEPROM Data Tab

The ZCU1275 System Controller includes an EEPROM which is used to store board information. The information entered into the Board Information window which pops up when the SCUI is launched (Figure D-2) can be stored to the EEPROM using the EEPROM Data tab. The EEPROM data can also be read using this tab (see Figure D-25).

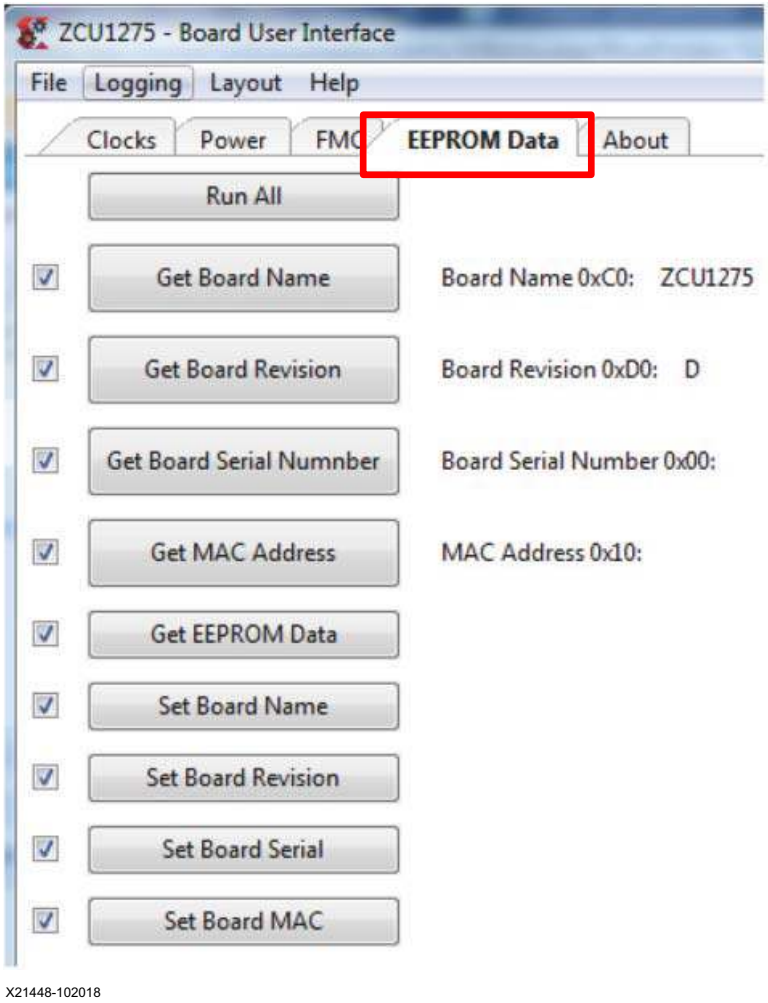


Figure D-25: **EEPROM Data**

Write Board EEPROM Data

To write EEPROM data, use the **Set xxxxxx** buttons shown in Figure D-26.

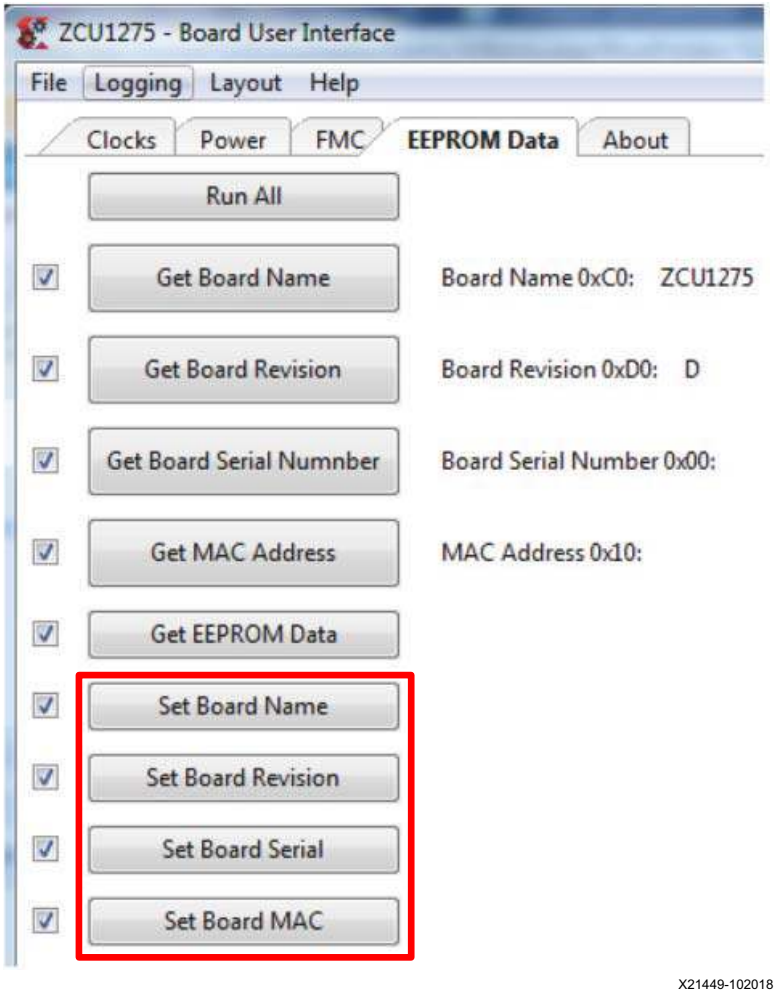


Figure D-26: **Set EEPROM Data**

Read Board EEPROM Data

To read EEPROM data, use the **Get xxxxxx** buttons shown in Figure D-27.

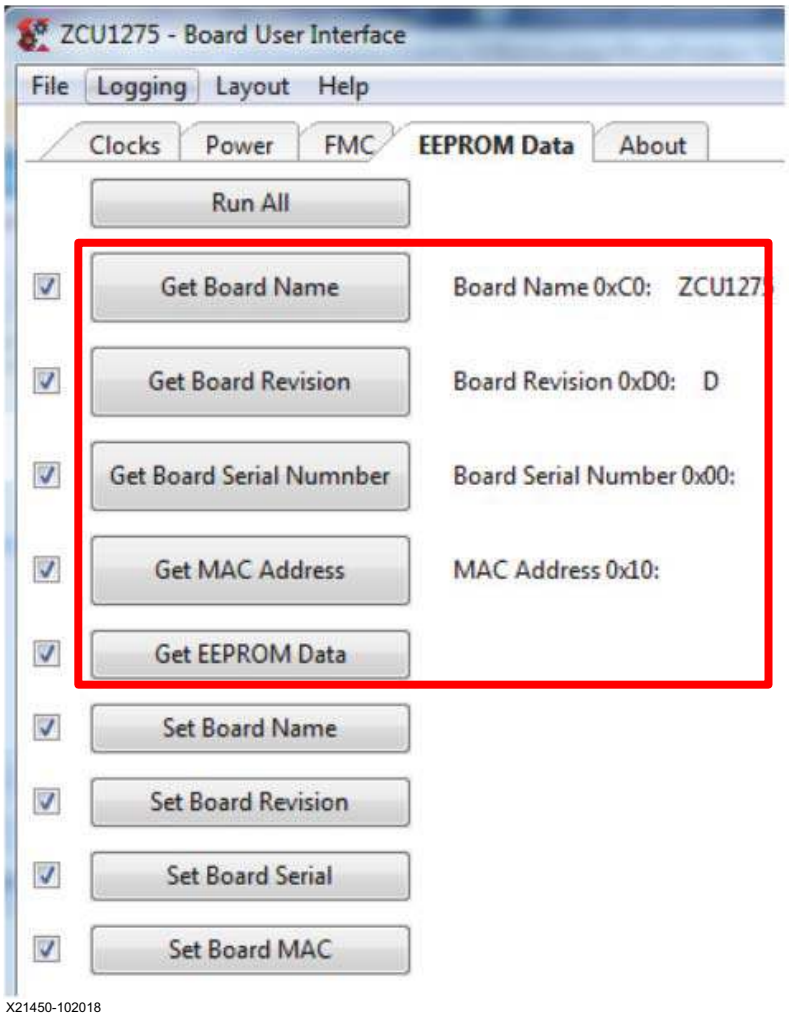


Figure D-27: **Get EEPROM Data**

The **Get EEPROM Data** button opens a window displaying the full contents of the EEPROM memory (Figure D-28).

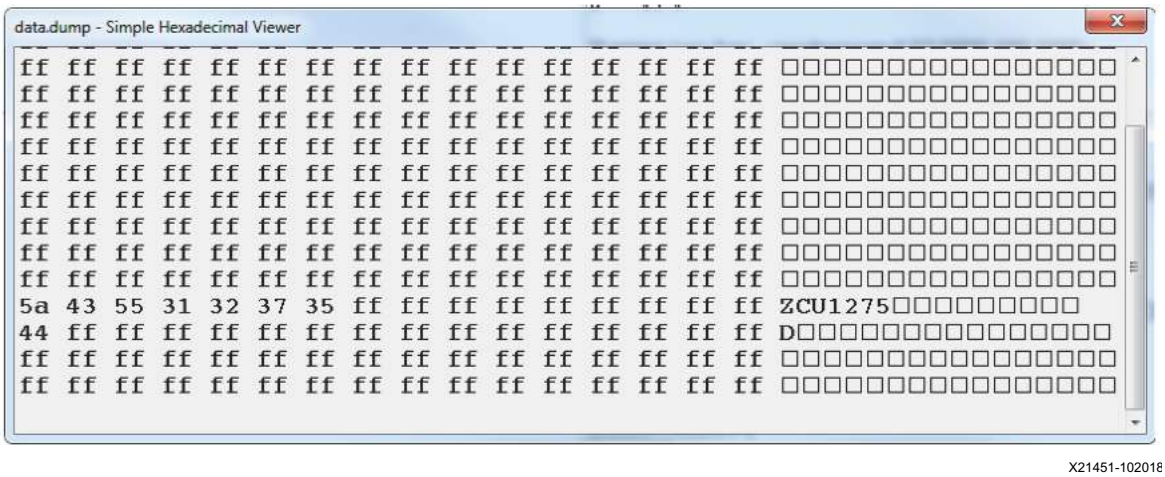


Figure D-28: **Get EEPROM Data Window**

Appendix E

Additional Resources and Legal Notices

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see Xilinx Support.

Solution Centers

See the Xilinx Solution Centers for support on devices, software tools, and intellectual property at all stages of the design cycle. Topics include design assistance, advisories, and troubleshooting tips.

Documentation Navigator and Design Hubs

Xilinx® Documentation Navigator provides access to Xilinx documents, videos, and support resources, which you can filter and search to find information. To open the Xilinx Documentation Navigator (DocNav):

- From the Vivado® IDE, select **Help > Documentation and Tutorials**.
- On Windows, select **Start > All Programs > Xilinx Design Tools > DocNav**.
- At the Linux command prompt, enter `docnav`.

Xilinx Design Hubs provide links to documentation organized by design tasks and other topics, which you can use to learn key concepts and address frequently asked questions. To access the Design Hubs:

- In the Xilinx Documentation Navigator, click the **Design Hubs View** tab.
- On the Xilinx website, see the Design Hubs page.

Note: For more information on Documentation Navigator, see the Documentation Navigator page on the Xilinx website.

References

The most up to date information related to ZCU1275 and its documentation is available on these websites.

Zynq UltraScale+ RFSoC ZCU1275 Characterization Kit

Zynq UltraScale+ ZCU1275 Characterization Kit — Master Answer Record 71640

These Xilinx documents and sites provide supplemental material useful with this guide:

1. Information about the power system components used in the ZCU1275 board is available from the Maxim Integrated website at www.maximintegrated.com/en/products/power/intune
2. Renesas Power Management: www.renesas.com/us/en/products/power-management/switching-regulators/integrated-fet-regulators/device/ISL8024.html#documents
3. Monolithic Power Systems: www.monolithicpower.com/en/reference-design-partners-xilinx-reference-design-rfsoc-power-module
4. *UltraScale Architecture and Product Data Sheet: Overview* (DS890)
5. *UltraScale Architecture System Monitor User Guide* (UG580)
6. Samtec, Inc. Bulls Eye interface: www.samtec.com/cables/high-speed/test/bulls-eye
7. Texas Instruments: www.ti.com/lit/ds/symlink/ina226.pdf
8. *Vivado Design Suite User Guide: Using Constraints* (UG903)
9. *HW-CLK-101-SCLK2 SuperClock-2 Module User Guide* (UG770)

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