

# 40160B/74C160/54C160 • 40161B/74C161/54C161 40162B/74C162/54C162 • 40163B/74C163/54C163

## 4-BIT SYNCHRONOUS COUNTERS

**DESCRIPTION** — The 40160B and the 40162B are fully synchronous edge-triggered 4-Bit Decade Counters. The 40161B and the 40163B are fully synchronous edge-triggered 4-Bit Binary Counters. Each device has a Clock Input (CP); four synchronous Parallel Data Inputs ( $P_0$ - $P_3$ ); three synchronous Mode Control Inputs, Parallel Enable ( $\overline{PE}$ ), Count Enable Parallel (CEP) and Count Enable Trickle (CET); Buffered Outputs from all four bit positions ( $Q_0$ - $Q_3$ ); and a Terminal Count Output (TC). The 40162B and 40163B have an additional synchronous Mode Control Input, Synchronous Reset ( $\overline{SR}$ ). Alternately, the 40160B and 40161B have an overriding asynchronous Master Reset ( $\overline{MR}$ ).

Operation is fully synchronous except for Master Reset on the 40160B and 40161B and occurs on the LOW-to-HIGH transition of the Clock Input (CP). When the Parallel Enable Input ( $\overline{PE}$ ) is LOW, the next LOW-to-HIGH transition of the Clock Input (CP) loads data into the counter from Parallel Inputs ( $P_0$ - $P_3$ ). When the Parallel Enable Input ( $\overline{PE}$ ) is HIGH, the next LOW-to-HIGH transition of the Clock Input (CP) advances the counter to its next state only if both Count Enable Inputs (CEP and CET) are HIGH when the state of the counter is nine ( $Q_0 = Q_3 = \text{HIGH}$ ,  $Q_1 = Q_2 = \text{LOW}$ ) for the 40160B and 40162B/fifteen ( $Q_0 = Q_1 = Q_2 = Q_3 = \text{HIGH}$ ) for the 40161B and 40163B and the Count Enable Trickle Input (CET) is HIGH. For the 40162B and 40163B a LOW on the Synchronous Reset Input ( $\overline{SR}$ ) sets all Outputs ( $Q_0$ - $Q_3$  and TC) LOW on the next LOW-to-HIGH transition of the Clock Input (CP) independent of the state of all other synchronous Mode Control Inputs (CEP, CET,  $\overline{PE}$ ). For the 40160B and 40161B, a LOW on the overriding asynchronous Master Reset ( $\overline{MR}$ ) sets all outputs ( $Q_0$ - $Q_3$  and TC) LOW, independent of the state of all other inputs.

These devices perform multistage synchronous counting without additional components by using a carry look-ahead counting technique.

The 40160B, 40161B, 40162B, and 40163B are edge-triggered; therefore, the synchronous Mode Control Input (CEP, CET,  $\overline{PE}$  for the 40160B/40161B and CEP, CET,  $\overline{PE}$ ,  $\overline{SR}$  for the 40162B/40163B) must be stable only during the set-up time before the LOW-to-HIGH transition of the Clock Input (CP).

The 40160B, 40161B, 40162B and 40163B are direct replacements for the 74C160/54C160, 74C161/54C161, 74C162/54C162, and 74C163/54C163 respectively.

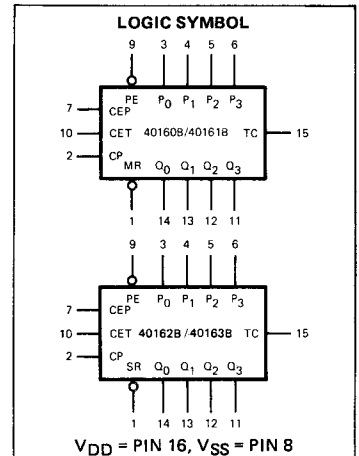
- 12 MHz TYPICAL COUNT FREQUENCY AT  $V_{DD} = 10\text{ V}$
- DECODED TERMINAL COUNT
- FULLY SYNCHRONOUS COUNTING AND PARALLEL ENTRY
- SYNCHRONOUS (40162B/40163B) OR ASYNCHRONOUS (40160B/40161B) RESET
- BUILT-IN CARRY CIRCUITRY
- FULLY EDGE-TRIGGERED

### PIN NAMES

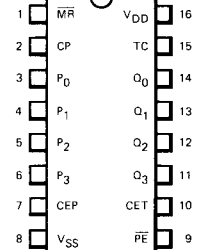
$\overline{PE}$	Parallel Enable Input (Active LOW)
$P_0$ - $P_3$	Parallel Inputs
CEP	Count Enable Parallel Input
CET	Count Enable Trickle Input
CP	Clock Input (L → H Edge-Triggered)
$\overline{MR}$	Master Reset Input (Active LOW) for the 40160B/40161B Only
$\overline{SR}$	Synchronous Reset Input (Active LOW) for the 40162B/40163B Only
$Q_0$ - $Q_3$	Parallel Outputs
TC	Terminal Count Output

### SELECTOR GUIDE

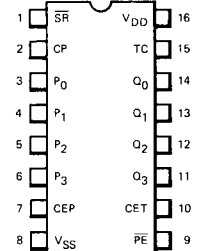
RESET	MODULUS	
	DECADE	BINARY
Asynchronous	40160B	40161B
Synchronous	40162B	40163B



### 40160B/40161B CONNECTION DIAGRAM DIP (TOP VIEW)



### 40162B/40163B CONNECTION DIAGRAM DIP (TOP VIEW)



**NOTE:**  
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

**SYNCHRONOUS MODE SELECTION**  
40160B/40161B

$\overline{PE}$	CEP	CET	MODE
L	X	X	Preset
H	L	X	No Change
H	X	L	No Change
H	H	H	Count

$\overline{MR}$  = HIGH

**SYNCHRONOUS MODE SELECTION**  
40162B/40163B

$\overline{SR}$	$\overline{PE}$	CEP	CET	MODE
H	L	X	X	Preset
H	H	L	X	No Change
H	H	X	L	No Change
H	H	H	H	Count
L	X	X	X	Reset

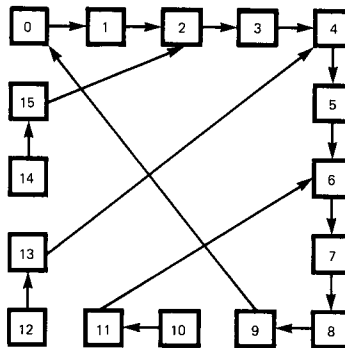
**TERMINAL COUNT GENERATION**

CET	40160B/40162B ( $Q_0 \cdot \overline{Q_1} \cdot \overline{Q_2} \cdot Q_3$ )	40161B/40163B ( $Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3$ )	TC
L	L	L	L
L	H	H	L
H	L	L	L
H	H	H	H

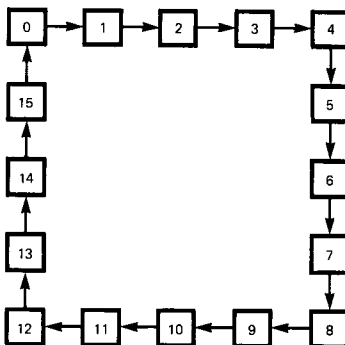
H = HIGH Level  
L = LOW Level  
X = Don't Care

TC = CET ·  $Q_0$  ·  $\overline{Q_1}$  ·  $\overline{Q_2}$  ·  $Q_3$  (40160B/40162B)  
TC = CET ·  $Q_0$  ·  $Q_1$  ·  $Q_2$  ·  $Q_3$  (40161B/40163B)

**STATE DIAGRAM**  
40160B • 40162B



**STATE DIAGRAM**  
40161B • 40163B

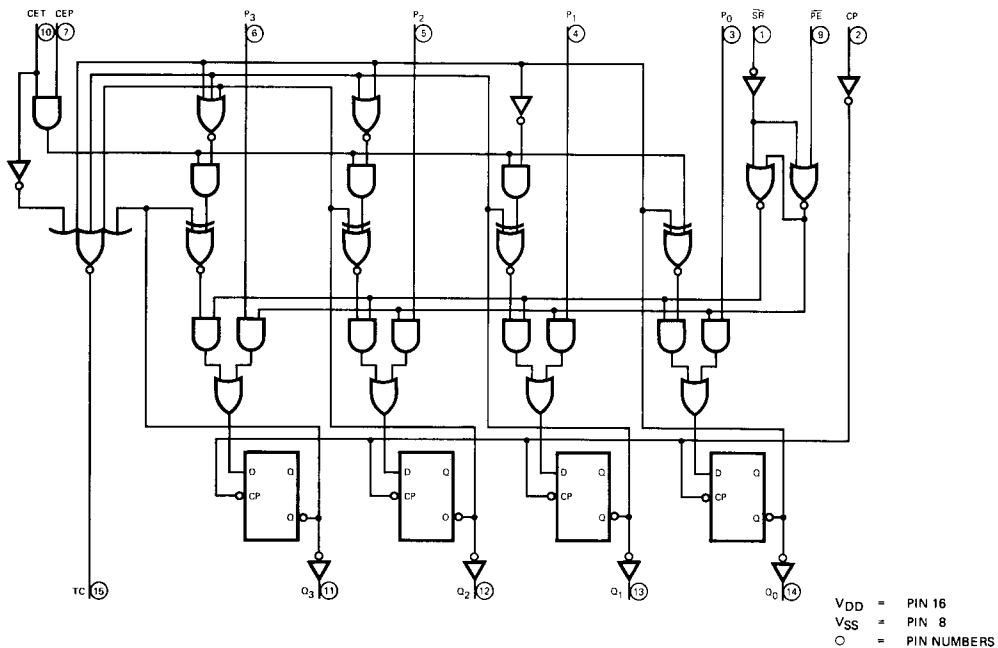


**NOTE:**

The 40160B or 40162B can be preset to any state, but will not count beyond 9. If preset to state 10, 11, 12, 13, 14 or 15, they will return to their normal sequence within two clock pulses.

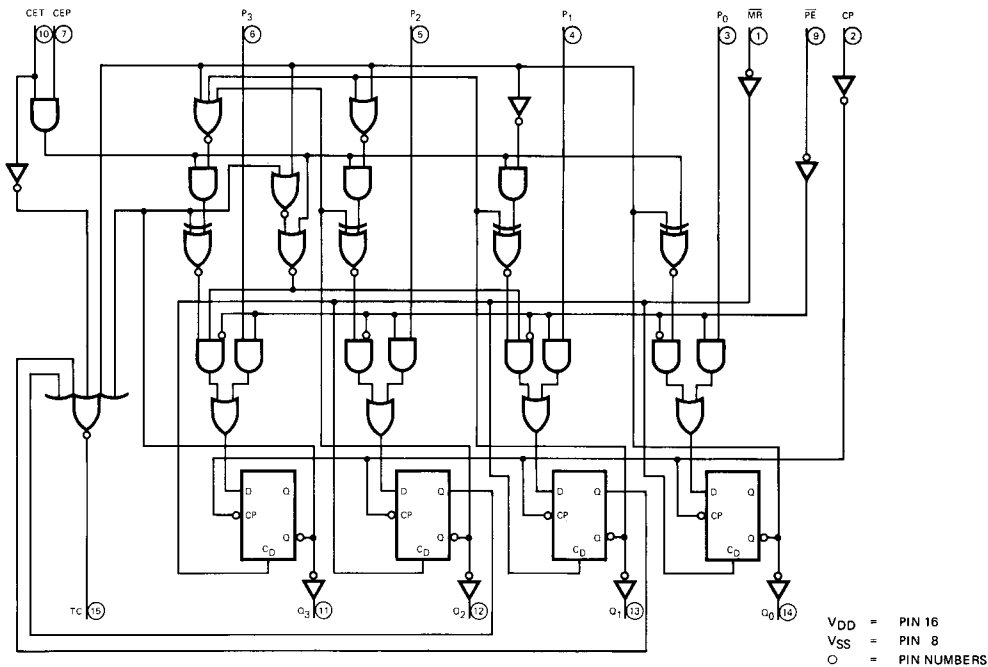
**40161B/40163B LOGIC DIAGRAM**

The 40161B and 40163B binary synchronous counters are similar. However, the 40161B has an asynchronous master reset circuit as shown on the 40160B/40162B Logic Diagram.



**40160B/40162B LOGIC DIAGRAM**

The 40160B and 40162B BCD synchronous counters are similar. However, the 40162B has a synchronous reset circuit as shown on the 40161B/40163B Logic Diagram.



**FAIRCHILD CMOS • 40160B/74C160/54C160 • 40161B/74C161/54C161 •  
40162B/74C162/54C162 • 40163B/74C163/54C163**

**DC CHARACTERISTICS:**  $V_{DD}$  as shown,  $V_{SS} = 0$  V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS	
			$V_{DD} = 5$ V			$V_{DD} = 10$ V			$V_{DD} = 15$ V						
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX				
$I_{DD}$	Quiescent Power	XC			20			40			80	$\mu$ A	MIN, 25°C	All inputs at 0 V or $V_{DD}$	
					150			300			600		MAX		
	Supply Current	XM			5			10			20		$\mu$ A		MIN, 25°C
					150			300			600				MAX

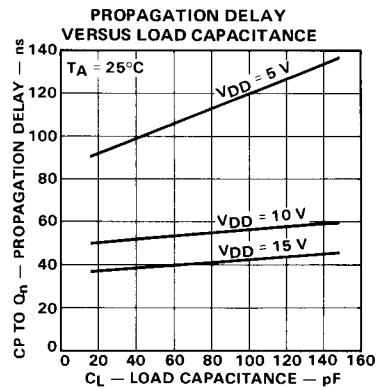
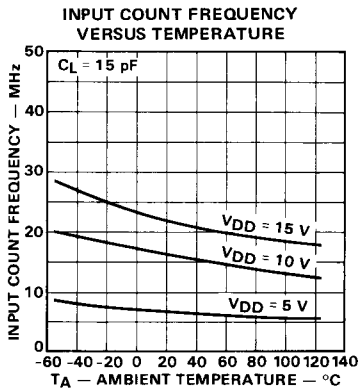
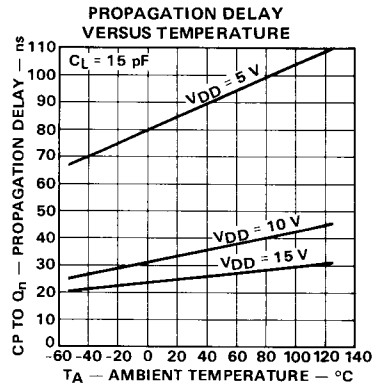
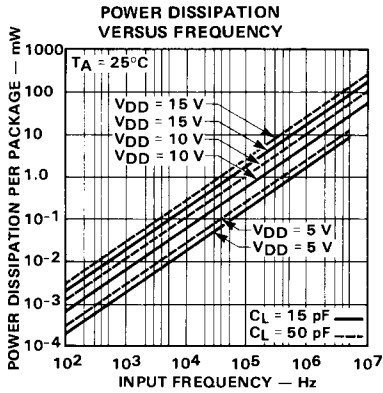
**AC CHARACTERISTICS AND SET-UP REQUIREMENTS:**  $V_{DD}$  as shown,  $V_{SS} = 0$  V,  $T_A = 25^\circ$ C (See Note 2)

SYMBOL	PARAMETER		LIMITS									UNITS	TEST CONDITIONS
			$V_{DD} = 5$ V			$V_{DD} = 10$ V			$V_{DD} = 15$ V				
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
$t_{PLH}$	Propagation Delay, CP to Q		120	220		55	105		40	84	ns	$C_L = 50$ pF, $R_L = 200$ k $\Omega$ Input Transition Times $\leq 20$ ns	
$t_{PHL}$			120	220		55	105		38	84			
$t_{PLH}$	Propagation Delay, CP to TC		155	285		70	130		45	104	ns		
$t_{PHL}$			155	285		70	130		40	104			
$t_{PLH}$	Propagation Delay, CET to TC		95	165		40	80		27	64	ns		
$t_{PHL}$			95	165		55	95		36	76			
$t_{PLH}$	Propagation Delay, MR to Q		150	285		65	125		44	100	ns		
$t_{PHL}$		Propagation Delay, MR to TC		175	335		75	145		52			116
$t_{TLH}$	Output Transition Time			60	135		35	70		25	45		ns
$t_{THL}$			70	135		30	70		23	45			
$t_{rec}$	MR Recovery Time		50	15		30	10		24	7	ns	(40160B/40161B)	
$t_{wMR(L)}$	MR Minimum Pulse Width		110	60		55	27		44	17	ns	(40160B/40161B)	
$t_{wCP}$	CP Minimum Pulse Width		90	50		40	20		32	15	ns		
$t_s$	Set-Up Time, Data to CP		70	35		35	18		28	13			
$t_h$	Hold Time, Data to CP		0	-30		0	-15		0	-10	ns		
$t_s$	Set-Up Time, $\overline{PE}$ to CP		110	60		60	30		48	20			
$t_h$	Hold Time, $\overline{PE}$ to CP		-10	-57		-5	-28		-4	-18	ns		
$t_s$	Set-Up Time, CEP, CET to CP		200	115		95	50		76	35			
$t_h$	Hold Time, CEP, CET to CP		-20	-110		-10	-48		-8	-32	ns		
$t_s$	Set-Up Time, $\overline{SR}$ to CP		40	15		18	15		14	4			
$t_h$	Hold Time, $\overline{SR}$ to CP		0	-5		0	-2		0	0	ns		
$f_{MAX}$	Input Count Frequency (Note 3)		3	6		7	12		8	14	MHz	(40162B/40163B) (40162B/40163B)	

**NOTES:**

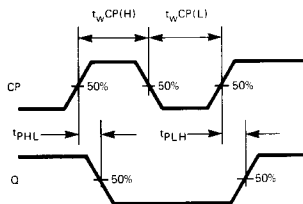
- Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
- Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.
- For  $f_{MAX}$ , input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
- It is recommended that input rise and fall times to the Clock Input be less than 15  $\mu$ s at  $V_{DD} = 5$  V, 4  $\mu$ s at  $V_{DD} = 10$  V, and 3  $\mu$ s at  $V_{DD} = 15$  V.

TYPICAL ELECTRICAL CHARACTERISTICS



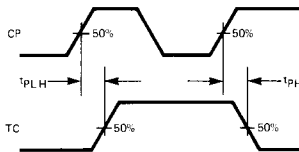
SWITCHING DIAGRAMS

CLOCK (CP) TO OUTPUT (Q)  
PROPAGATION DELAYS AND MINIMUM  
CLOCK PULSE WIDTH



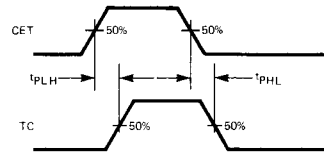
CONDITIONS:  $\overline{PE} = \overline{MR} = CEP = CET = H$   
for 40160B/40161B and  $\overline{PE} = \overline{SR} = CEP =$   
 $CET = H$  for 40162B/40163B.

CLOCK (CP) TO TERMINAL COUNT (TC)  
PROPAGATION DELAYS



CONDITIONS: See the Terminal Count  
Generation Table.  $\overline{PE} = CEP = CET = \overline{MR} =$   
 $H$  for 40160B/40161B and  $\overline{PE} = CEP = CET =$   
 $\overline{SR} = H$  for 40162B/40163B.

COUNT ENABLE TRICKLE INPUT (CET)  
TO TERMINAL COUNT OUTPUT (TC)  
PROPAGATION DELAYS

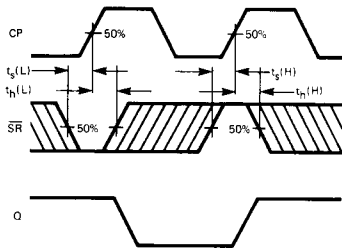


CONDITIONS: See the Terminal Count  
Generation Table.  $CP = \overline{PE} = CEP = \overline{MR} = H$   
for 40160B/40161B and  $CP = \overline{PE} = CEP =$   
 $\overline{SR} = H$  for 40162B/40163B.

SWITCHING DIAGRAMS (Continued)

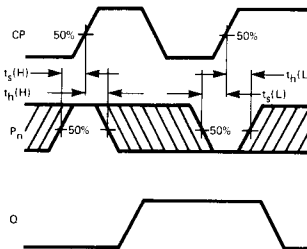
40162B/40163B

SET-UP TIMES ( $t_s$ ) AND HOLD TIMES ( $t_h$ )  
FOR SYNCHRONOUS RESET (SR).



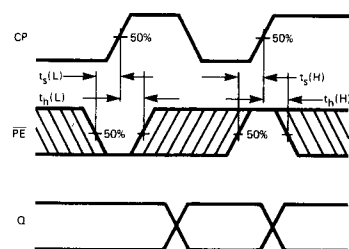
CONDITIONS:  $\overline{PE} = L, P_0-P_3 = H.$

SET-UP TIMES ( $t_s$ ) AND HOLD TIMES ( $t_h$ )  
FOR PARALLEL DATA INPUTS ( $P_0-P_3$ ).



CONDITIONS:  $\overline{PE} = L, \overline{MR} = H$  for 40160B/  
40161B and  $\overline{PE} = L, \overline{SR} = H$  for 40162B/  
40163B.

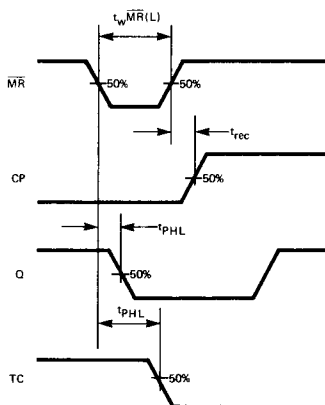
SET-UP TIMES ( $t_s$ ) AND HOLD TIMES ( $t_h$ )  
FOR PARALLEL ENABLE INPUT PE.



CONDITIONS:  $\overline{MR} = H$  for 40160B/40161B  
and  $\overline{SR} = H$  for 40162B/40163B.

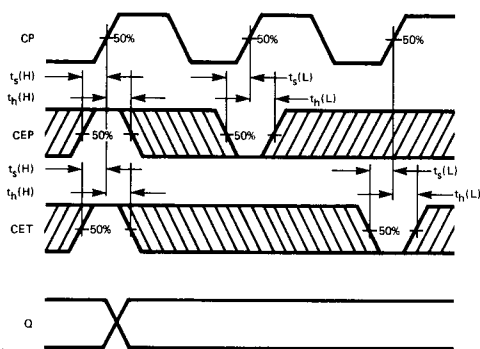
40160B/40161B

MASTER RESET ( $\overline{MR}$ ) TO OUTPUT (Q)  
DELAY, MASTER RESET PULSE WIDTH,  
MASTER RESET RECOVERY TIME, AND  
MASTER RESET TO TERMINAL COUNT  
(TC) DELAY.



CONDITIONS:  $\overline{PE} = L$  and  $P_0 = P_1 = P_2 =$   
 $P_3 = H.$

SET-UP TIMES ( $t_s$ ) AND HOLD TIMES ( $t_h$ )  
FOR COUNT ENABLE INPUTS (CEP AND  
CET).



CONDITIONS:  $\overline{PE} = \overline{MR} = H$  for 40160B/  
40161B and  $\overline{PE} = \overline{SR} = H$  for 40162B/  
40163B.

NOTE:

1. Set-up Times ( $t_s$ ) and Hold Times ( $t_h$ ) are shown as positive values, but may be specified as negative values.