

Features

- Two independent clock channels
- Frequency and Phase Sync over Packet Networks
 - Frequency accuracy performance for WCDMA-FDD, GSM, LTE-FDD and femtocell applications
 - Frequency performance for ITU-T G.823 and G.824 synchronization interface, as well as G.8261 PNT PEC and CES interfaces
 - Phase Synchronization performance for WCDMA-TDD, Mobile WiMAX, TD-SCDMA and CDMA2000 applications
- Client holdover and reference switching between multiple Servers
- Server, client and boundary clock operation
- Any input clock rate from 1 kHz to 750 MHz
- Automatic hitless reference switching and digital holdover on reference fail
- Digital PLLs filter jitter at 5.2 Hz, 14 Hz, 28 Hz, 56 Hz, 112 Hz, 224 Hz, 448 Hz or 896 Hz
- Operates from a single crystal resonator or clock oscillator

Ordering Information:

ZL30367GDG2 144 Pin LPGA Trays

 Pb Free Tin/Silver/Copper
-40°C to +85°C
 Package size: 13 x 13 mm

- Electrical phase alignment to input 1 Hz frame pulse with associated reference clock (ref/sync pairing)
- Programmable synthesizers
 - Any output clock rate from 1 Hz to 750 MHz
 - Low output jitter for 10G PHYs
 - Six LVPECL outputs and six LVCMOS outputs
- Field programmable via SPI/I²C interface

Applications

- OTN muxponders and transponders
- 10 Gigabit line cards
- Synchronous Ethernet, SONET/SDH, Fibre Channel, XAUI

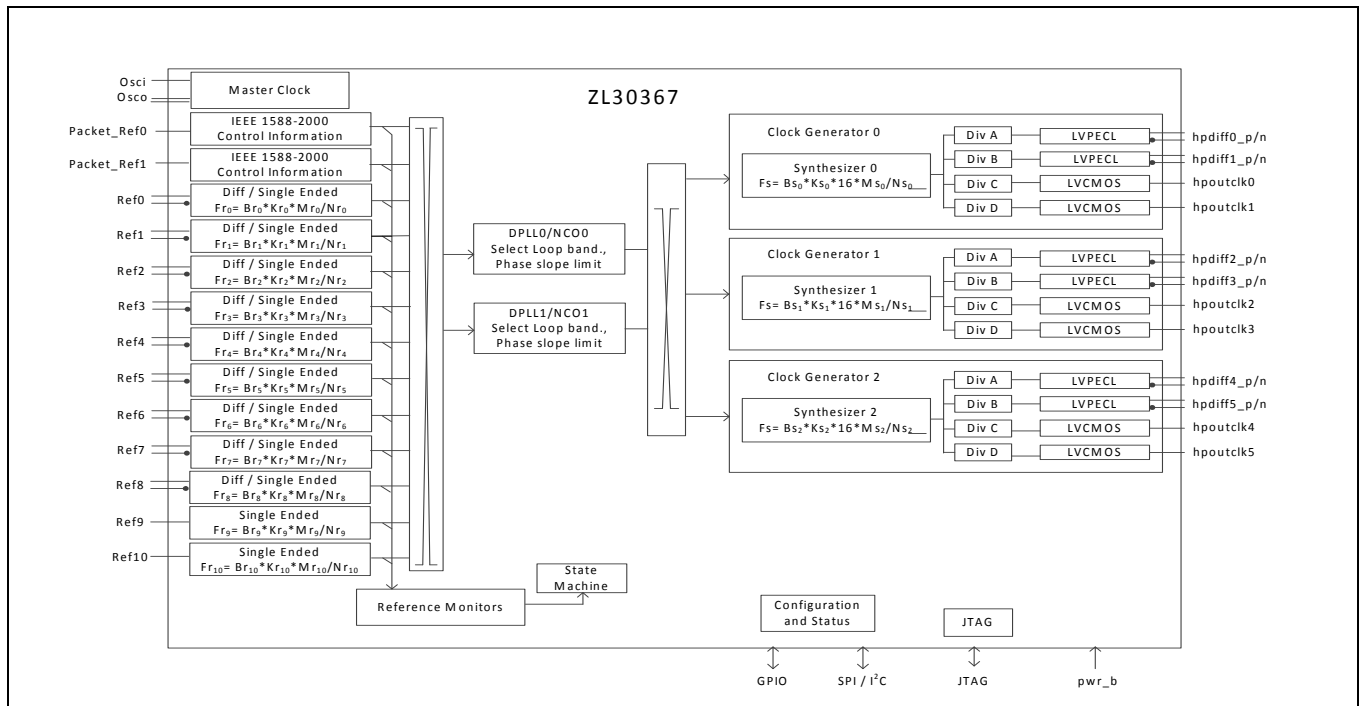


Figure 1 - Functional Block Diagram

Detailed Features

General

- Two independent clock channels
- Operates from a single crystal resonator or clock oscillator
- Configurable via SPI or I²C interface

Time Synchronization Algorithm

- External algorithm controls software digital PLL to adjust frequency & phase alignment
- Frequency, Phase and Time Synchronization over IP, MPLS and Ethernet Packet Networks
- Frequency accuracy performance for WCDMA-FDD, GSM, LTE-FDD and femtocell applications, with target performance less than ± 15 ppb.
- Frequency performance for ITU-T G.823 and G.824 synchronization interface, as well as G.8261 PNT EEC, PNT PEC and CES interface specifications.
- Phase Synchronization performance for WCDMA-TDD, Mobile WiMAX, TD-SCDMA and CDMA2000 applications with target performance less than ± 1 μ s phase alignment.
- Time Synchronization for UTC-traceability and GPS replacement.
- Client reference switching between multiple Servers
- Client holdover when Server packet connectivity is lost

Electrical Clock Inputs

- Nine input references configurable as single ended or differential and two singled ended input references
- Synchronize to any clock rate from 1 kHz to 750 MHz on differential inputs
- Synchronize to any clock rate from 1 kHz to 177.75 MHz on singled-ended inputs
- Synchronize to sync pulse and clock pair
- Flexible input reference monitoring automatically disqualifies references based on frequency and phase irregularities
 - LOS
 - Single cycle monitor
 - Precise frequency monitor
 - Coarse frequency monitor
 - Guard soak timer
- Per input clock delay compensation

Electrical Clock Engine

- Flexible two-stage architecture translates between arbitrary data rates, line coding rates and FEC rates
- Internal state machine automatically controls mode of operation (free-run, locked, holdover)
- Automatic hitless reference switching and digital holdover on reference fail
 - Physical-to-physical reference switching
 - Physical-to-packet reference switching
 - Packet-to-physical reference switching
 - Packet-to-packet reference switching

- Selectable phase slope limiting
- Supports ITU-T G.823, G.824 and G.8261 for 2048 kbit/s and 1544 kbit/s interfaces

Electrical Clock Generation

- Three programmable synthesizers
- Six LVPECL outputs
 - Two LVPECL outputs per synthesizer
 - Generate any clock rate from 1 Hz to 750 MHz
 - Low output jitter for 10G PHYs
 - Meets OC-192, STM-64, 1 GbE & 10 GbE interface jitter requirements
- Six LVCMOS outputs
 - Two LVCMOS outputs per synthesizer
 - Generate any clock rate from 1 Hz to 177.75 MHz
- Programmable output advancement/delay to accommodate trace delays or compensate for system routing paths
- Outputs may be disabled to save power

API Software

- Interfaces to 1588-capable PHY and switches with integrated timestamping
- Abstraction layer for independence from OS and CPU, from embedded SoC to home-grown
- Fits into centralized, highly integrated pizza box architectures as well as distributed architectures with multiple line cards and timing cards



**For more information about all Microsemi products
visit our Web Site at**

www.microsemi.com/timing-and-synchronization

Information relating to products and services furnished herein by Microsemi Corporation or its subsidiaries (collectively "Microsemi") is believed to be reliable. However, Microsemi assumes no liability for errors that may appear in this publication, or for liability otherwise arising from the application or use of any such information, product or service or for any infringement of patents or other intellectual property rights owned by third parties which may result from such application or use. Neither the supply of such information or purchase of product or service conveys any license, either express or implied, under patents or other intellectual property rights owned by Microsemi or licensed from third parties by Microsemi, whatsoever. Purchasers of products are also hereby notified that the use of product in certain ways or in combination with Microsemi, or non-Microsemi furnished goods or services may infringe patents or other intellectual property rights owned by Microsemi.

This publication is issued to provide information only and (unless agreed by Microsemi in writing) may not be used, applied or reproduced for any purpose nor form part of any order or contract nor to be regarded as a representation relating to the products or services concerned. The products, their specifications, services and other information appearing in this publication are subject to change by Microsemi without notice. No warranty or guarantee express or implied is made regarding the capability, performance or suitability of any product or service. Information concerning possible methods of use is provided as a guide only and does not constitute any guarantee that such methods of use will be satisfactory in a specific piece of equipment. It is the user's responsibility to fully determine the performance and suitability of any equipment using such information and to ensure that any publication or data used is up to date and has not been superseded. Manufacturing does not necessarily include testing of all functions or parameters. These products are not suitable for use in any medical **and other** products whose failure to perform may result in significant injury or death to the user. All products and materials are sold and services provided subject to Microsemi's conditions of sale which are available on request.

Purchase of Microsemi's I2C components conveys a license under the Philips I2C Patent rights to use these components in an I2C System, provided that the system conforms to the I2C Standard Specification as defined by Philips.

Microsemi, ZL, and combinations thereof, VoiceEdge, VoicePort, SLAC, ISLIC, ISLAC and VoicePath are trademarks of Microsemi Corporation.

TECHNICAL DOCUMENTATION - NOT FOR RESALE
