2.7 V to 5.5 V Input, 3.0 A Integrated MOSFET Single Synchronous Buck DC/DC Converter

BD9B305QUZ

General Description

BD9B305QUZ is a synchronous buck DC/DC converter with built-in low on-resistance power MOSFETs. It is capable of providing current up to 3 A. It features fast transient response due to constant on-time control system. The Light Load Mode control improves efficiency in light-load conditions. It is ideal for reducing standby power consumption of equipment. Power Good function makes it possible for system to control sequence. It achieves the high power density and offer a small footprint on the PCB by employing small package.

Key Specifications

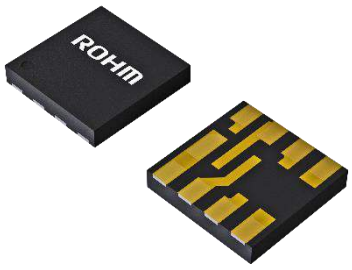
- Input Voltage Range: 2.7 V to 5.5 V
- Output Voltage Range: 0.6 V to V_{IN} x 0.8 V
- Output Current: 3.0 A (Max)
- Switching Frequency: 1 MHz (Typ)
- High-Side FET ON Resistance: 50 mΩ (Typ)
- Low-Side FET ON Resistance: 40 mΩ (Typ)
- Shutdown Current: 0 µA (Typ)

Package

Package	W (Typ) x D (Typ) x H (Max)
VMMP08LZ2020	2.00 mm x 2.00 mm x 0.40 mm

Features

- Single Synchronous Buck DC/DC Converter
- Constant On-time Control
- Light Load Mode Control
- Adjustable Soft Start
- Power Good Output
- Output Capacitor Discharge Function
- Over Voltage Protection (OVP)
- Over Current Protection (OCP)
- Short Circuit Protection (SCP)
- Thermal Shutdown Protection (TSD)
- Under Voltage Lockout Protection (UVLO)
- VMMP08LZ2020 Package
  Backside Heat Dissipation
  0.5 mm Pitch

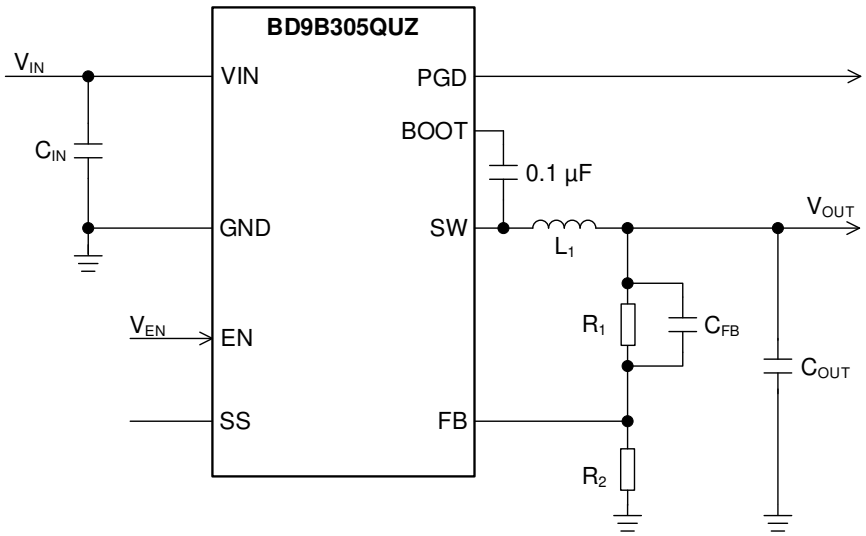


VMMP08LZ2020

Applications

- Step-down Power Supply for SoC, FPGA, Microprocessor
- Laptop PC / Tablet PC / Server
- LCD TV
- Storage Device (HDD / SSD)
- Printer, OA Equipment
- Distributed Power Supply, Secondary Power Supply

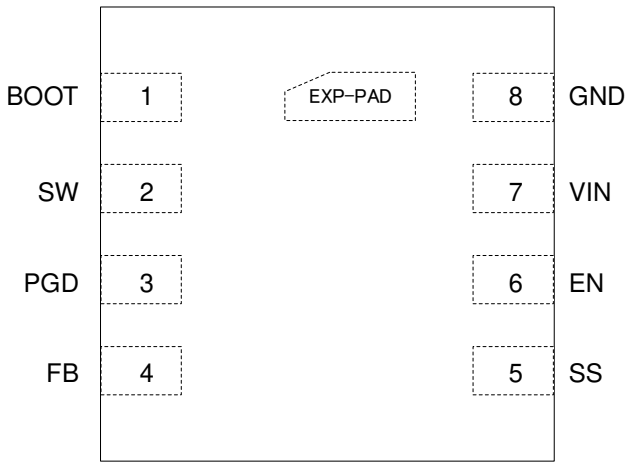
Typical Application Circuit



○Product structure : Silicon integrated circuit ○This product has no designed protection against radioactive rays.

Pin Configuration

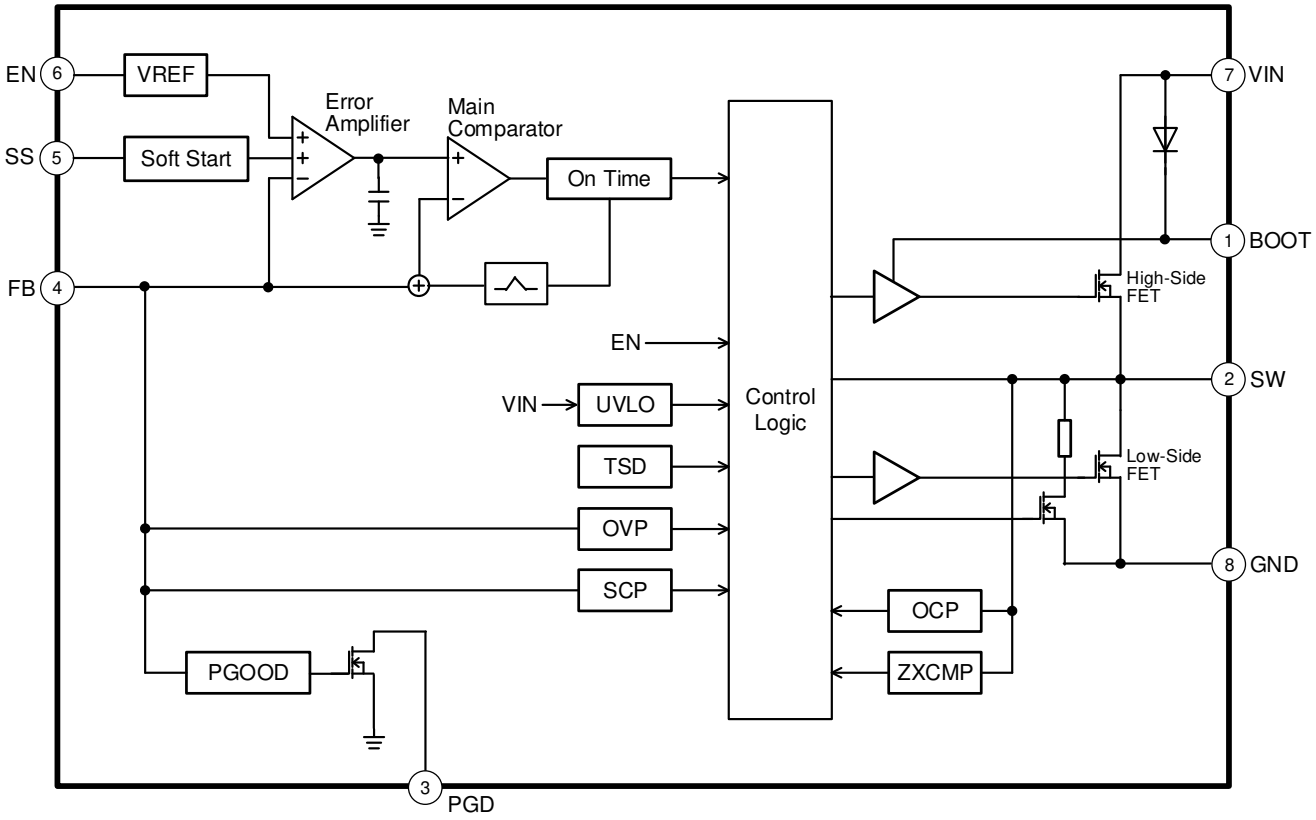
(TOP VIEW)



Pin Descriptions

Pin No.	Pin Name	Function
1	BOOT	Pin for bootstrap. Connect a bootstrap capacitor of 0.1 µF between this pin and the SW pin. The voltage of this pin is the gate drive voltage of the High-Side FET.
2	SW	Switch pin. This pin is connected to the source of the High-Side FET and the drain of the Low-Side FET. Connect a bootstrap capacitor of 0.1 µF between this pin and the BOOT pin. In addition, connect an inductor considering the direct current superimposition characteristic.
3	PGD	Power Good pin. This pin is an open drain output that requires a pull-up resistor. See page 17 for setting the resistance. If not used, this pin can be left floating or connected to the ground.
4	FB	Output voltage feedback pin. See page 31 for how to calculate the resistances of the output voltage setting.
5	SS	Pin for setting the soft start time of output voltage. The soft start time is 1 ms (Typ) when the SS pin is left floating. A ceramic capacitor connected to the SS pin makes the soft start time more than 1 ms. See page 31 for how to calculate the capacitance.
6	EN	Enable pin. The device starts up with setting V_{EN} to 0.920 V (Typ) or more. The device enters the shutdown mode with setting V_{EN} to 0.875 V (Typ) or less. This pin must be terminated.
7	VIN	Power supply pin. Connecting 0.1 µF (Typ) and 22 µF (Typ) ceramic capacitors is recommended. The detail of a selection is described in page 31.
8	GND	Ground pin.
-	EXP-PAD	A backside heat dissipation exposed pad. Connecting to the PCB power ground plane by using thermal vias provides excellent heat dissipation characteristics. See page 34 to 35 for the detailed PCB layout design.

Block Diagram



Description of Blocks

1. VREF
   The VREF block generates the internal reference voltage.

2. Soft Start
   The Soft Start circuit slows down the rise of output voltage during start-up and controls the current, which allows the prevention of output voltage overshoot and inrush current. The internal soft start time is 1 ms (Typ) when the SS pin is left floating. A capacitor connected to the SS pin makes the rising time more than 1 ms.

3. Error Amplifier
   The Error Amplifier adjusts the Main Comparator input voltage to make the internal reference voltage equal to FB voltage.

4. Main Comparator
   The Main Comparator compares the Error Amplifier output voltage and FB voltage (V_{FB}). When V_{FB} becomes lower than the Error Amplifier output voltage, the output turns high and reports to the On Time block that the output voltage has dropped below the control voltage.

5. On Time
   This block generates On Time. The designed On Time is generated after the Main Comparator output turns high. The On Time is adjusted to control the frequency to be fixed even with I/O voltage is changed.

6. PGOOD
   The PGOOD block is for power good function. When the output voltage reaches within ±10 % (Typ) of the setting voltage, the built-in open drain Nch MOSFET connected to the PGD pin is turned off and the PGD pin becomes Hi-Z (High impedance). When the output voltage reaches outside ±15 % (Typ) of the setting voltage, the open drain Nch MOSFET is turned on and PGD pin is pulled down with 100 Ω (Typ).

7. UVLO
   The UVLO block is for under voltage lockout protection. The device is shut down when input voltage (V_{IN}) falls to 2.45 V (Typ) or less. The threshold voltage has the 100 mV (Typ) hysteresis.

8. TSD
   The TSD block is for thermal protection. The device is shut down when the junction temperature Tj reaches to 175 °C (Typ) or more. The device is automatically restored to normal operation with a hysteresis of 25 °C (Typ) when the Tj goes down.

9. OVP
   The OVP block is for output over voltage protection. When the FB voltage (V_{FB}) exceeds 115 % (Typ) or more of FB threshold voltage V_{FBTH}, the output MOSFETs are turned off. After V_{FB} falls 110 % (Typ) or less of V_{FBTH}, the output MOSFETs are returned to normal operation condition.

10. OCP
    The OCP block is for over current protection. This function operates by limiting the current that flows through the High-Side FET and the Low-Side FET at each cycle of the switching frequency.

11. SCP
    The SCP is for short circuit protection. When 256 times OCP are counted on the condition where the device completes the soft start and the output voltage falls below 85 % (Typ) of the setting voltage, the device is shut down for 128 ms (Typ). After 128 ms shutdown, the device restarts. (HICCUP operation)

12. ZXCMP
    The ZXCMP is a comparator that monitors the inductor current. When inductor current falls below 0A (Typ) while the Low-Side FET is on, it turns the FET off.

13. Control Logic
    The Control Logic controls the switching operation and protection function operation.

Absolute Maximum Ratings (Ta = 25 °C)

Parameter	Symbol	Rating	Unit
Input Voltage	V_{IN}	-0.3 to +7	V
EN Voltage	V_{EN}	-0.3 to +V_{IN}	V
FB Voltage	V_{FB}	-0.3 to +7	V
SS Voltage	V_{SS}	-0.3 to +V_{IN}	V
PGD Voltage	V_{PGD}	-0.3 to +7	V
SW Voltage	V_{SW}	-0.3 to V_{IN} + 0.3	V
Voltage from GND to BOOT	V_{BOOT}	-0.3 to +14	V
Voltage from SW to BOOT	$\Delta V_{BOOT-SW}$	-0.3 to +7	V
Output Current	I_{OUT}	3.5	A
Maximum Junction Temperature	Tjmax	150	°C
Storage Temperature Range	Tstg	-55 to +150	°C

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

Caution 2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*

Thermal Resistance *(Note 1)*

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s *(Note 3)*	2s2p *(Note 4)*	
VMMP08LZ2020				
Junction to Ambient	θ_{JA}	208.30	90.30	°C/W
Junction to Top Characterization Parameter *(Note 2)*	Ψ_{JT}	28.00	22.00	°C/W

(Note 1) Based on JESD51-2A (Still-Air).
(Note 2) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 3) Using a PCB board based on JESD51-3.
(Note 4) Using a PCB board based on JESD51-5, 7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70 µm

Layer Number of Measurement Board	Material	Board Size	Thermal Via *(Note 5)*	
			Pitch	Diameter
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt	1.20 mm	Φ0.30 mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 µm	74.2 mm x 74.2 mm	35 µm	74.2 mm x 74.2 mm	70 µm

(Note 5) This thermal via connects with the copper pattern of all layers.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input Voltage	V_{IN}	2.7	-	5.5	V
Operating Temperature *(Note 1)*	Ta	-40	-	+85	°C
Output Current *(Note 1)*	I_{OUT}	0	-	3.0	A
Output Voltage Setting	V_{OUT}	0.6	-	V_{IN} x 0.8	V

(Note 1) Tj must be lower than 150 °C under the actual operating environment.

Electrical Characteristics (Unless otherwise specified Ta = 25 °C, V_{IN} = 5 V, V_{EN} = 5 V)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Input Supply						
Shutdown Current	I_{SDN}	-	0	10	µA	V_{EN} = 0 V
Quiescent Current at No Load	I_Q	-	15	30	µA	I_{OUT} = 0 A, No switching
UVLO Detection Threshold Voltage	V_{UVLO1}	2.350	2.450	2.550	V	V_{IN} falling
UVLO Release Threshold Voltage	V_{UVLO2}	2.425	2.550	2.700	V	V_{IN} rising
UVLO Hysteresis Voltage	$V_{UVLOHYS}$	50	100	200	mV	
Enable						
EN Threshold Voltage High	V_{ENH}	0.875	0.920	0.965	V	V_{EN} rising
EN Threshold Voltage Low	V_{ENL}	0.830	0.875	0.920	V	V_{EN} falling
EN Hysteresis Voltage	V_{ENHYS}	27	45	63	mV	
EN Input Current	I_{EN}	-	0	10	µA	V_{EN} = 5 V
Reference Voltage, Error Amplifier, Soft Start						
FB Threshold Voltage	V_{FBTH}	0.591	0.600	0.609	V	PWM mode
FB Input Current	I_{FB}	-	-	100	nA	V_{FB} = 0.6 V
Soft Start Time	t_{SS}	0.6	1.0	1.4	ms	SS pin is left floating.
Soft Start Charge Current	I_{SS}	0.6	1.0	1.4	µA	
On Time						
On Time	t_{ON}	270	360	450	ns	V_{OUT} = 1.8 V, PWM mode
SW (MOSFET)						
High-Side FET ON Resistance	R_{ONH}	-	50	100	mΩ	V_{BOOT} - V_{SW} = 5 V
Low-Side FET ON Resistance	R_{ONL}	-	40	80	mΩ	
High-Side FET Leakage Current	I_{LKH}	-	0	10	µA	No switching
Low-Side FET Leakage Current	I_{LKL}	-	0	10	µA	No switching
Power Good						
Power Good Rising Threshold Voltage	V_{PGDGR}	85	90	95	%	V_{FB} rising, V_{PGDGR} = V_{FB} / V_{FBTH} x 100
Power Good Falling Threshold Voltage	V_{PGDGF}	105	110	115	%	V_{FB} falling, V_{PGDGF} = V_{FB} / V_{FBTH} x 100
Power Fault Rising Threshold Voltage	V_{PGDFR}	110	115	120	%	V_{FB} rising, V_{PGDFR} = V_{FB} / V_{FBTH} x 100
Power Fault Falling Threshold Voltage	V_{PGDFF}	80	85	90	%	V_{FB} falling, V_{PGDFF} = V_{FB} / V_{FBTH} x 100
PGD Output Leakage Current	I_{LKPGD}	-	0	5	µA	V_{PGD} = 5 V
PGD MOSFET ON Resistance	R_{PGD}	-	100	200	Ω	
PGD Output Low Level Voltage	V_{PGDL}	-	0.1	0.2	V	I_{PGD} = 1 mA

Typical Performance Curves

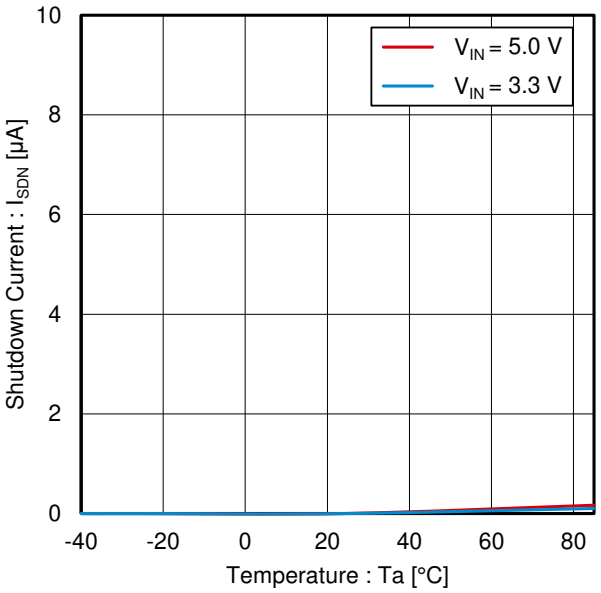


Figure 1. Shutdown Current vs Temperature

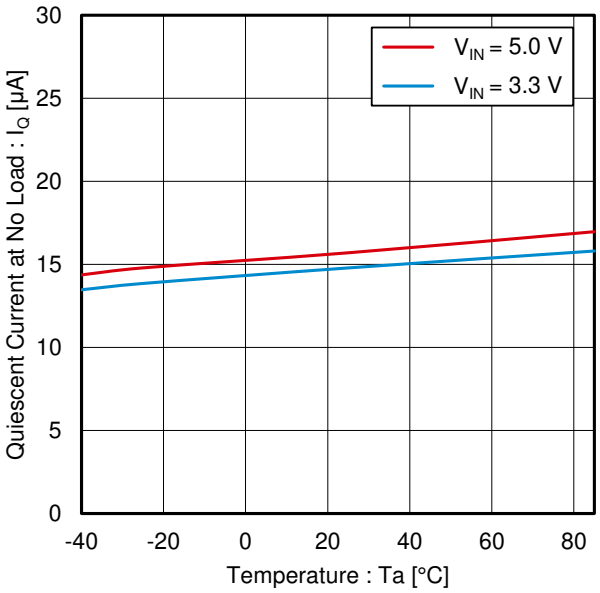


Figure 2. Quiescent Current at No Load vs Temperature

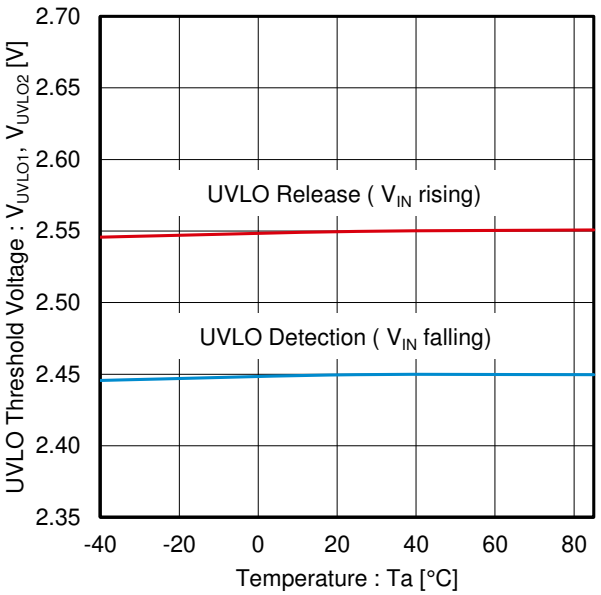


Figure 3. UVLO Threshold Voltage vs Temperature

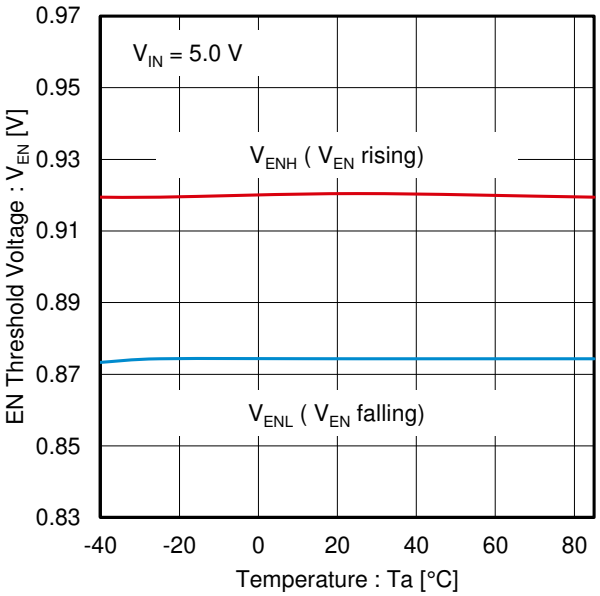


Figure 4. EN Threshold Voltage vs Temperature

Typical Performance Curves – continued

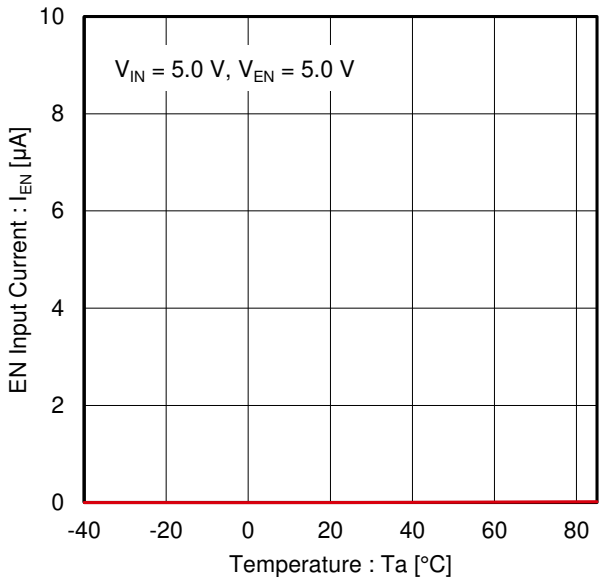


Figure 5. EN Input Current vs Temperature

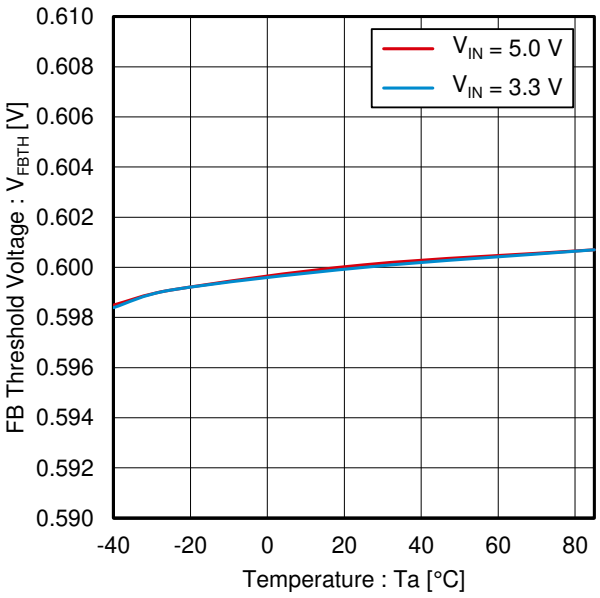


Figure 6. FB Threshold Voltage vs Temperature

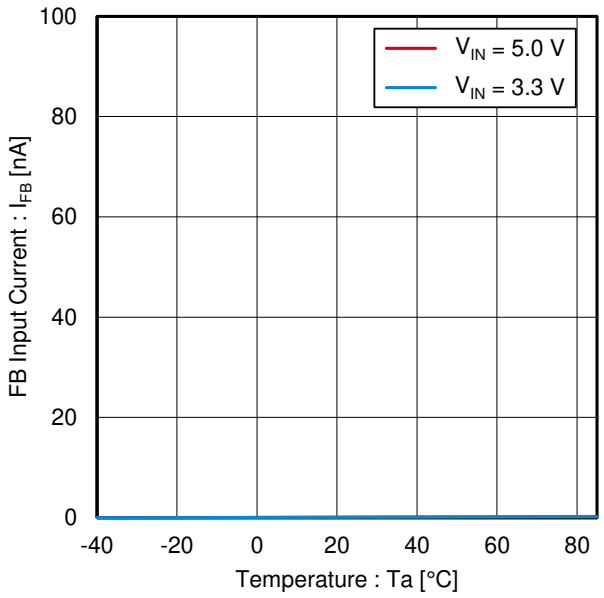


Figure 7. FB Input Current vs Temperature

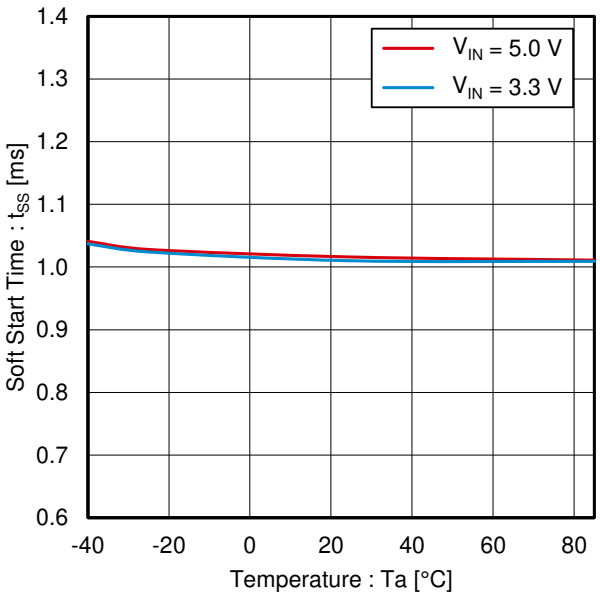


Figure 8. Soft Start Time vs Temperature
(SS pin is left floating.)

Typical Performance Curves – continued

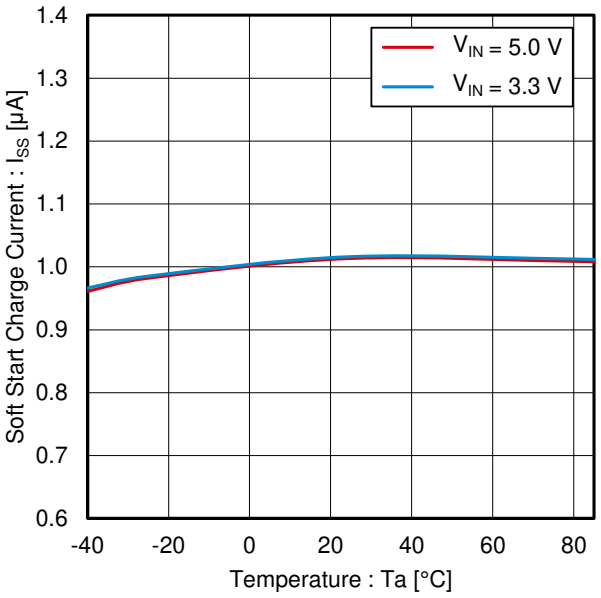


Figure 9. Soft Start Charge Current vs Temperature

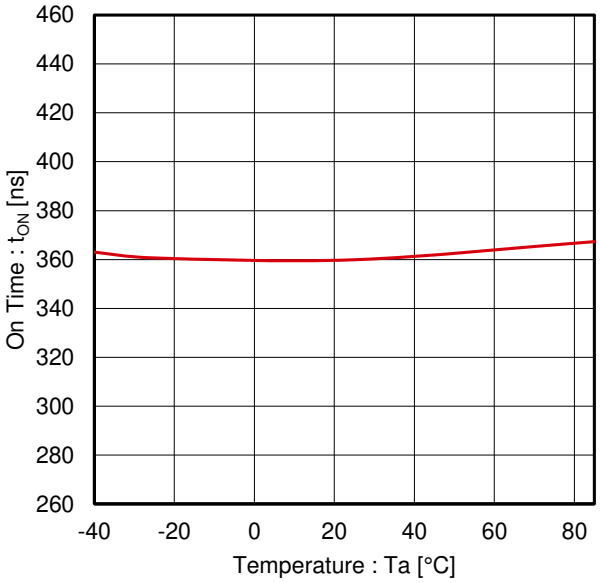


Figure 10. On Time vs Temperature
(V_{IN} = 5.0 V, V_{OUT} = 1.8 V, I_{OUT} = 1.0 A)

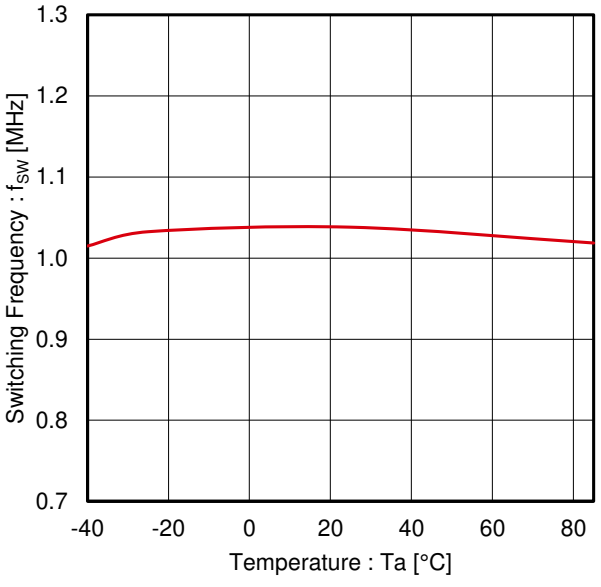


Figure 11. Switching Frequency vs Temperature
(V_{IN} = 5.0 V, V_{OUT} = 1.8 V, I_{OUT} = 1.0 A)

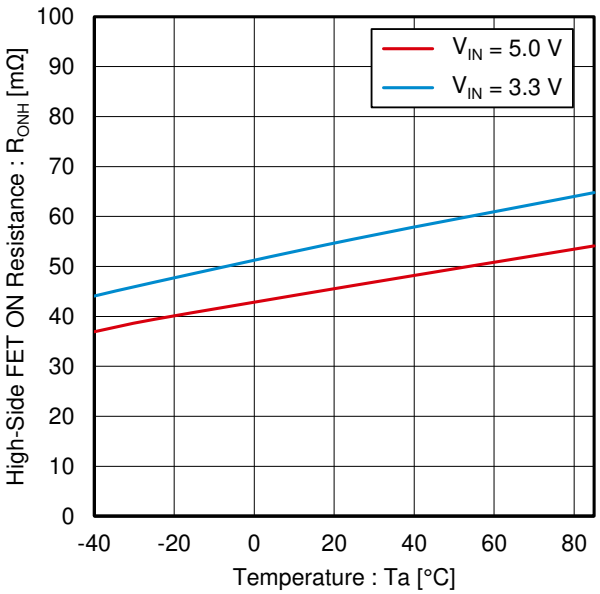


Figure 12. High-Side FET ON Resistance vs Temperature

Typical Performance Curves – continued

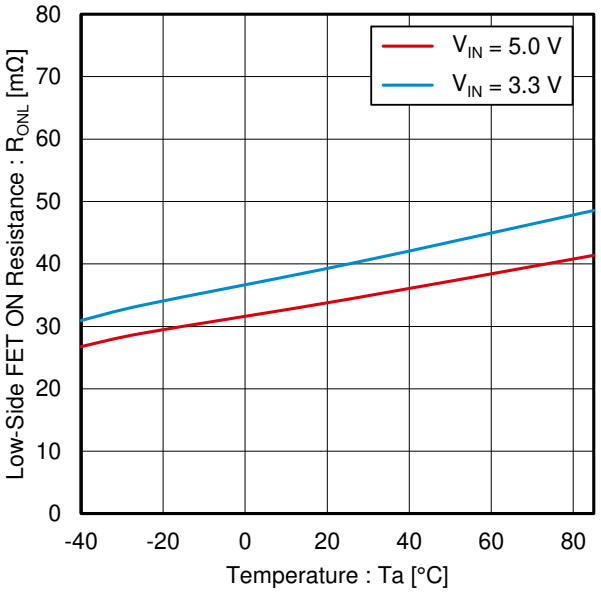


Figure 13. Low-Side FET ON Resistance vs Temperature

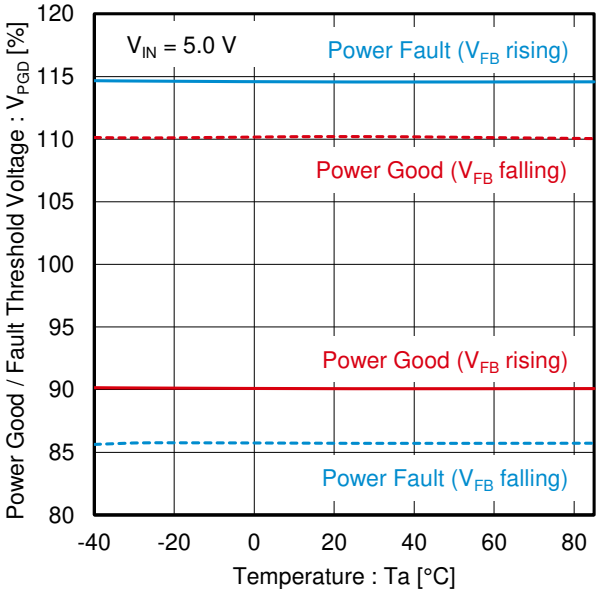


Figure 14. Power Good / Fault Threshold Voltage vs Temperature

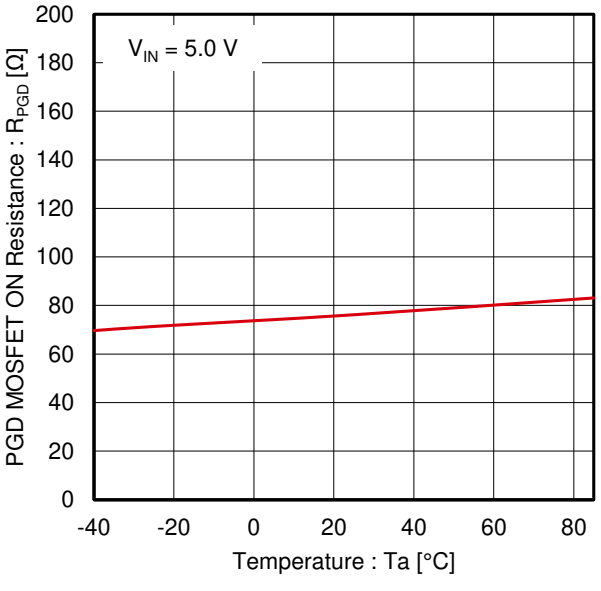


Figure 15. PGD MOSFET ON Resistance vs Temperature

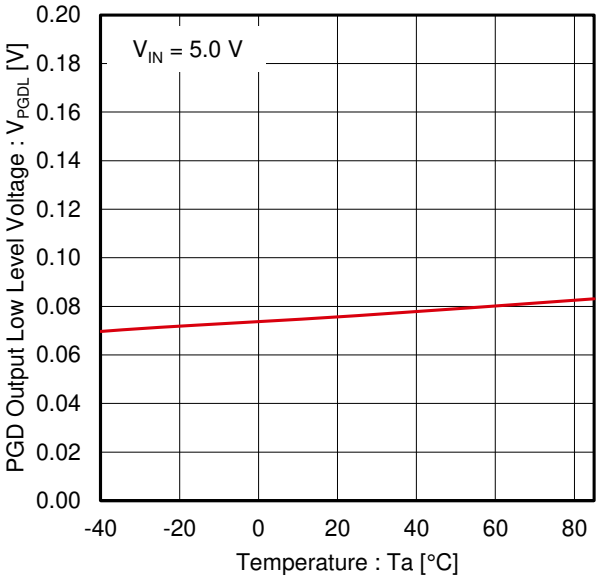


Figure 16. PGD Output Low Level Voltage vs Temperature

Typical Performance Curves – continued

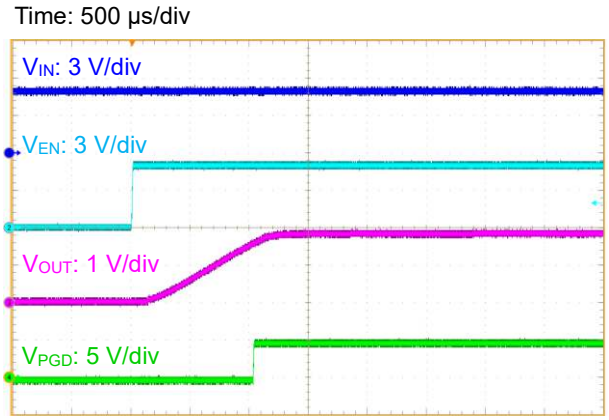


Figure 17. Start-up at No Load: V_{EN} = 0 V to 5 V
(V_{IN} = 5.0 V, V_{OUT} = 1.8 V, C_{SS} = OPEN)

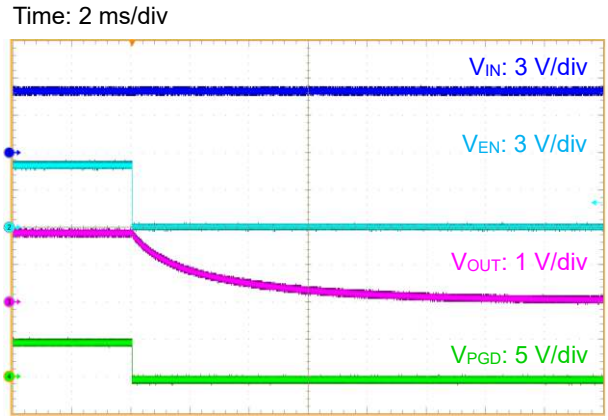


Figure 18. Shutdown at No Load: V_{EN} = 5 V to 0 V
(V_{IN} = 5.0 V, V_{OUT} = 1.8 V, C_{SS} = OPEN)

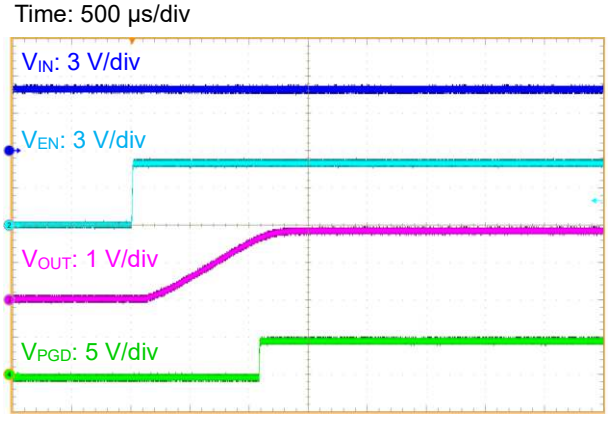


Figure 19. Start-up at R_{Load} = 0.6 Ω: V_{EN} = 0 V to 5 V
(V_{IN} = 5.0 V, V_{OUT} = 1.8 V, C_{SS} = OPEN)

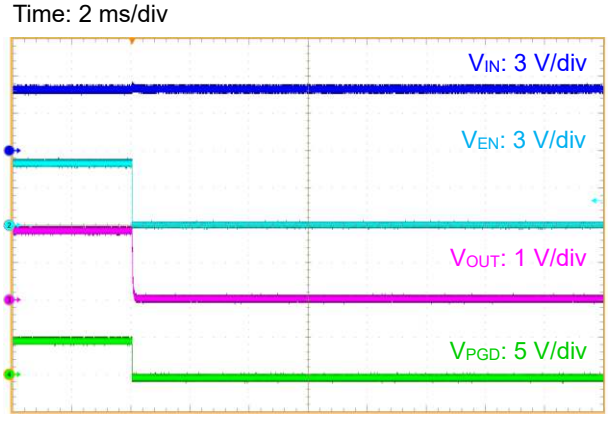


Figure 20. Shutdown at R_{Load} = 0.6 Ω: V_{EN} = 5 V to 0 V
(V_{IN} = 5.0 V, V_{OUT} = 1.8 V, C_{SS} = OPEN)

Typical Performance Curves – continued

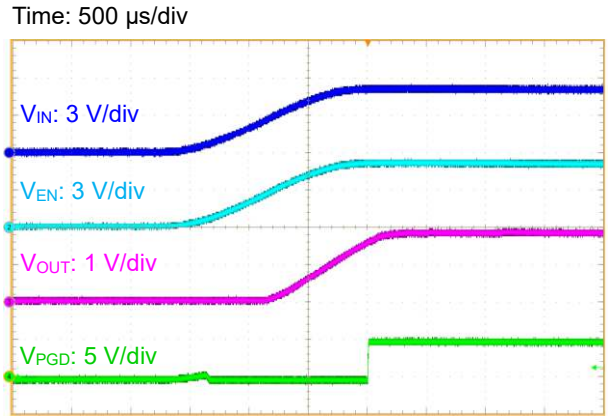


Figure 21. Start-up at No Load: V_{IN} = V_{EN} = 0 V to 5 V (V_{OUT} = 1.8 V, C_{SS} = OPEN)

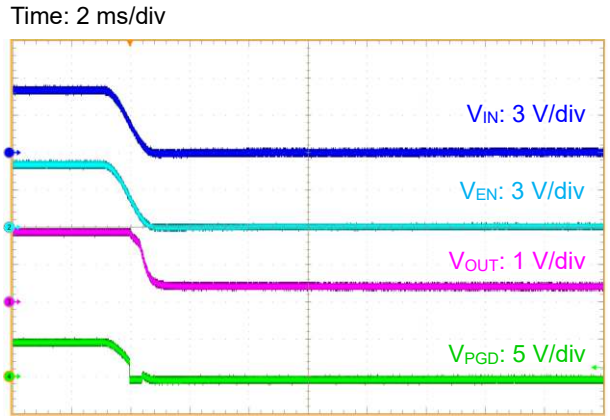


Figure 22. Shutdown at No Load: V_{IN} = V_{EN} = 5 V to 0 V (V_{OUT} = 1.8 V, C_{SS} = OPEN)

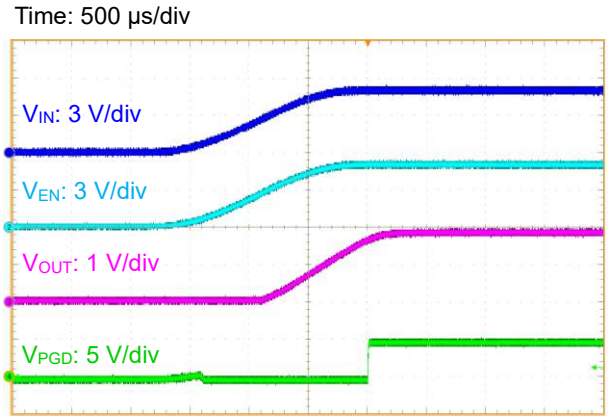


Figure 23. Start-up at R_{Load} = 0.6 Ω: V_{IN} = V_{EN} = 0 V to 5 V (V_{OUT} = 1.8 V, C_{SS} = OPEN)

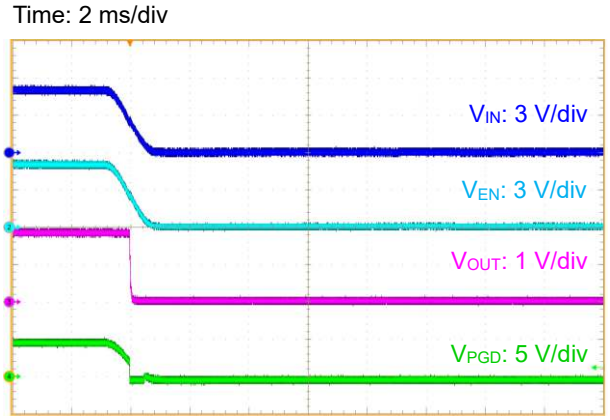


Figure 24. Shutdown at R_{Load} = 0.6 Ω: V_{IN} = V_{EN} = 5 V to 0 V (V_{OUT} = 1.8 V, C_{SS} = OPEN)

Typical Performance Curves – continued

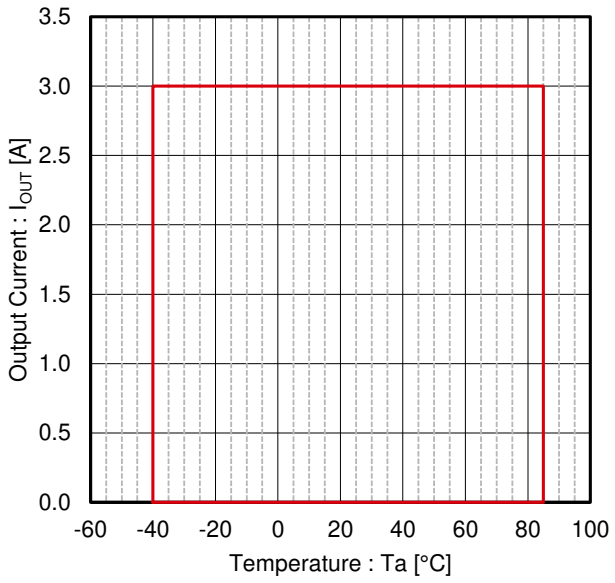


Figure 25. Output Current vs Temperature *(Note 1)*
Operating Range: Tj < 150 °C (V_{IN} = 5.0 V, V_{OUT} = 1.8 V)

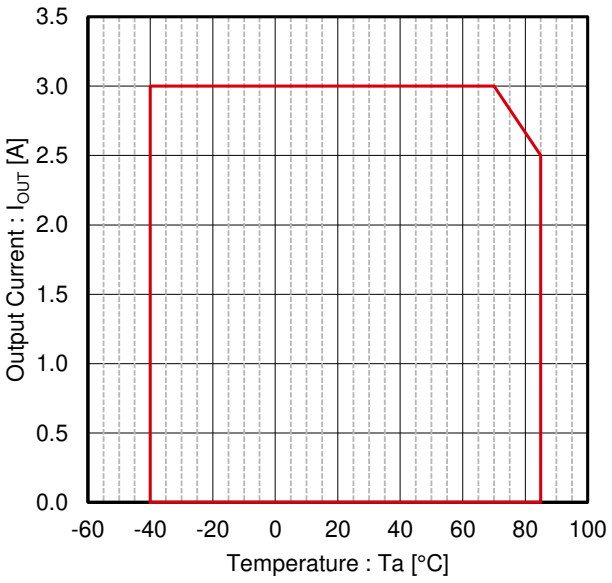


Figure 26. Output Current vs Temperature *(Note 1)*
Operating Range: Tj < 150 °C (V_{IN} = 3.3 V, V_{OUT} = 1.8 V)

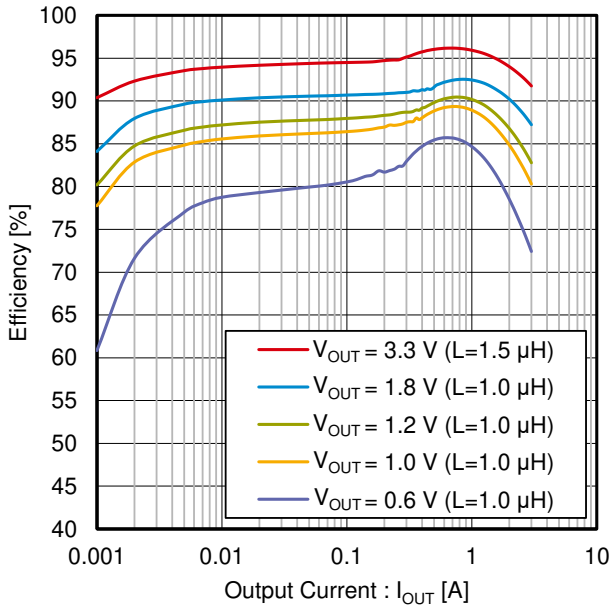


Figure 27. Efficiency vs Output Current
(V_{IN} = 5.0 V, L: FDSD0518 series; Murata)

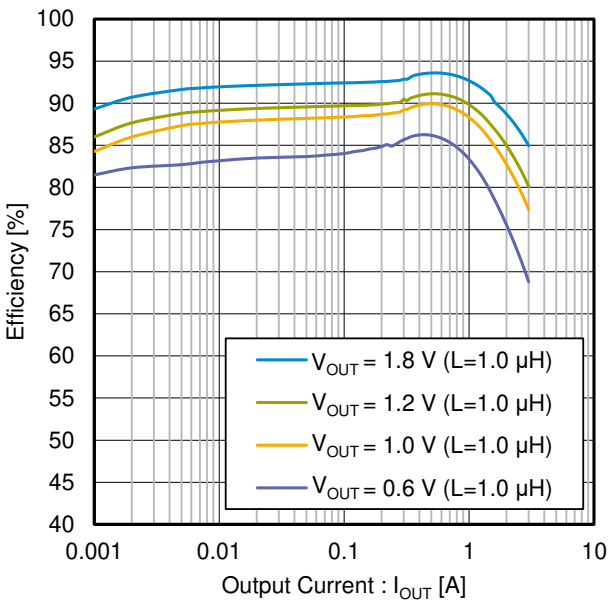


Figure 28. Efficiency vs Output Current
(V_{IN} = 3.3 V, L: FDSD0518 series; Murata)

(Note 1) Measured on FR-4 board 67.5 mm x 67.5 mm, Copper Thickness: Top and Bottom 70 µm, 2 Internal Layers 35 µm.

Typical Performance Curves – continued

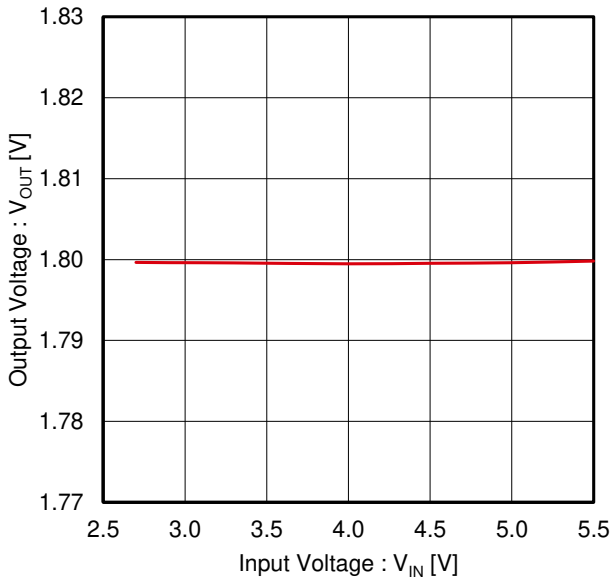


Figure 29. Output Voltage vs Input Voltage (Line Regulation)
(V_{OUT} = 1.8 V, I_{OUT} = 1.0 A)

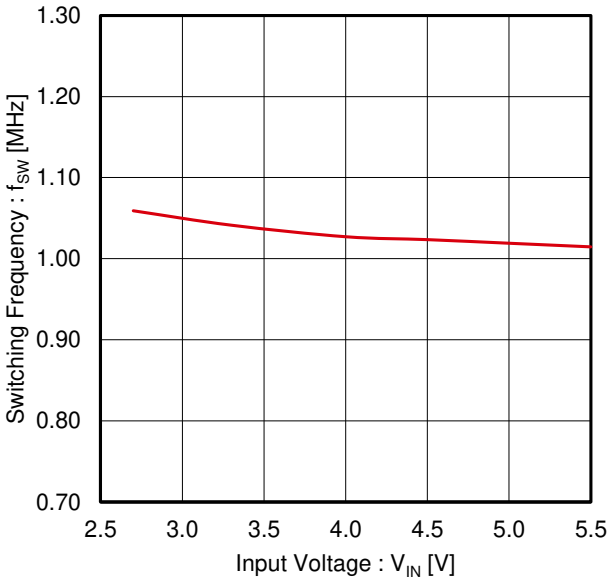


Figure 30. Switching Frequency vs Input Voltage
(V_{OUT} = 1.8 V, I_{OUT} = 1.0 A)

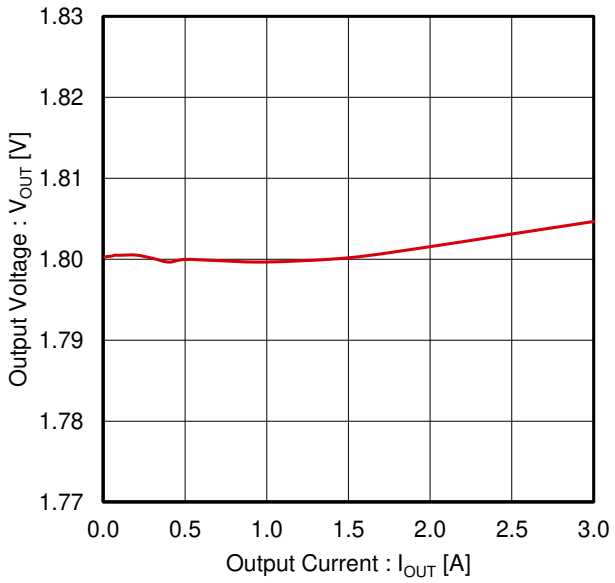


Figure 31. Output Voltage vs Output Current (Load Regulation)
(V_{IN} = 5.0 V, V_{OUT} = 1.8 V)

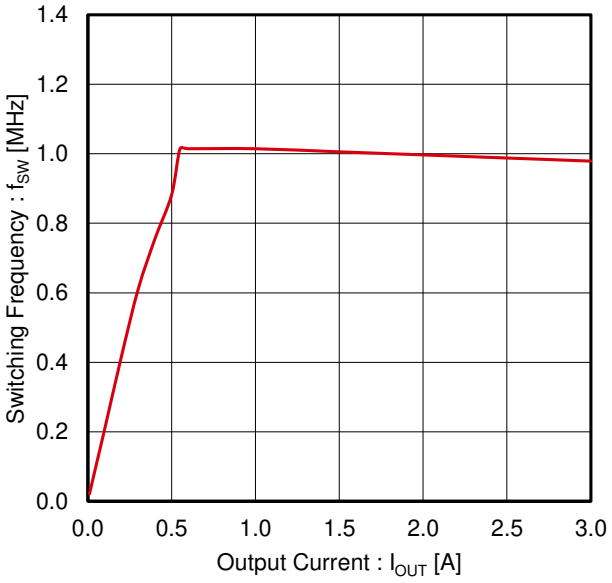


Figure 32. Switching Frequency vs Output Current
(V_{IN} = 5.0 V, V_{OUT} = 1.8 V)

Typical Performance Curves – continued

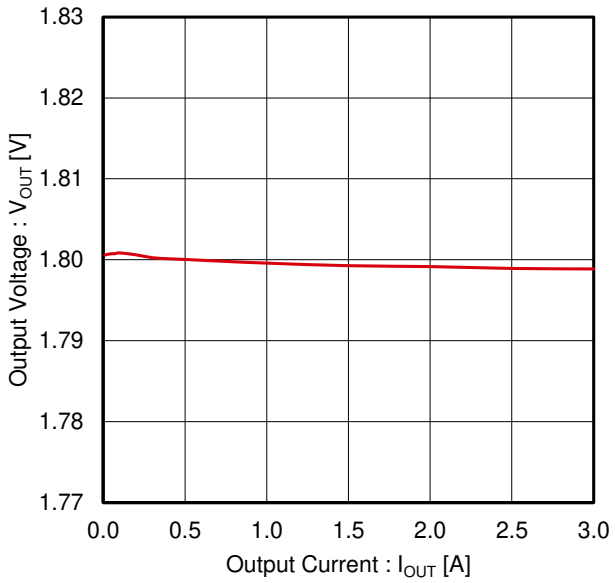


Figure 33. Output Voltage vs Output Current (Load Regulation)
(V_{IN} = 3.3 V, V_{OUT} = 1.8 V)

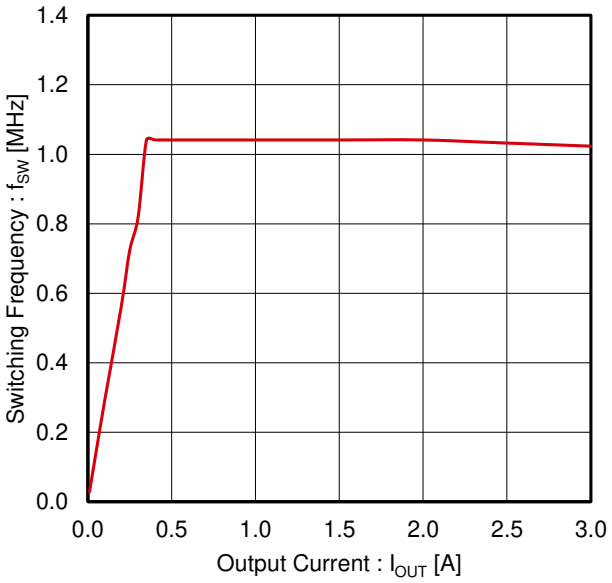


Figure 34. Switching Frequency vs Output Current
(V_{IN} = 3.3 V, V_{OUT} = 1.8 V)

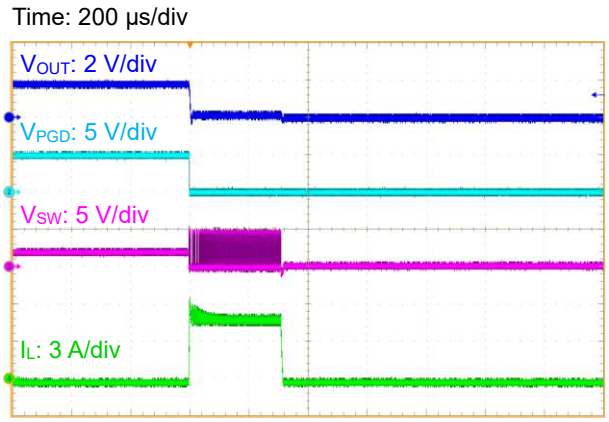


Figure 35. OCP Operation (V_{IN} = 5.0 V, V_{OUT} = 1.8 V to 0 V)

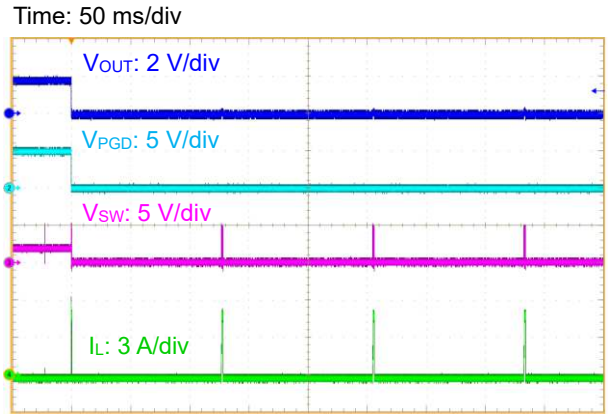


Figure 36. SCP Operation (V_{IN} = 5.0 V, V_{OUT} = 1.8 V to 0 V)

Function Explanations

1. Basic Operation

(1) DC/DC Converter Operation

BD9B305QUZ is a synchronous buck DC/DC converter that achieves faster load transient response due to constant on-time control. The device performs switching operation in PWM (Pulse Width Modulation) control at heavy load. It operates in Light Load Mode control at lighter load to improve efficiency.

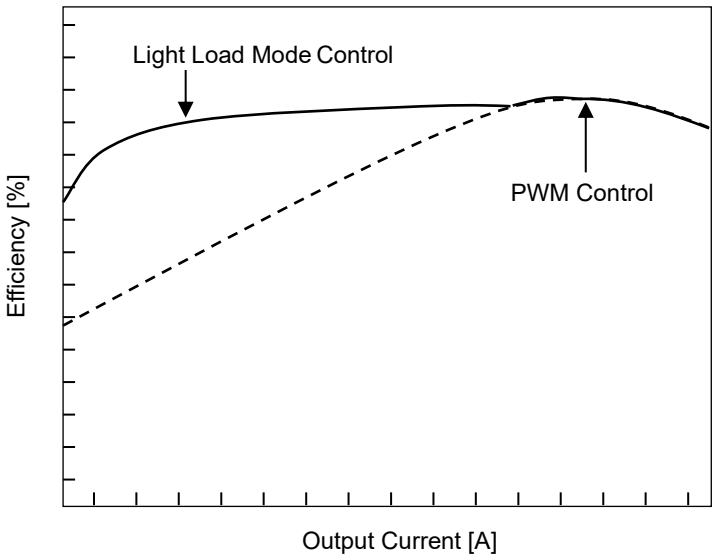


Figure 37. Efficiency Image between Light Load Mode Control and PWM Control

(2) Enable Control

The startup and shutdown can be controlled by the EN voltage (V_{EN}). When V_{EN} becomes 0.920 V (Typ) or more, the internal circuit is activated and the device starts up. When V_{EN} becomes 0.875 V (Typ) or less, the device is shut down. In this shutdown mode, the High-Side FET and the Low-Side FET are turned off and the SW pin is connected to GND through an internal resistor 100 Ω (Typ) to discharge the output. The start-up with V_{EN} must be at the same time of the input voltage V_{IN} (V_{IN} = V_{EN}) or after supplying V_{IN}.

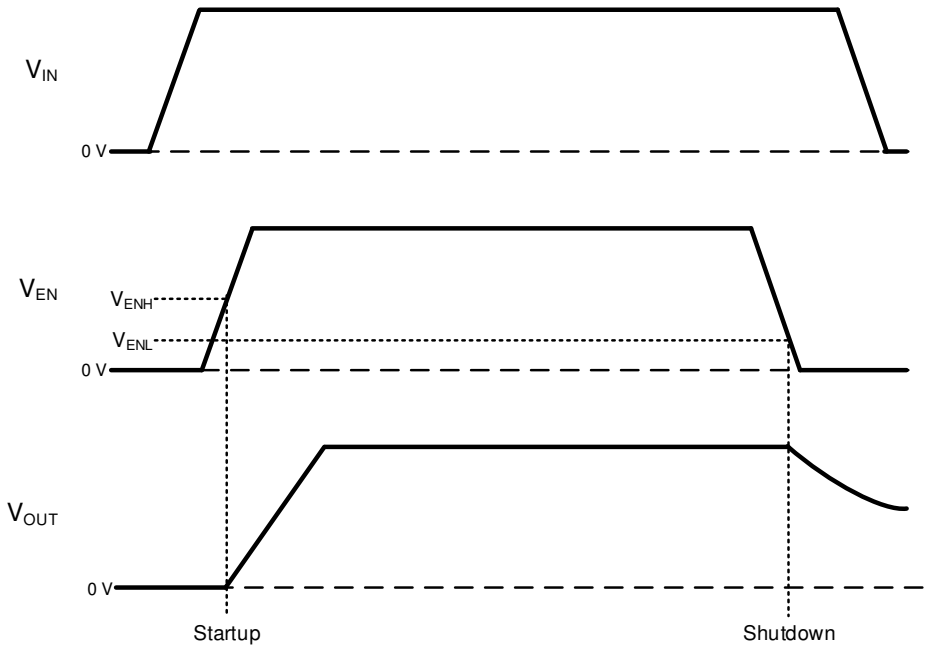


Figure 38. Startup and Shutdown with Enable Control Timing Chart

Function Explanations – continued

(3) Soft Start

When V_{EN} goes high, soft start function operates and output voltage gradually rises. This soft start function can prevent overshoot of the output voltage and excessive inrush current. The soft start time t_{SS} is 1 ms (Typ) when the SS pin is left floating. A capacitor connected to the SS pin makes t_{SS} more than 1 ms. See page 31 for how to set the soft start time.

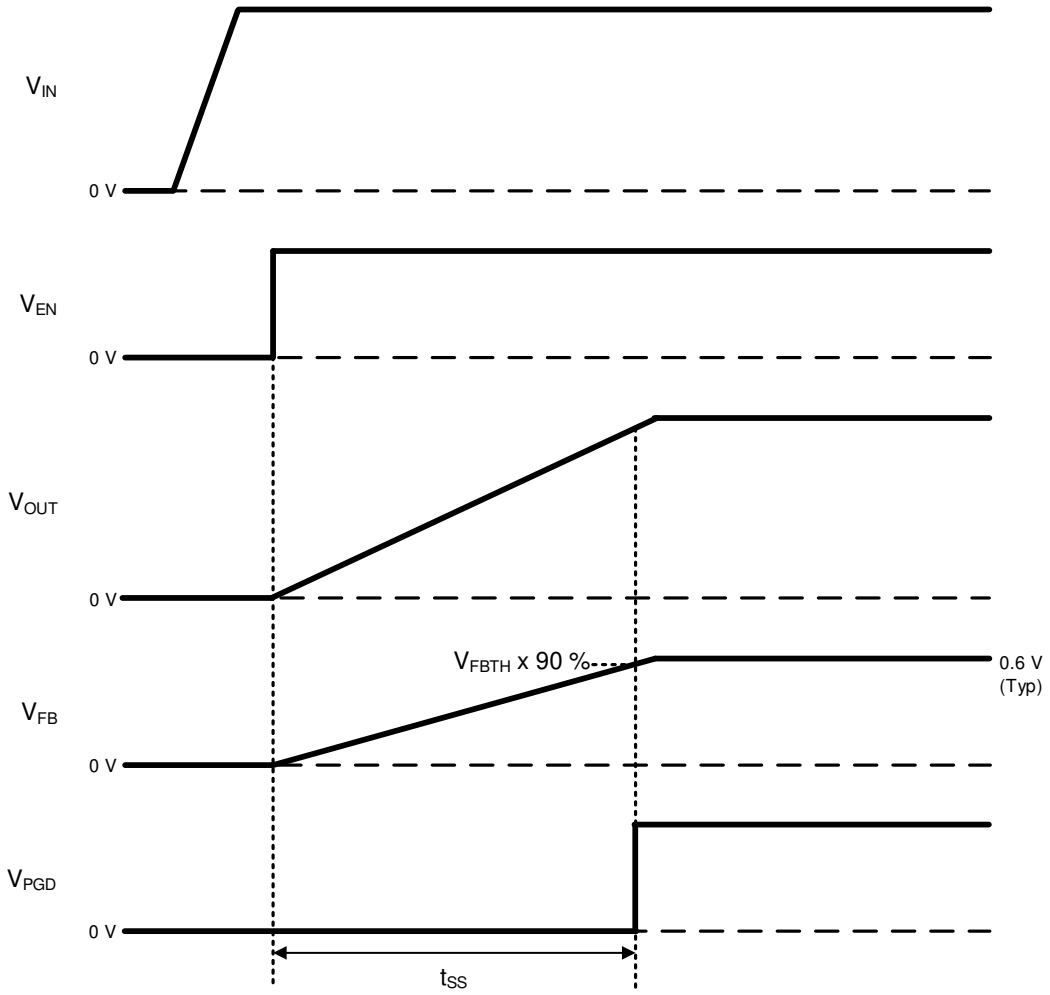


Figure 39. Soft Start Timing Chart

(4) Power Good Output

When the output voltage V_{OUT} reaches within ±10 % (Typ) of the voltage setting, the built-in open drain Nch MOSFET connected to the PGD pin is turned off, and the PGD pin goes Hi-Z (High impedance). When V_{OUT} reaches outside ±15 % (Typ) of the voltage setting, the open drain Nch MOSFET is turned on and PGD pin is pulled down with 100 Ω (Typ). It is recommended to connect a pull-up resistor of 10 kΩ to 100 kΩ.

Table 1. PGD Output

State	Condition	PGD Output
Before Supply Input Voltage	V_{IN} < 0.7 V (Typ)	Hi-Z
Shutdown	V_{EN} ≤ 0.875 V (Typ)	Low (Pull-down)
Enable V_{EN} ≥ 0.920 V (Typ)	90 % (Typ) ≤ V_{FB} / V_{FBTH} ≤ 110 % (Typ)	Hi-Z
	V_{FB} / V_{FBTH} ≤ 85 % (Typ) or 115 % (Typ) ≤ V_{FB} / V_{FBTH}	Low (Pull-down)
UVLO	0.7 V (Typ) < V_{IN} ≤ 2.45 V (Typ)	Low (Pull-down)
TSD	Tj ≥ 175 °C (Typ)	Low (Pull-down)
SCP	Complete Soft Start V_{FB} / V_{FBTH} ≤ 85 % (Typ) OCP 256 counts	Low (Pull-down)

Function Explanations – continued

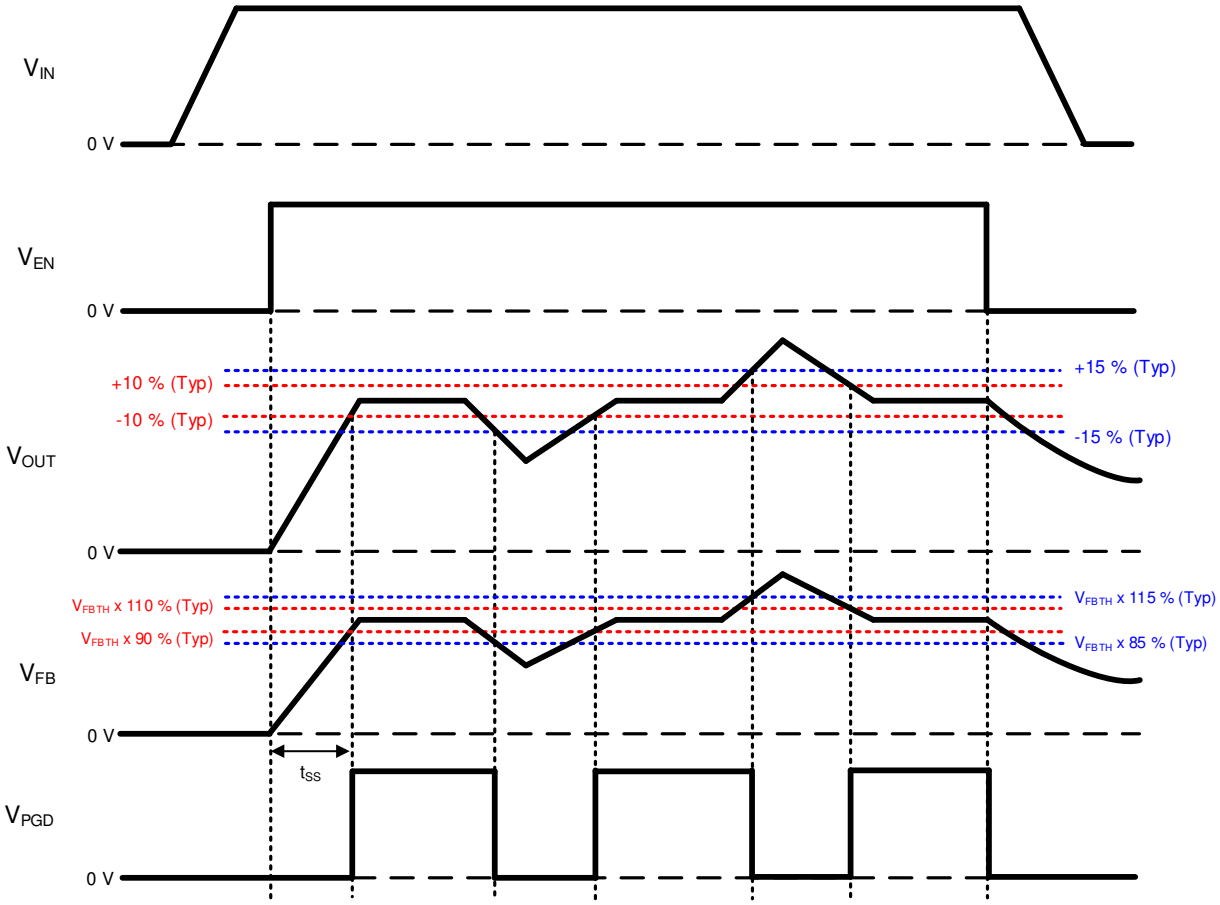


Figure 40. Power Good Timing Chart
(Connecting a pull-up resistor to the PGD pin)

(5) Output Capacitor Discharge Function

When even one of the following conditions is satisfied, output is discharged with 100 Ω (Typ) resistor through the SW pin.

- Shutdown: $V_{EN} \leq 0.875$ V (Typ)
- UVLO: $V_{IN} \leq 2.45$ V (Typ)
- TSD: Tj ≥ 175 °C (Typ)
- SCP: Complete Soft Start, $V_{FB} / V_{FBTH} \leq 85$ % (Typ), and OCP 256 counts

When all of the above conditions are released, output discharge is stopped.

Function Explanations – continued

2. Protection

The protection circuits are intended for prevention of damage caused by unexpected accidents. Do not use the continuous protection.

(1) Over Current Protection (OCP) / Short Circuit Protection (SCP)

Over Current Protection (OCP) restricts the flowing current through the Low-Side FET and the High-Side FET for every switching period. If the inductor current exceeds the Low-Side OCP I_{LOCP} = 4.5 A (Typ) while the Low-Side FET is on, the Low-Side FET remains on even with FB voltage V_{FB} falls to V_{FBTH} = 0.6 V (Typ) or lower. If the inductor current becomes lower than I_{LOCP}, the High-Side FET is able to be turned on. When the inductor current becomes the High-Side OCP I_{HOCP} = 6.5 A (Typ) or more while the High-Side FET is on, the High-Side FET is turned off. Output voltage may decrease by changing frequency and duty due to the OCP operation.

Short Circuit Protection (SCP) function is a Hiccup mode. When Low-Side OCP operates 256 cycles while V_{FB} is V_{FBTH} x 85 % or less (V_{PGD} = Low), the device stops the switching operation for 128 ms (Typ). After the 128 ms (Typ), the device restarts. SCP does not operate during the soft start even if the device is in the SCP conditions. Do not exceed the maximum junction temperature (Tjmax = 150 °C) during OCP and SCP operation.

Table 2. The Operating Condition of OCP and SCP

V_{EN}	V_{FB}	Start-up	OCP	SCP
≥ 0.920 V (Typ)	≤ V_{FBTH} x 85 % (Typ)	During Soft Start	Enable	Disable
	> V_{FBTH} x 85 % (Typ)	Complete Soft Start	Enable	Disable
	≤ V_{FBTH} x 85 % (Typ)		Enable	Enable
≤ 0.875 V (Typ)	-	Shutdown	Disable	Disable

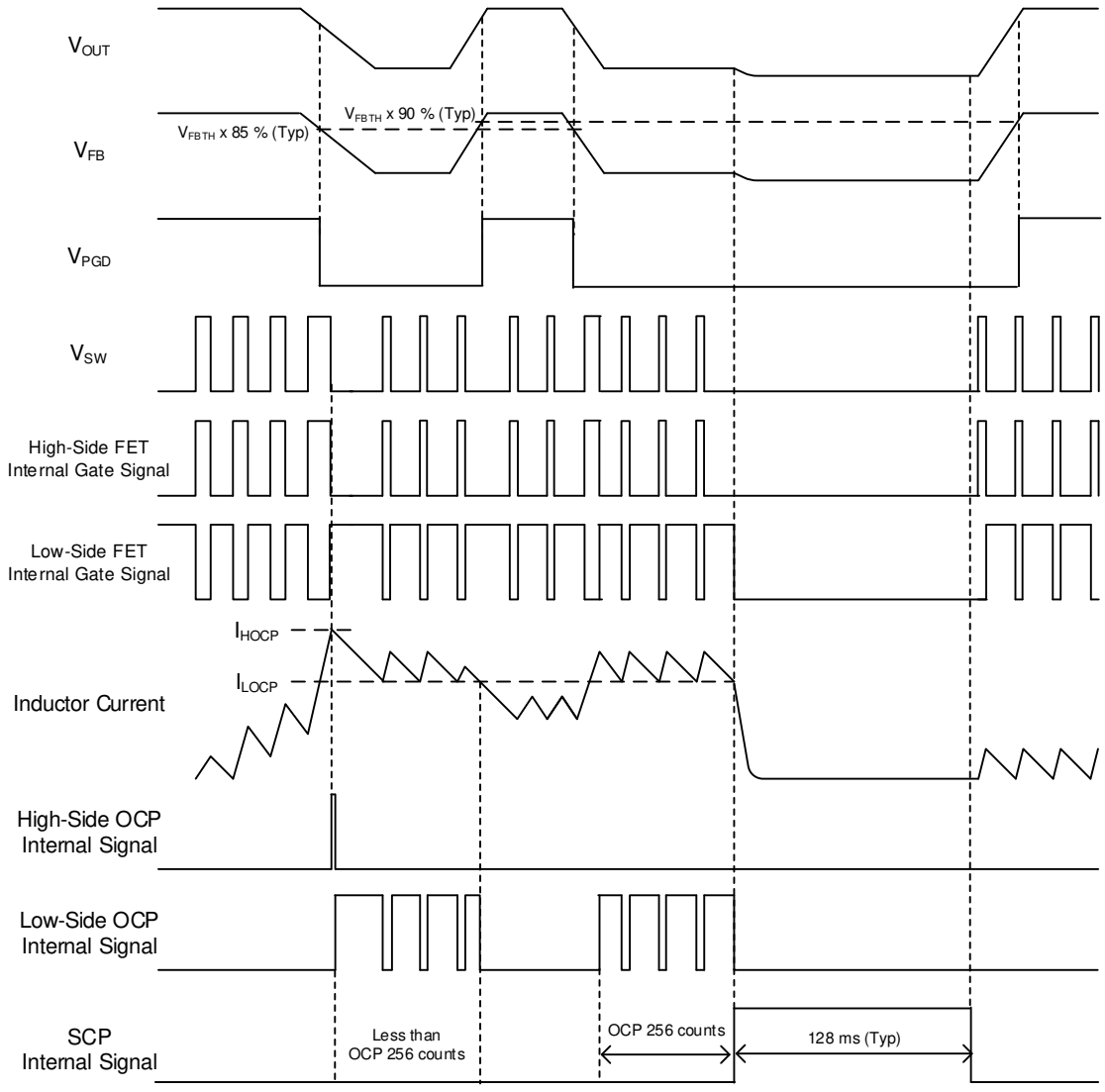


Figure 41. OCP and SCP Timing Chart

Function Explanations – continued

(2) Under Voltage Lockout Protection (UVLO)

When input voltage V_{IN} falls to 2.45 V (Typ) or lower, the device is shut down. When V_{IN} becomes 2.55 V (Typ) or more, the device starts up. The hysteresis is 100 mV (Typ).

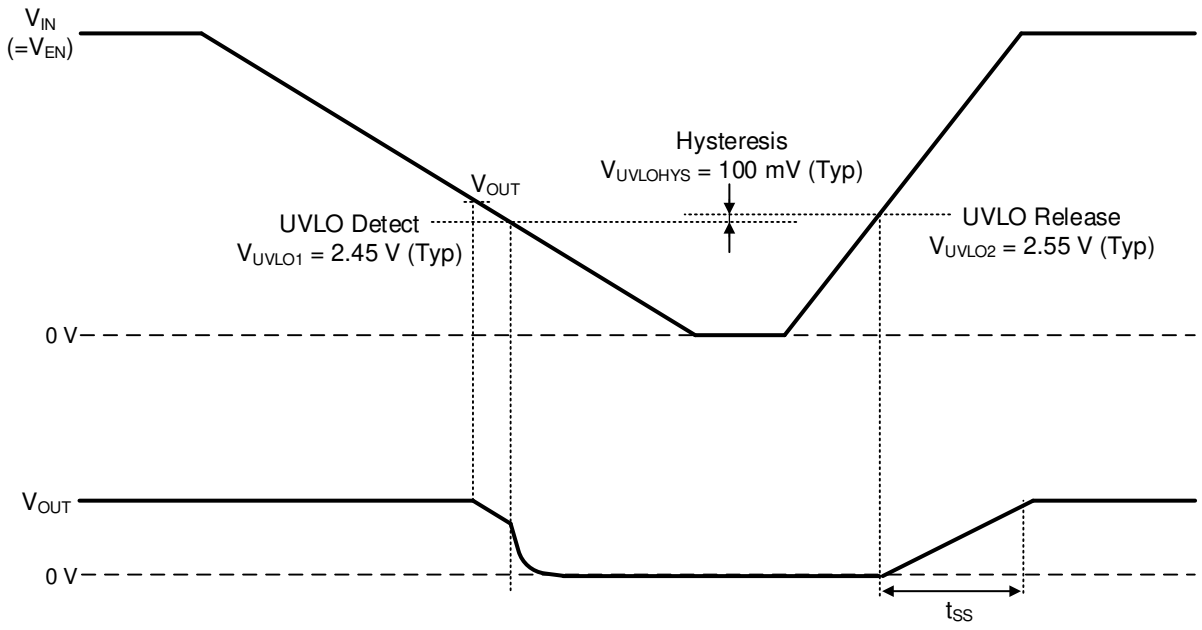


Figure 42. UVLO Timing Chart

(3) Thermal Shutdown Protection (TSD)

Thermal shutdown circuit prevents heat damage to the IC. The device should always operate within the IC's maximum junction temperature rating (Tjmax = 150 °C). However, if it continues exceeding the rating and the junction temperature Tj rises to 175 °C (Typ), the TSD circuit is activated and it turns the output MOSFETs off. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation. The TSD threshold has a hysteresis of 25 °C (Typ). Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings. Therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

(4) Over Voltage Protection (OVP)

When the FB voltage V_{FB} exceeds V_{FBTH} x 115 % (Typ) or more, the output MOSFETs are turned off to prevent the increase in the output voltage. After the V_{FB} falls V_{FBTH} x 110 % (Typ) or less, the output MOSFETs are returned to normal operation condition. Switching operation will restart after V_{FB} falls below V_{FBTH}.

Application Examples

1. V_{IN} = 5 V, V_{OUT} = 3.3 V

Table 3. Specification of Application (V_{IN} = 5 V, V_{OUT} = 3.3 V)

Parameter	Symbol	Specification Value
Input Voltage	V_{IN}	5 V (Typ)
Output Voltage	V_{OUT}	3.3 V (Typ)
Maximum Output Current	I_{OUTMAX}	3.0 A
Switching Frequency	f_{SW}	1.0 MHz (Typ)
Soft Start Time	t_{SS}	1 ms (Typ)
Temperature	Ta	25 °C

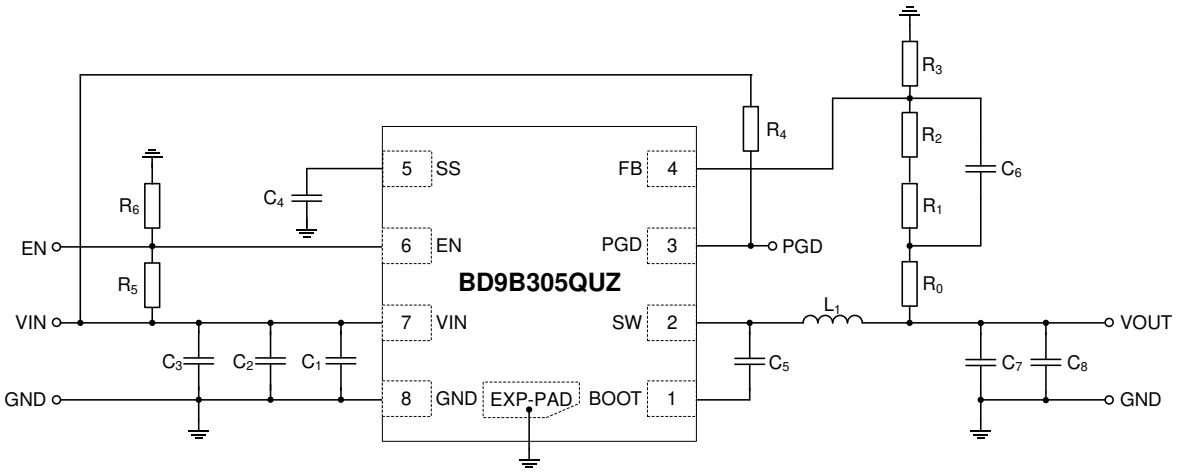


Figure 43. Application Circuit

Table 4. Recommended Component Values (V_{IN} = 5 V, V_{OUT} = 3.3 V)

Part No.	Value	Part Name	Size Code (mm)	Manufacturer
L_1	1.5 µH	FDSD0518-H-1R5M	5249	Murata
C_1 *(Note 1)*	0.1 µF (16V, X5R, ±10 %)	GRM033R61C104KE14	0603	Murata
C_2 *(Note 2)*	22 µF (10V, X5R, ±20 %)	GRM188R61A226ME15	1608	Murata
C_3 *(Note 2)*	-	-	-	-
C_4	-	-	-	-
C_5 *(Note 3)*	0.1 µF (16V, X5R, ±10 %)	GRM033R61C104KE14	0603	Murata
C_6	100 pF (50 V, C0G, ±5 %)	GRM0335C1H101JA01	0603	Murata
C_7 *(Note 4)*	22 µF (10V, X5R, ±20 %)	GRM188R61A226ME15	1608	Murata
C_8 *(Note 4)*	22 µF (10V, X5R, ±20 %)	GRM188R61A226ME15	1608	Murata
R_1	200 kΩ (1 %, 1/16 W)	MCR01MZPF2003	1005	ROHM
R_2	12 kΩ (1 %, 1/16 W)	MCR01MZPF1202	1005	ROHM
R_3	47 kΩ (1 %, 1/16 W)	MCR01MZPF4702	1005	ROHM
R_4	100 kΩ (1 %, 1/16 W)	MCR01MZPF1003	1005	ROHM
R_5	1.8 MΩ (1 %, 1/16 W)	MCR01MZPF1804	1005	ROHM
R_6	470 kΩ (1 %, 1/16 W)	MCR01MZPF4703	1005	ROHM
R_0 *(Note 5)*	Short	-	-	-

(Note 1) In order to reduce the influence of high frequency noise, connect a 0.1 µF ceramic capacitor C_1 as close as possible to the VIN pin and the GND pin if needed.

(Note 2) For the input capacitor C_2 and C_3, take temperature characteristics, DC bias characteristics, etc. into consideration to set to the actual capacitance of no less than 4.7 µF.

(Note 3) For the bootstrap capacitor C_5, take temperature characteristics, DC bias characteristics, etc. into consideration to set to the actual capacitance of no less than 0.022 µF.

(Note 4) In case of changing the actual capacitance value due to temperature characteristics, DC bias characteristics, etc. of the output capacitor C_7 and C_8, the loop response characteristics may change. Confirm with the actual application. The total capacitance of 10 µF to 47 x 2 µF is recommended for the output capacitor.

(Note 5) R_0 is an option, used for feedback's frequency response measurement. By inserting a resistor at R_0, it is possible to measure the frequency response (phase margin) using a FRA. However, the resistor will not be used in actual application, use this resistor pattern in short-circuit mode.

1. V_{IN} = 5 V, V_{OUT} = 3.3 V – continued

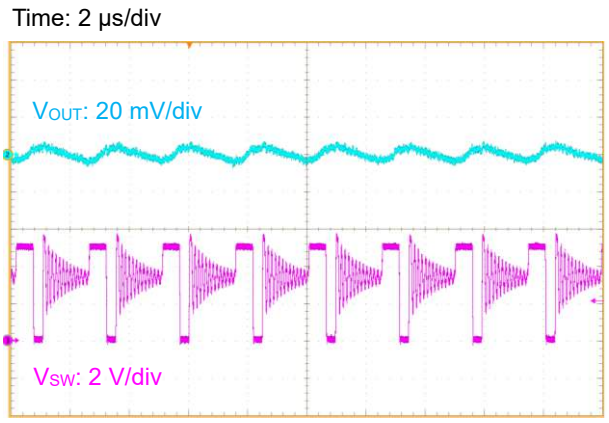


Figure 44. Output Ripple Voltage (I_{OUT} = 0.1 A)

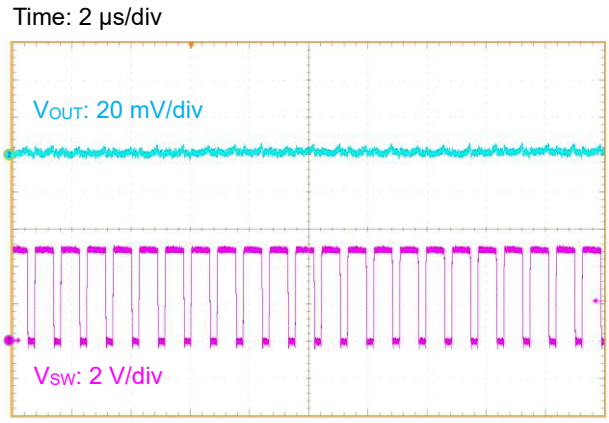


Figure 45. Output Ripple Voltage (I_{OUT} = 3.0 A)

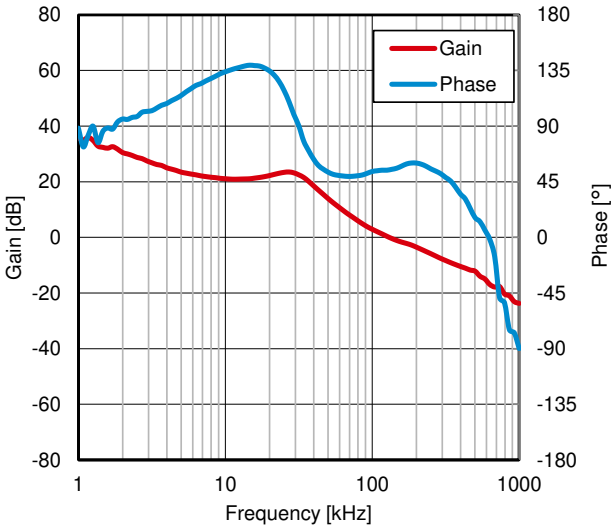


Figure 46. Frequency Characteristics (I_{OUT} = 3.0 A)

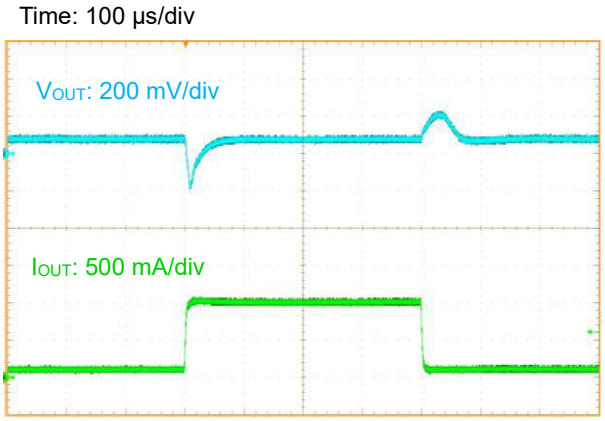


Figure 47. Load Transient Response (I_{OUT} = 0.1 A to 1.0 A)

Application Examples – continued

2. V_{IN} = 5 V, V_{OUT} = 1.8 V

Table 5. Specification of Application (V_{IN} = 5 V, V_{OUT} = 1.8 V)

Parameter	Symbol	Specification Value
Input Voltage	V_{IN}	5 V (Typ)
Output Voltage	V_{OUT}	1.8 V (Typ)
Maximum Output Current	I_{OUTMAX}	3.0 A
Switching Frequency	f_{SW}	1.0 MHz (Typ)
Soft Start Time	t_{SS}	1 ms (Typ)
Temperature	Ta	25 °C

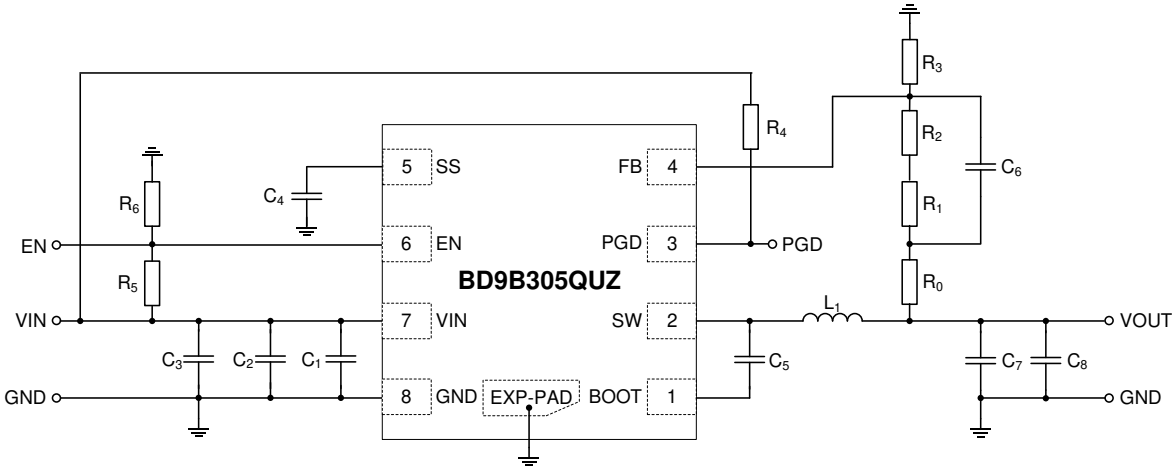


Figure 48. Application Circuit

Table 6. Recommended Component Values (V_{IN} = 5 V, V_{OUT} = 1.8 V)

Part No.	Value	Part Name	Size Code (mm)	Manufacturer
L_1	1.0 µH	FDSD0518-H-1R0M	5249	Murata
C_1 *(Note 1)*	0.1 µF (16V, X5R, ±10 %)	GRM033R61C104KE14	0603	Murata
C_2 *(Note 2)*	22 µF (10V, X5R, ±20 %)	GRM188R61A226ME15	1608	Murata
C_3 *(Note 2)*	-	-	-	-
C_4	-	-	-	-
C_5 *(Note 3)*	0.1 µF (16V, X5R, ±10 %)	GRM033R61C104KE14	0603	Murata
C_6	100 pF (50 V, C0G, ±5 %)	GRM0335C1H101JA01	0603	Murata
C_7 *(Note 4)*	47 µF (4 V, X5R, ±20 %)	AMK107BBJ476MA-RE	1608	TAIYO YUDEN
C_8 *(Note 4)*	-	-	-	-
R_1	200 kΩ (1 %, 1/16 W)	MCR01MZPF2003	1005	ROHM
R_2	Short	-	-	-
R_3	100 kΩ (1 %, 1/16 W)	MCR01MZPF1003	1005	ROHM
R_4	100 kΩ (1 %, 1/16 W)	MCR01MZPF1003	1005	ROHM
R_5	-	-	-	-
R_6	-	-	-	-
R_0 *(Note 5)*	Short	-	-	-

(Note 1) In order to reduce the influence of high frequency noise, connect a 0.1 µF ceramic capacitor C_1 as close as possible to the VIN pin and the GND pin if needed.

(Note 2) For the input capacitor C_2 and C_3, take temperature characteristics, DC bias characteristics, etc. into consideration to set to the actual capacitance of no less than 4.7 µF.

(Note 3) For the bootstrap capacitor C_5, take temperature characteristics, DC bias characteristics, etc. into consideration to set to the actual capacitance of no less than 0.022 µF.

(Note 4) In case of changing the actual capacitance value due to temperature characteristics, DC bias characteristics, etc. of the output capacitor C_7 and C_8, the loop response characteristics may change. Confirm with the actual application. The total capacitance of 10 µF to 47 x 2 µF is recommended for the output capacitor.

(Note 5) R_0 is an option, used for feedback's frequency response measurement. By inserting a resistor at R_0, it is possible to measure the frequency response (phase margin) using a FRA. However, the resistor will not be used in actual application, use this resistor pattern in short-circuit mode.

2. V_{IN} = 5 V, V_{OUT} = 1.8 V – continued

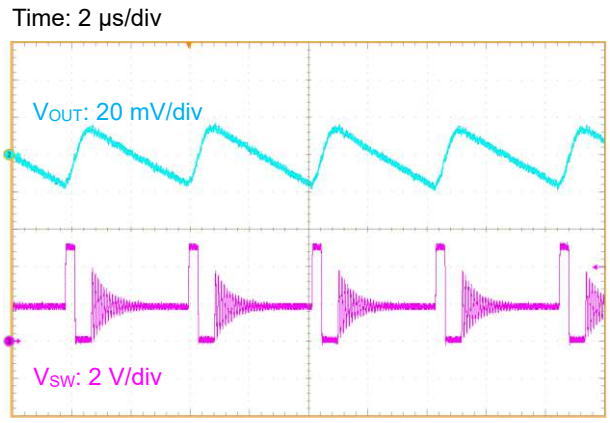


Figure 49. Output Ripple Voltage (I_{OUT} = 0.1 A)

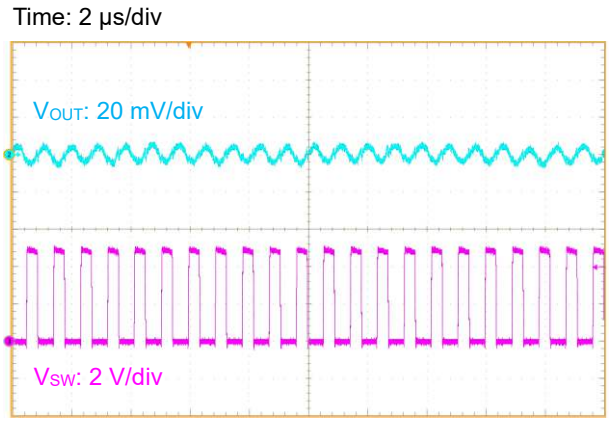


Figure 50. Output Ripple Voltage (I_{OUT} = 3.0 A)

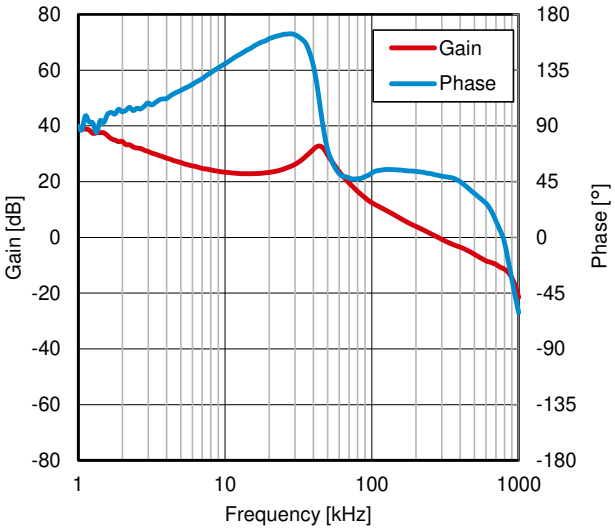


Figure 51. Frequency Characteristics (I_{OUT} = 3.0 A)

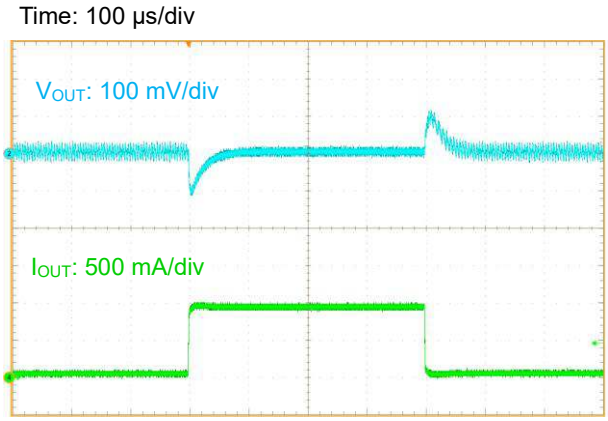


Figure 52. Load Transient Response (I_{OUT} = 0.1 A to 1.0 A)

Application Examples – continued

3. V_{IN} = 5 V, V_{OUT} = 1.2 V

Table 7. Specification of Application (V_{IN} = 5 V, V_{OUT} = 1.2 V)

Parameter	Symbol	Specification Value
Input Voltage	V_{IN}	5 V (Typ)
Output Voltage	V_{OUT}	1.2 V (Typ)
Maximum Output Current	I_{OUTMAX}	3.0 A
Switching Frequency	f_{SW}	1.0 MHz (Typ)
Soft Start Time	t_{SS}	1 ms (Typ)
Temperature	Ta	25 °C

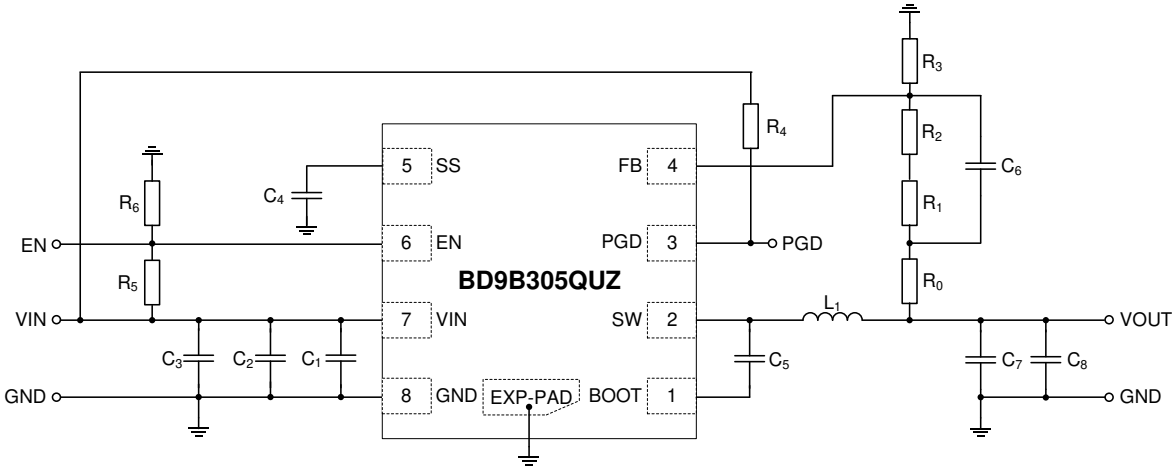


Figure 53. Application Circuit

Table 8. Recommended Component Values (V_{IN} = 5 V, V_{OUT} = 1.2 V)

Part No.	Value	Part Name	Size Code (mm)	Manufacturer
L_1	1.0 µH	FDSD0518-H-1R0M	5249	Murata
C_1 *(Note 1)*	0.1 µF (16V, X5R, ±10 %)	GRM033R61C104KE14	0603	Murata
C_2 *(Note 2)*	22 µF (10V, X5R, ±20 %)	GRM188R61A226ME15	1608	Murata
C_3 *(Note 2)*	-	-	-	-
C_4	-	-	-	-
C_5 *(Note 3)*	0.1 µF (16V, X5R, ±10 %)	GRM033R61C104KE14	0603	Murata
C_6	120 pF (50 V, C0G, ±5 %)	GRM0335C1H121JA01	0603	Murata
C_7 *(Note 4)*	47 µF (4 V, X5R, ±20 %)	AMK107BBJ476MA-RE	1608	TAIYO YUDEN
C_8 *(Note 4)*	-	-	-	-
R_1	150 kΩ (1 %, 1/16 W)	MCR01MZPF1503	1005	ROHM
R_2	Short	-	-	-
R_3	150 kΩ (1 %, 1/16 W)	MCR01MZPF1503	1005	ROHM
R_4	100 kΩ (1 %, 1/16 W)	MCR01MZPF1003	1005	ROHM
R_5	-	-	-	-
R_6	-	-	-	-
R_0 *(Note 5)*	Short	-	-	-

(Note 1) In order to reduce the influence of high frequency noise, connect a 0.1 µF ceramic capacitor C_1 as close as possible to the VIN pin and the GND pin if needed.

(Note 2) For the input capacitor C_2 and C_3, take temperature characteristics, DC bias characteristics, etc. into consideration to set to the actual capacitance of no less than 4.7 µF.

(Note 3) For the bootstrap capacitor C_5, take temperature characteristics, DC bias characteristics, etc. into consideration to set to the actual capacitance of no less than 0.022 µF.

(Note 4) In case of changing the actual capacitance value due to temperature characteristics, DC bias characteristics, etc. of the output capacitor C_7 and C_8, the loop response characteristics may change. Confirm with the actual application. The total capacitance of 10 µF to 47 x 2 µF is recommended for the output capacitor.

(Note 5) R_0 is an option, used for feedback's frequency response measurement. By inserting a resistor at R_0, it is possible to measure the frequency response (phase margin) using a FRA. However, the resistor will not be used in actual application, use this resistor pattern in short-circuit mode.

3. V_{IN} = 5 V, V_{OUT} = 1.2 V – continued

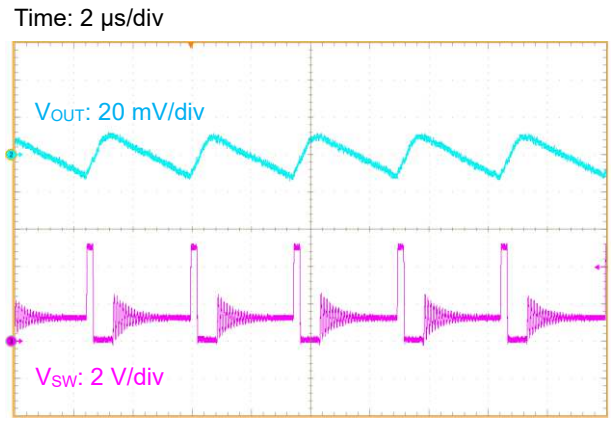


Figure 54. Output Ripple Voltage (I_{OUT} = 0.1 A)

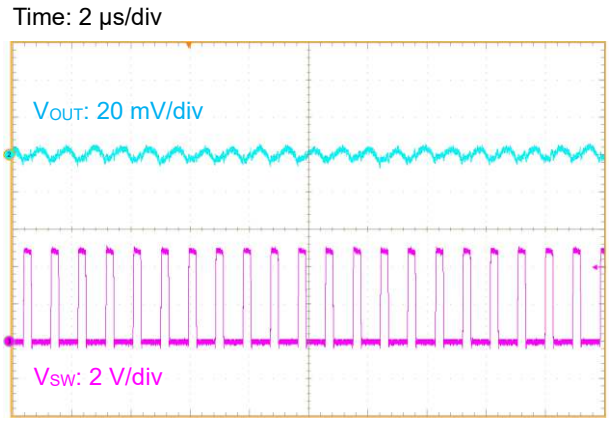


Figure 55. Output Ripple Voltage (I_{OUT} = 3.0 A)

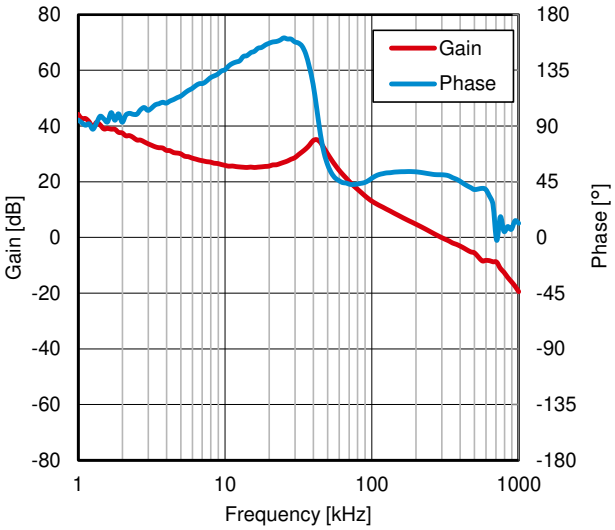


Figure 56. Frequency Characteristics (I_{OUT} = 3.0 A)

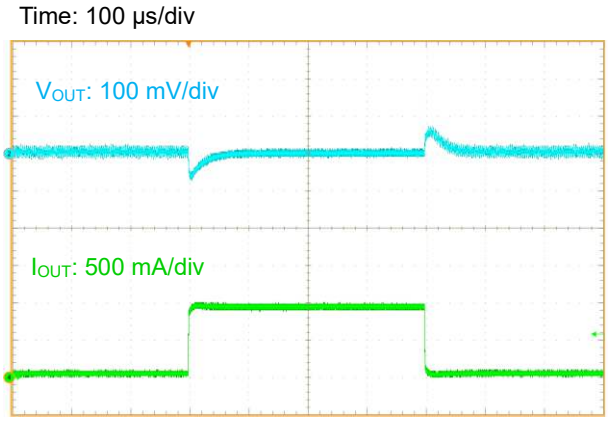


Figure 57. Load Transient Response (I_{OUT} = 0.1 A to 1.0 A)

Application Examples – continued

4. V_{IN} = 5 V, V_{OUT} = 1.0 V

Table 9. Specification of Application (V_{IN} = 5 V, V_{OUT} = 1.0 V)

Parameter	Symbol	Specification Value
Input Voltage	V_{IN}	5 V (Typ)
Output Voltage	V_{OUT}	1.0 V (Typ)
Maximum Output Current	I_{OUTMAX}	3.0 A
Switching Frequency	f_{SW}	1.0 MHz (Typ)
Soft Start Time	t_{SS}	1 ms (Typ)
Temperature	Ta	25 °C

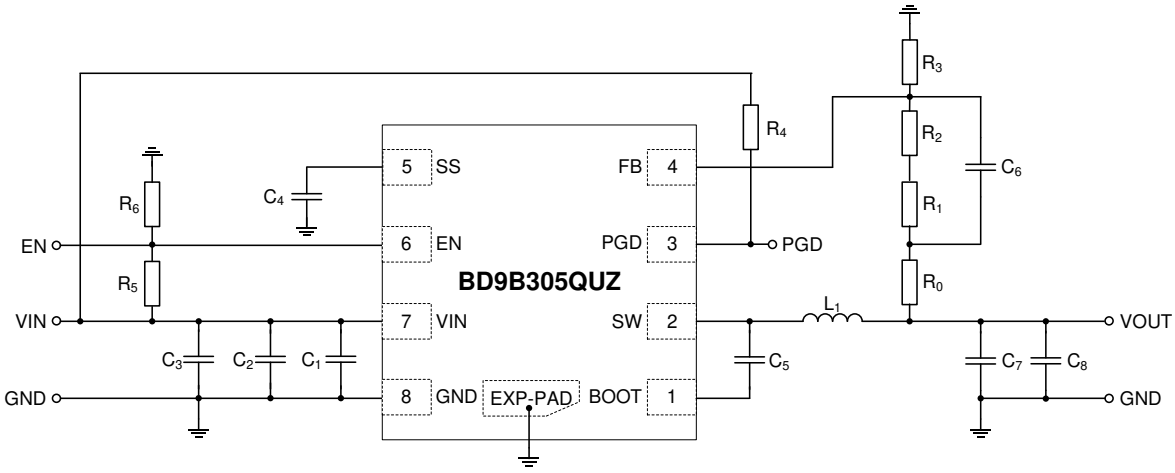


Figure 58. Application Circuit

Table 10. Recommended Component Values (V_{IN} = 5 V, V_{OUT} = 1.0 V)

Part No.	Value	Part Name	Size Code (mm)	Manufacturer
L_1	1.0 µH	FDSD0518-H-1R0M	5249	Murata
C_1 *(Note 1)*	0.1 µF (16V, X5R, ±10 %)	GRM033R61C104KE14	0603	Murata
C_2 *(Note 2)*	22 µF (10V, X5R, ±20 %)	GRM188R61A226ME15	1608	Murata
C_3 *(Note 2)*	-	-	-	-
C_4	-	-	-	-
C_5 *(Note 3)*	0.1 µF (16V, X5R, ±10 %)	GRM033R61C104KE14	0603	Murata
C_6	120 pF (50 V, C0G, ±5 %)	GRM0335C1H121JA01	0603	Murata
C_7 *(Note 4)*	47 µF (4 V, X5R, ±20 %)	AMK107BBJ476MA-RE	1608	TAIYO YUDEN
C_8 *(Note 4)*	-	-	-	-
R_1	100 kΩ (1 %, 1/16 W)	MCR01MZPF1003	1005	ROHM
R_2	Short	-	-	-
R_3	150 kΩ (1 %, 1/16 W)	MCR01MZPF1503	1005	ROHM
R_4	100 kΩ (1 %, 1/16 W)	MCR01MZPF1003	1005	ROHM
R_5	-	-	-	-
R_6	-	-	-	-
R_0 *(Note 5)*	Short	-	-	-

(Note 1) In order to reduce the influence of high frequency noise, connect a 0.1 µF ceramic capacitor C_1 as close as possible to the VIN pin and the GND pin if needed.

(Note 2) For the input capacitor C_2 and C_3, take temperature characteristics, DC bias characteristics, etc. into consideration to set to the actual capacitance of no less than 4.7 µF.

(Note 3) For the bootstrap capacitor C_5, take temperature characteristics, DC bias characteristics, etc. into consideration to set to the actual capacitance of no less than 0.022 µF.

(Note 4) In case of changing the actual capacitance value due to temperature characteristics, DC bias characteristics, etc. of the output capacitor C_7 and C_8, the loop response characteristics may change. Confirm with the actual application. The total capacitance of 10 µF to 47 x 2 µF is recommended for the output capacitor.

(Note 5) R_0 is an option, used for feedback's frequency response measurement. By inserting a resistor at R_0, it is possible to measure the frequency response (phase margin) using a FRA. However, the resistor will not be used in actual application, use this resistor pattern in short-circuit mode.

4. V_{IN} = 5 V, V_{OUT} = 1.0 V – continued

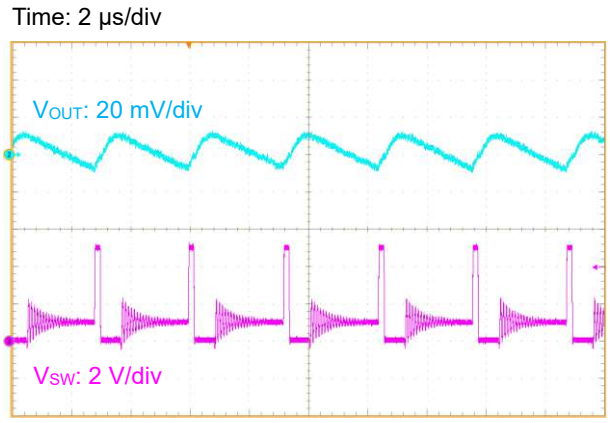


Figure 59. Output Ripple Voltage (I_{OUT} = 0.1 A)

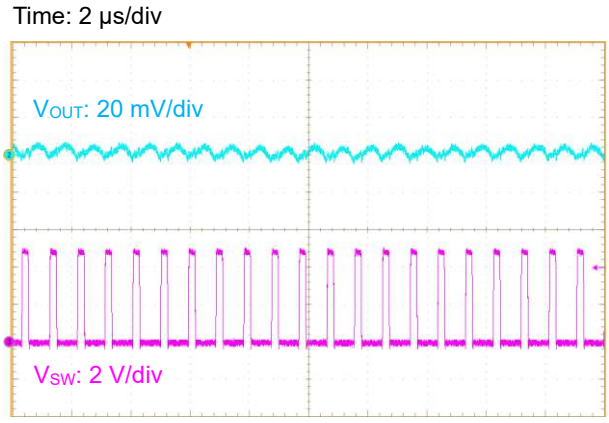


Figure 60. Output Ripple Voltage (I_{OUT} = 3.0 A)

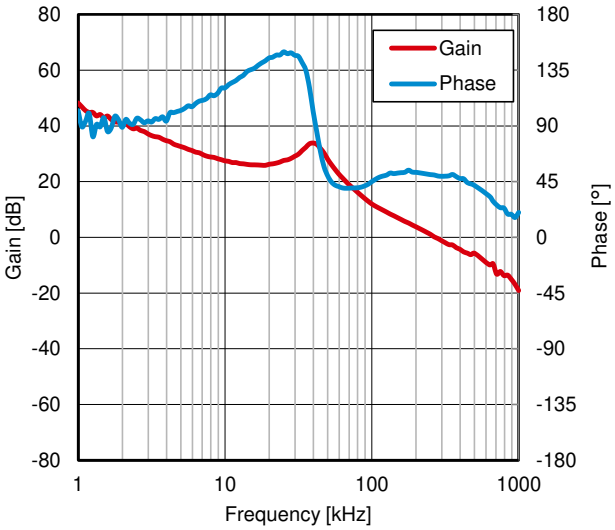


Figure 61. Frequency Characteristics (I_{OUT} = 3.0 A)

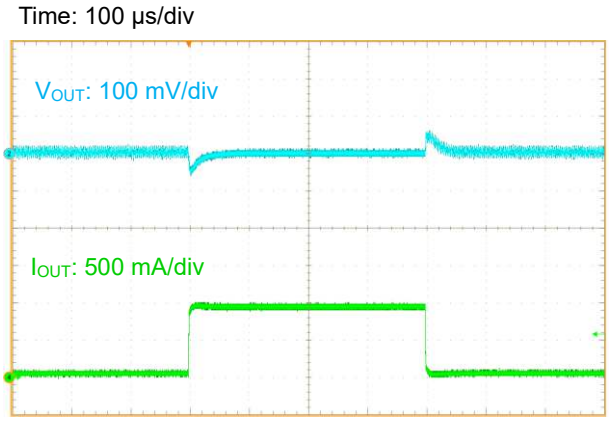


Figure 62. Load Transient Response (I_{OUT} = 0.1 A to 1.0 A)

Application Examples – continued

5. V_{IN} = 5 V, V_{OUT} = 0.6 V

Table 11. Specification of Application (V_{IN} = 5 V, V_{OUT} = 0.6 V)

Parameter	Symbol	Specification Value
Input Voltage	V_{IN}	5 V (Typ)
Output Voltage	V_{OUT}	0.6 V (Typ)
Maximum Output Current	I_{OUTMAX}	3.0 A
Switching Frequency	f_{SW}	1.0 MHz (Typ)
Soft Start Time	t_{SS}	1 ms (Typ)
Temperature	Ta	25 °C

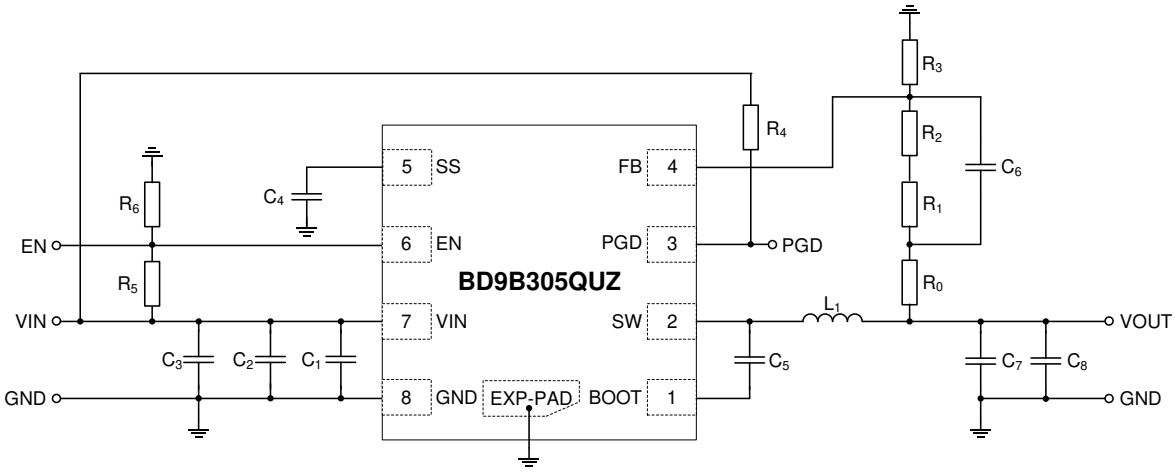


Figure 63. Application Circuit

Table 12. Recommended Component Values (V_{IN} = 5 V, V_{OUT} = 0.6 V)

Part No.	Value	Part Name	Size Code (mm)	Manufacturer
L_1	1.0 µH	FDSD0518-H-1R0M	5249	Murata
C_1 *(Note 1)*	0.1 µF (16V, X5R, ±10 %)	GRM033R61C104KE14	0603	Murata
C_2 *(Note 2)*	22 µF (10V, X5R, ±20 %)	GRM188R61A226ME15	1608	Murata
C_3 *(Note 2)*	-	-	-	-
C_4	-	-	-	-
C_5 *(Note 3)*	0.1 µF (16V, X5R, ±10 %)	GRM033R61C104KE14	0603	Murata
C_6	120 pF (50 V, C0G, ±5 %)	GRM0335C1H121JA01	0603	Murata
C_7 *(Note 4)*	47 µF (4 V, X5R, ±20 %)	AMK107BBJ476MA-RE	1608	TAIYO YUDEN
C_8 *(Note 4)*	-	-	-	-
R_1	100 kΩ (1 %, 1/16 W)	MCR01MZPF1003	1005	ROHM
R_2	Short	-	-	-
R_3	-	-	-	-
R_4	100 kΩ (1 %, 1/16 W)	MCR01MZPF1003	1005	ROHM
R_5	-	-	-	-
R_6	-	-	-	-
R_0 *(Note 5)*	Short	-	-	-

(Note 1) In order to reduce the influence of high frequency noise, connect a 0.1 µF ceramic capacitor C_1 as close as possible to the VIN pin and the GND pin if needed.

(Note 2) For the input capacitor C_2 and C_3, take temperature characteristics, DC bias characteristics, etc. into consideration to set to the actual capacitance of no less than 4.7 µF.

(Note 3) For the bootstrap capacitor C_5, take temperature characteristics, DC bias characteristics, etc. into consideration to set to the actual capacitance of no less than 0.022 µF.

(Note 4) In case of changing the actual capacitance value due to temperature characteristics, DC bias characteristics, etc. of the output capacitor C_7 and C_8, the loop response characteristics may change. Confirm with the actual application. The total capacitance of 10 µF to 47 x 2 µF is recommended for the output capacitor.

(Note 5) R_0 is an option, used for feedback's frequency response measurement. By inserting a resistor at R_0, it is possible to measure the frequency response (phase margin) using a FRA. However, the resistor will not be used in actual application, use this resistor pattern in short-circuit mode.

5. V_{IN} = 5 V, V_{OUT} = 0.6 V – continued

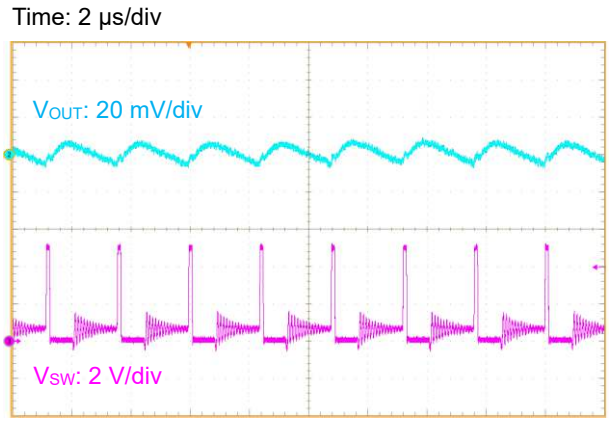


Figure 64. Output Ripple Voltage (I_{OUT} = 0.1 A)

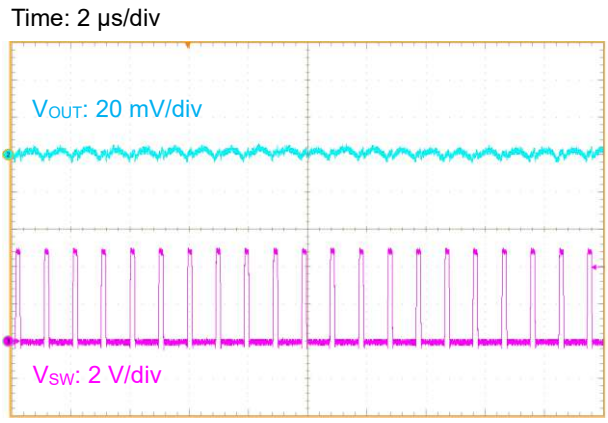


Figure 65. Output Ripple Voltage (I_{OUT} = 3.0 A)

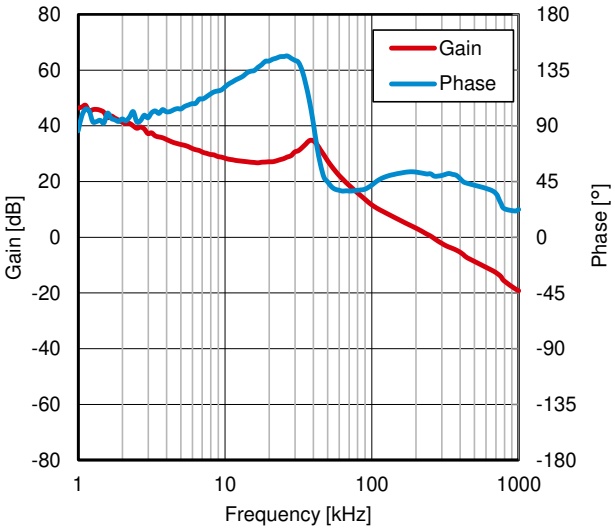


Figure 66. Frequency Characteristics (I_{OUT} = 3.0 A)

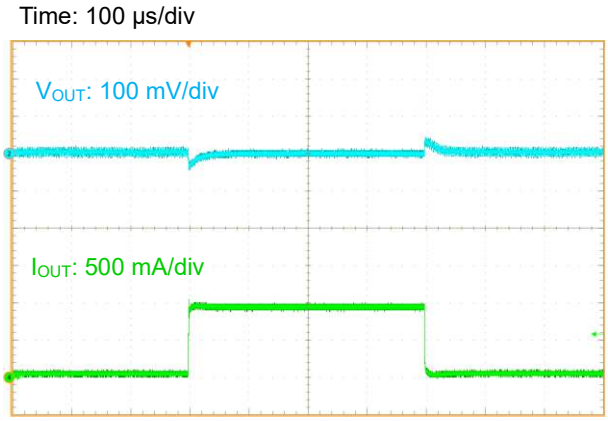


Figure 67. Load Transient Response (I_{OUT} = 0.1 A to 1.0 A)

Selection of Components Externally Connected

Contact us if not use the recommended component values in Application Examples.

1. Input Capacitor

Use ceramic type capacitor for the input capacitor. The input capacitor is used to reduce the input ripple noise and it is effective by being placed as close as possible to the VIN pin. Set the capacitor value so that it does not fall to 4.7 µF considering the capacitor value variances, temperature characteristics, DC bias characteristics, aging characteristics, and etc. The PCB layout and the position of the capacitor may lead to IC malfunction. Refer to the notes on the PCB layout on page 34 to 35 when designing PCB layout. In addition, the capacitor with value 0.1 µF can be connected as close as possible to the VIN pin and the GND pin in order to reduce the high frequency noise.

2. Output Voltage Setting

The output voltage can be set by the feedback resistance ratio connected to the FB pin. For stable operation, the parallel resistance of feedback resistors R_1 and R_2 should be set to 20 kΩ or more.

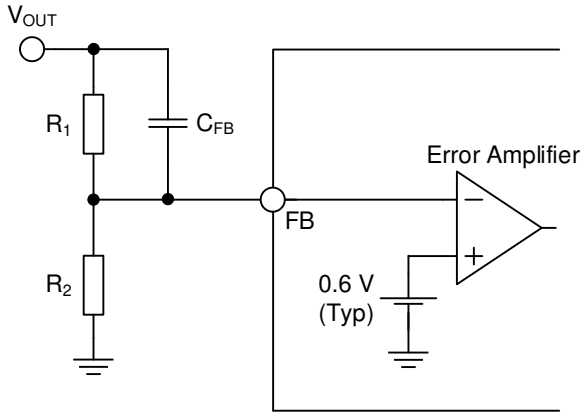


Figure 68. Feedback Resistor Circuit

The output voltage V_{OUT} can be calculated as below.

$$V_{OUT} = \frac{R_1+R_2}{R_2} \times 0.6 \text{ [V]}$$

$$0.6 \leq V_{OUT} \leq (V_{IN} \times 0.8) \text{ [V]}$$

$$1/(\frac{1}{R_1}+\frac{1}{R_2}) \geq 20 \text{ [kΩ]}$$

3. Soft Start Capacitor (Soft Start Time Setting)

The soft start time t_{SS} depends on the value of the capacitor connected to the SS pin. The t_{SS} is 1 ms (Typ) when the SS pin is left floating. The capacitor connected to the SS pin makes t_{SS} more than 1 ms. The t_{SS} and C_{SS} can be calculated using below equation. The C_{SS} should be set in the range between 3300 pF and 0.1 µF.

$$t_{SS} = \frac{C_{SS} \times 0.6}{I_{SS}} \text{ [s]}$$

where:
I_{SS} is the Soft Start Charge Current 1.0 µA (Typ).

With C_{SS} = 8200 pF, t_{SS} can be calculated as below.

$$t_{SS} = \frac{8200\ pF \times 0.6}{1.0\ \mu A} = 4.9 \text{ [ms]}$$

Selection of Components Externally Connected – continued

4. Output LC Filter

In order to supply a continuous current to the load, the DC/DC converter requires an LC filter for smoothing the output voltage. Use the inductor with value 1.0 µH to 1.5 µH.

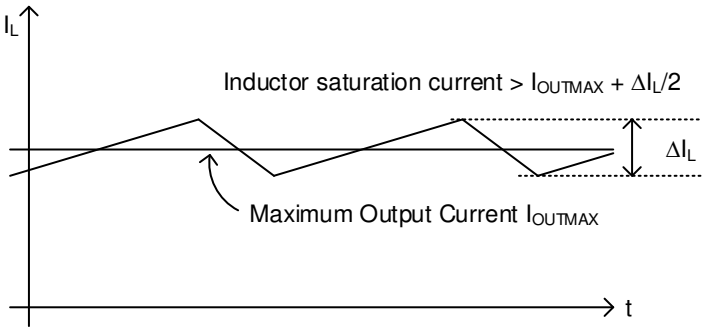


Figure 69. Waveform of Inductor Current

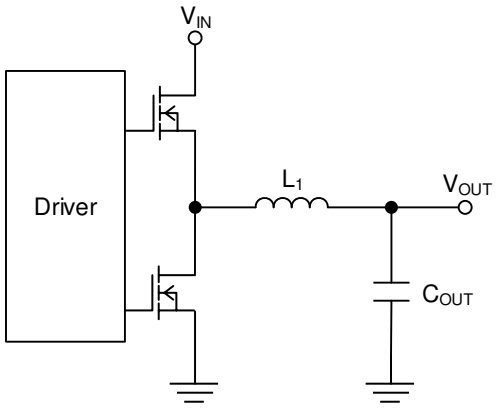


Figure 70. Output LC Filter Circuit

For example, given that V_{IN} = 5 V, V_{OUT} = 1.8 V, L_1 = 1.0 µH, and the switching frequency f_{SW} = 1.0 MHz, Inductor current ΔI_L can be represented by the following equation.

$$\Delta I_L = V_{OUT} \times (V_{IN} - V_{OUT}) \times \frac{1}{V_{IN} \times f_{SW} \times L_1} = 1.15 \text{ [A]}$$

The rated current of the inductor (Inductor saturation current) must be larger than the sum of the maximum output current I_{OUTMAX} and 1/2 of the inductor ripple current ΔI_L.

Use ceramic type capacitor for the output capacitor C_{OUT}. The capacitance value of C_{OUT} is recommended in the range between 10 µF and 47 x 2 µF. C_{OUT} affects the output ripple voltage. Select C_{OUT} so that it must satisfy the required ripple voltage characteristics.
The output ripple voltage can be estimated by the following equation.

$$\Delta V_{RPL} = \Delta I_L \times \left(R_{ESR} + \frac{1}{8 \times C_{OUT} \times f_{SW}} \right) \text{ [V]}$$

where:
R_{ESR} is the Equivalent Series Resistance (ESR) of the output capacitor.

For example, given that C_{OUT} = 47 µF and R_{ESR} = 3 mΩ, ΔV_{RPL} can be calculated as below.

$$\Delta V_{RPL} = 1.15\ A \times \left(3\ m\Omega + \frac{1}{8 \times 47\ \mu F \times 1\ MHz} \right) = 6.5 \text{ [mV]}$$

4. Output LC Filter – continued

In addition, the total capacitance connected to V_{OUT} needs to satisfy the value obtained by the following equation.

$$C_{OUTMAX} < \frac{t_{SSMIN}}{V_{OUT}} \times (3.1 + \frac{\Delta I_L}{2} - I_{OUTSS}) \text{ [F]}$$

where:
t_{SSMIN} is the minimum soft start time.
V_{OUT} is the output voltage.
ΔI_L is the inductor current.
I_{OUTSS} is the maximum output current during soft start.

For example, given that V_{IN} = 5 V, V_{OUT} = 1.8 V, L_1 = 1.0 µH, f_{SW} = 1 MHz (Typ), t_{SSMIN} = 0.6 ms (C_{SS} = OPEN), and I_{OUTSS} = 3 A, C_{OUTMAX} can be calculated as below.

$$C_{OUTMAX} < \frac{0.6\ ms}{1.8\ V} \times (3.1 + \frac{1.15\ A}{2} - 3\ A) = 225 \text{ [µF]}$$

If the total capacitance connected to V_{OUT} is larger than C_{OUTMAX}, over current protection may be activated by the inrush current at startup and prevented to turn on the output. Confirm this on the actual application.

5. FB Capacitor

The Constant On-time Control required the sufficient ripple voltage on FB voltage for the operation stability. This device is designed to correspond to low ESR output capacitors by injecting the ripple voltage to FB voltage inside the IC. The FB capacitor C_{FB} (Figure 68) should be set within the range of the following expression in order to inject an appropriate ripple.

$$\frac{V_{OUT} \times (1 - V_{OUT}/V_{IN})}{f_{SW} \times 21 \times 10^3} < C_{FB} < \frac{V_{OUT} \times (1 - V_{OUT}/V_{IN})}{f_{SW} \times 3.3 \times 10^3} \text{ [F]}$$

where:
V_{IN} is the input voltage.
V_{OUT} is the output voltage.
f_{SW} is the switching frequency 1.0 MHz (Typ).

Load transient response and the loop stability depends on L_1, C_{OUT}, and C_{FB}. Actually, these characteristics may change depending on PCB layout, wiring, the type of components, and the conditions (temperature, etc.). Be sure to check them on the actual application.

6. Bootstrap Capacitor

The bootstrap capacitor 0.1µF is recommended. Connect the capacitor between the SW pin and the BOOT pin. For the capacitance, take temperature characteristics, DC bias characteristics, and etc. into consideration to set to the actual capacitance of no less than 0.022 µF.

PCB Layout Design

PCB layout design for DC/DC converter is very important. Appropriate layout can avoid various problems concerning power supply circuit. Figure 71-a to Figure 71-c show the current path in a buck DC/DC converter circuit. The Loop 1 in Figure 71-a is a current path when H-side switch is ON and L-side switch is OFF, the Loop 2 in Figure 71-b is when H-side switch is OFF and L-side switch is ON. The thick line in Figure 71-c shows the difference between Loop1 and Loop2. The current in thick line change sharply each time the switching element H-side and L-side switch change from OFF to ON, and vice versa. These sharp changes induce a waveform with harmonics in this loop. Therefore, the loop area of thick line that is consisted by input capacitor and IC should be as small as possible to minimize noise. For more details, refer to application note of switching regulator series “PCB Layout Techniques of Buck Converter”.

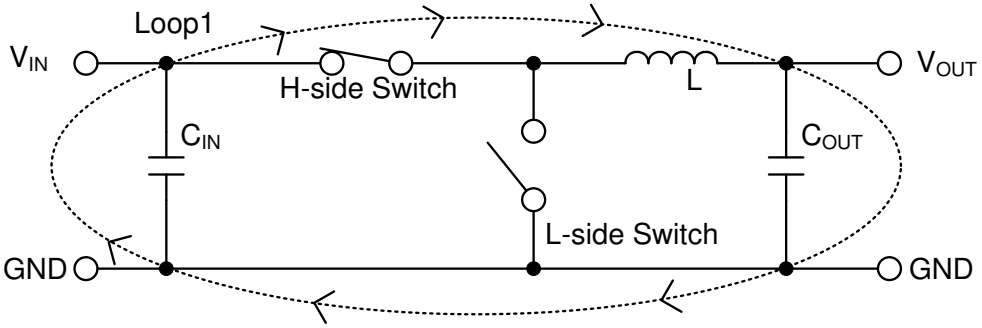


Figure 71-a. Current Path when H-side Switch = ON, L-side Switch = OFF

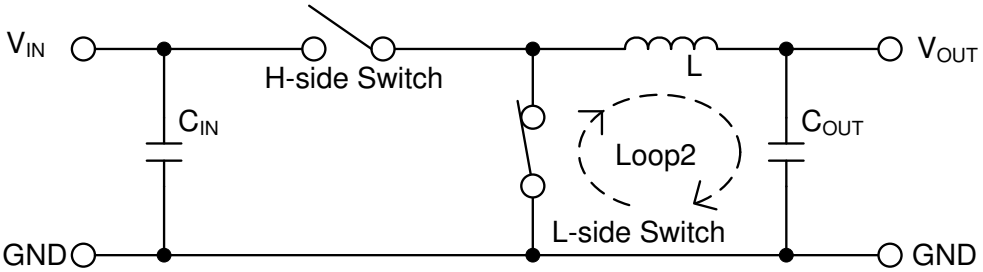


Figure 71-b. Current Path when H-side Switch = OFF, L-side Switch = ON

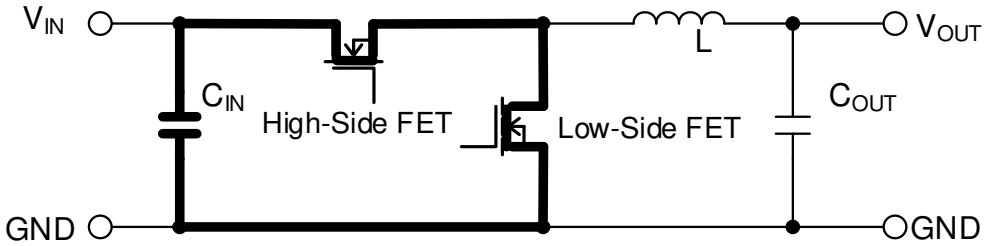


Figure 71-c. Difference of Current and Critical Area in Layout

PCB Layout Design – continued

When designing the PCB layout, pay attention to the following points:

- Connect the input capacitor C_{IN1} and C_{IN2} as close as possible to the VIN pin and GND pin on the same plane as the IC.
- Switching nodes such as SW are susceptible to noise due to AC coupling with other nodes. Route the inductor pattern L_1 as thick and as short as possible.
- Feedback line connected to the FB pin far from the SW nodes.
- Place the output capacitor C_{OUT} away from input capacitor C_{IN1} and C_{IN2} to avoid harmonics noise from the input.
- Separate the reference ground and the power ground and connect them through VIA. The reference ground should be connected to the power ground that is close to the output capacitor C_{OUT}. It is because C_{OUT} has less high frequency switching noise.
- R_0 is provided for the measurement of feedback frequency characteristics (optional). By inserting a resistor into R_0, it is possible to measure the frequency characteristics of feedback (phase margin) using FRA etc. R_0 is short-circuited for normal use.

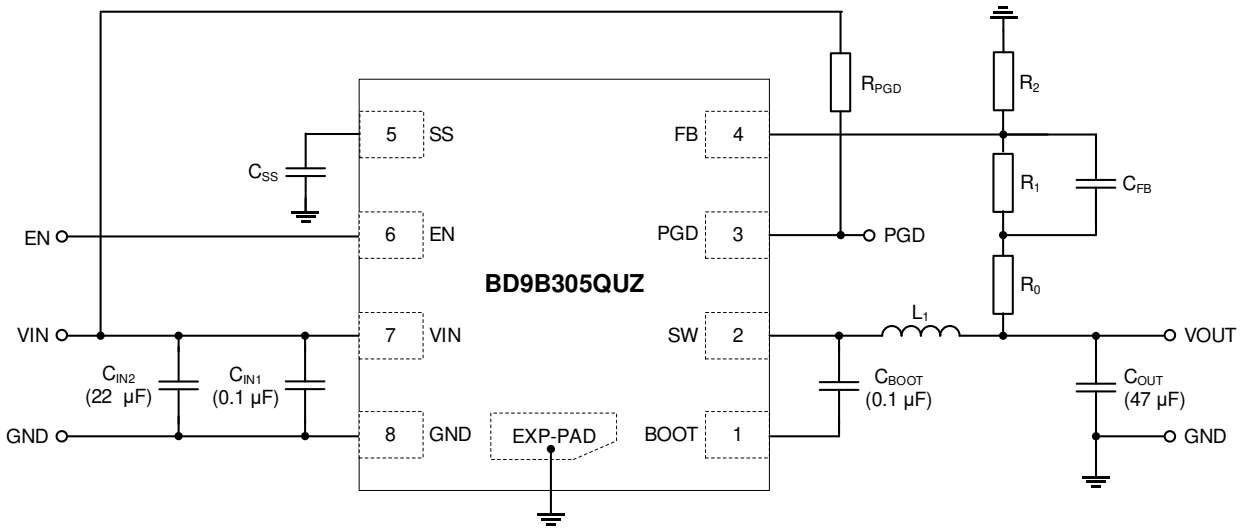


Figure 72. Application Circuit

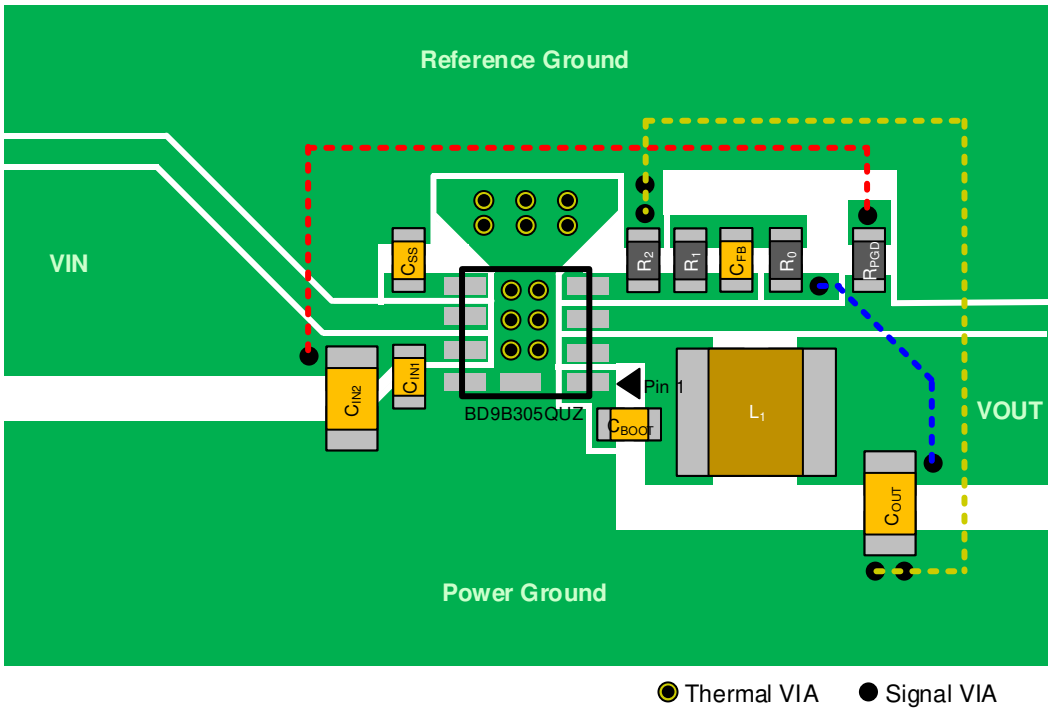
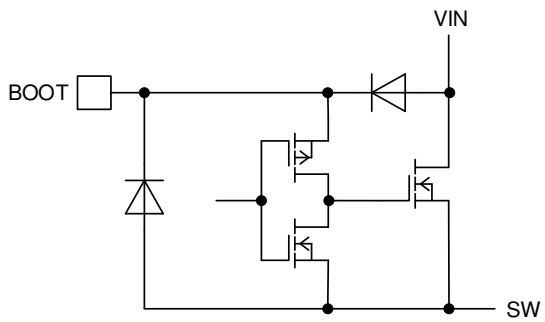
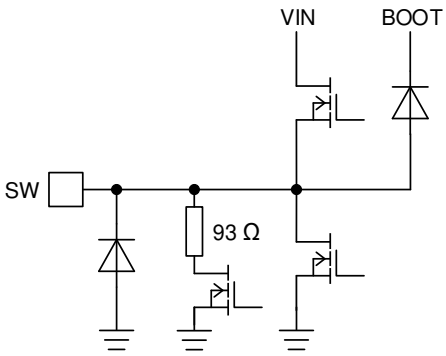
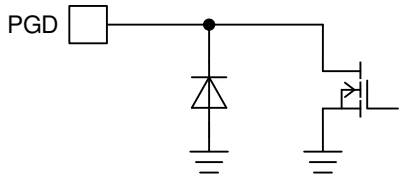
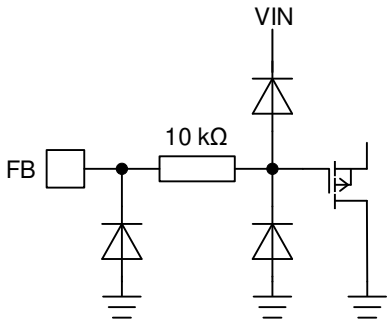
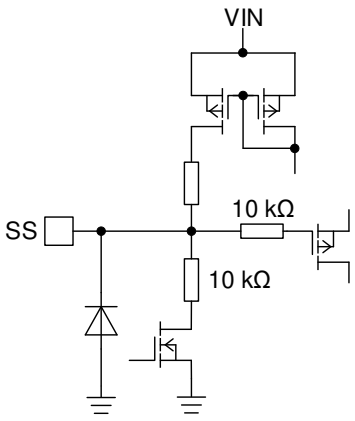
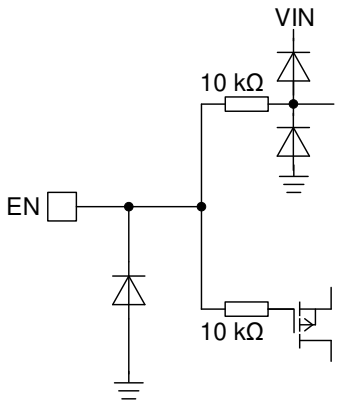


Figure 73. Example of PCB Layout

I/O Equivalence Circuits

1. BOOT	2. SW
	
3. PGD	**4. FB**
	
5. SS	**6. EN**
	

(Note) Resistor values are typical.

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition. However, pins that drive inductive loads (e.g. motor driver outputs, DC-DC converter outputs) may inevitably go below ground due to back EMF or electromotive force. In such cases, the user should make sure that such voltages going below ground will not cause the IC and the system to malfunction by examining carefully all relevant factors and conditions such as motor characteristics, supply voltage, operating frequency and PCB wiring to name a few.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Recommended Operating Conditions**
   The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. **Inter-pin Short and Mounting Errors**
   Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. **Unused Input Pins**
   Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

10. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

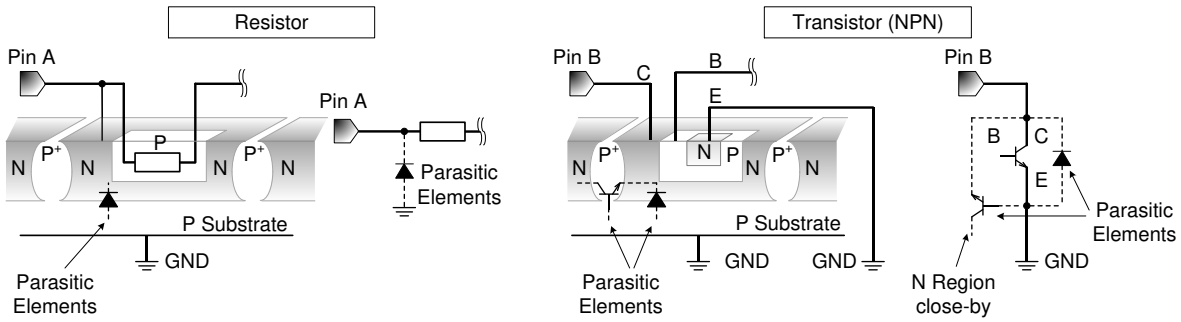


Figure 74. Example of Monolithic IC Structure

11. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

12. Thermal Shutdown Circuit (TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF power output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

13. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

Ordering Information

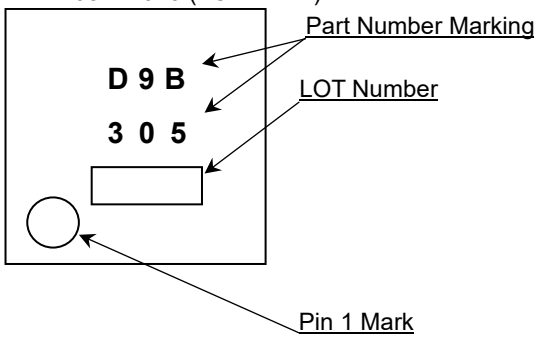
B	D	9	B	3	0	5	Q	U	Z	-	E 2

Package
VMMP08LZ2020

Packaging and forming specification
E2: Embossed tape and reel

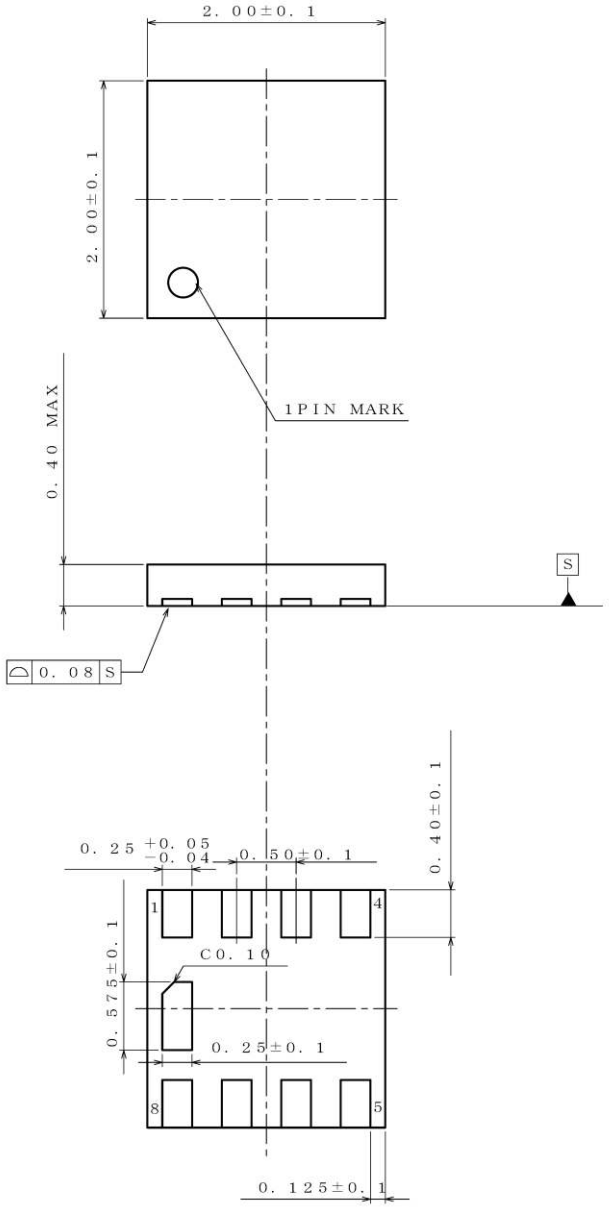
Marking Diagram

VMMP08LZ2020 (TOP VIEW)



Physical Dimension and Packing Information

Package Name	VMMP08LZ2020

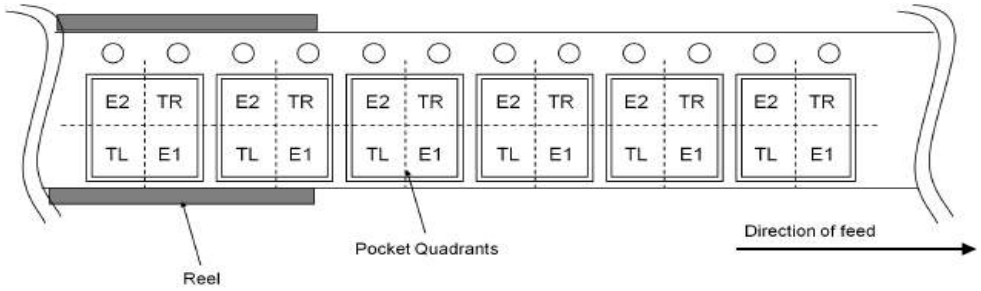


(UNIT:mm)

PKG:VMMP08LZ2020
Drawing No.:EX767-5002-1

< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	4000pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



Revision History

Date	Revision	Changes
08.Mar.2019	001	New Release
20.Feb.2023	002	Change the recommended components C_6, C_7 and C_8 in Table 4. Update Figure 44, Figure 45, Figure 46 and Figure 47.

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1. Our Products are designed and manufactured for application in ordinary electronic equipment (such as AV equipment, OA equipment, telecommunication equipment, home electronic appliances, amusement equipment, etc.). If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), transport equipment, traffic equipment, aircraft/spacecraft, nuclear power controllers, fuel controllers, car equipment including car accessories, safety devices, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.) ; or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

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This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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