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## NTE5534A Silicon Controlled Rectifier (SCR) 600V, 50 Amp, TO3 Isolated Square Pack

**Description:**

The NTE5534A is a general purpose SCR in a TO3 isolated high power square pack designed for use in applications where power handling and power dissipation are critical, such as solid state relays, welding equipment, and high power motor controls.

Based on a clip assembly technology, the NTE5534A offers superior performance in surge current handling capabilities.

**Features:**

- High Stability and Reliability
- High Surge Capability
- High On-State Current
- Easy Mounting (Fast-On Connections)
- Isolated Package: Insulating Voltage = 2500V<sub>RMS</sub>

**Absolute Maximum Ratings:** (Limiting Values)

RMS On-State Current ( $T_C = +75^\circ\text{C}$ , 180° Conduction Angle), $I_{T(RMS)}$ .....	50A
Average On-State Current ( $T_C = +75^\circ\text{C}$ , 180° Conduction Angle), $I_{T(AV)}$ .....	32A
Non-Repetitive Surge Peak On-State Current ( $T_J = +25^\circ\text{C}$ ), $I_{TSM}$	
$t = 8.3\text{ms}$ .....	610A
$t = 10\text{ms}$ .....	580A
$I^2t$ Value for Fusing ( $T_J = +25^\circ\text{C}$ ), $I^2t$ .....	1680A <sup>2</sup> s
Critical Rate of Rise On-State Current, $di/dt$	
( $I_G = 160\text{mA}$ , $t_r \leq 100\text{ns}$ , $F = 60\text{Hz}$ , $T_J = +125^\circ\text{C}$ ) .....	50A/ $\mu\text{s}$
Peak Gate Current ( $t_p = 20\mu\text{s}$ , $T_J = +125^\circ\text{C}$ ), $I_{GM}$ .....	8A
Average Gate Power Dissipation ( $T_J = +125^\circ\text{C}$ ), $P_{G(AV)}$ .....	1W
Maximum Peak Reverse Gate Voltage, $V_{GRM}$ .....	5V
Operating Junction Temperature Range, $T_J$ .....	-40° to +125°C
Storage Temperature Range, $T_{stg}$ .....	-40° to +150°C
Thermal Resistance, Junction-to-Case, $R_{thJC}$ .....	0.9°C/W
Thermal Resistance, Junction-to-Ambient, $R_{thJA}$ .....	50°C/W

**Electrical Characteristics:** ( $T_J = +25^\circ\text{C}$  unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Gate Trigger Current	$I_{GT}$	$V_D = 12\text{V}, R_L = 33\Omega$	8	-	80	mA
Gate Trigger Voltage	$V_{GT}$	$V_D = 12\text{V}, R_L = 33\Omega$	-	-	1.3	V
Gate Non-Trigger Voltage	$V_{GD}$	$T_J = +125^\circ\text{C}, V_D = 600\text{V}, R_L = 3.3\text{k}\Omega$	0.2	-	-	V
Holding Current	$I_H$	$I_T = 500\text{mA}, \text{Gate Open}$	-	-	150	mA
Latching Current	$I_L$	$I_G = 1.2 \times I_{GT}$	-	-	200	mA
Critical Rise of Off-State Voltage	$dV/dt$	$T_J = 125^\circ\text{C}, \text{Gate Open}, V_D = 402\text{V}$	1000	-	-	$\text{V}/\mu\text{s}$
Peak On-State Voltage	$V_{TM}$	$I_{TM} = 100\text{A}, t_p = 380\mu\text{s}, T_J = 25^\circ\text{C}$	-	-	1.9	V
Threshold Voltage	$V_{TO}$	$T_J = 125^\circ\text{C}$	-	-	1.0	V
Dynamic Resistance	$R_d$	$T_J = 125^\circ\text{C}$	-	-	8.5	$\text{m}\Omega$
Peak Forward Blocking Current	$I_{DRM}$	$V_{DRM} = 600\text{V}$	-	-	10	$\mu\text{A}$
		$T_J = +125^\circ\text{C}$	-	-	5	mA
Peak Reverse Blocking Current	$I_{RRM}$	$V_{DRM} = 600\text{V}$	-	-	10	$\mu\text{A}$
		$T_J = +125^\circ\text{C}$	-	-	5	mA

