MC74LCX158

Low-Voltage CMOS Quad 2-Input Multiplexer

With 5 V−Tolerant Inputs (Inverting)

The MC74LCX158 is a high performance, quad 2−input inverting multiplexer operating from a 2.3 to 3.6 V supply. High impedance TTL compatible inputs significantly reduce current loading to input drivers while TTL compatible outputs offer improved switching noise performance. A V_I specification of 5.5 V allows MC74LCX158 inputs to be safely driven from 5 V devices.

Four bits of data from two sources can be selected using the Select and Enable inputs. The four outputs present the selected data in the inverted form. The MC74LCX158 can also be used as a function generator. Current drive capability is 24 mA at the outputs.

Features

- Designed for 2.3 to 3.6 V V_{CC} Operation
- 5 V Tolerant Inputs − Interface Capability With 5 V TTL Logic
- LVTTL Compatible
- LVCMOS Compatible
- 24 mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current (10 μA) Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 500 mA
- ESD Performance:
  - ♦ Human Body Model >2000 V
  - ♦ Machine Model >200 V
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

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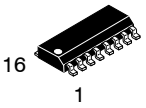
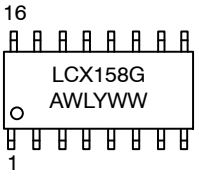
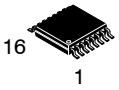
MARKING DIAGRAMS

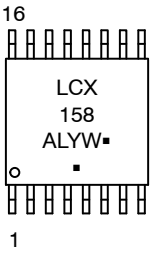


SOIC−16
D SUFFIX
CASE 751B





TSSOP−16
DT SUFFIX
CASE 948F



A	=	Assembly Location
WL, L	=	Wafer Lot
Y	=	Year
WW, W	=	Work Week
G or ▪	=	Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 3 of this data sheet.

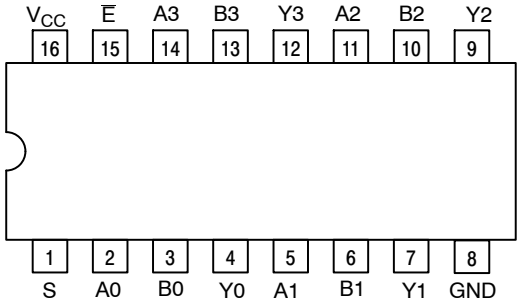


Figure 1. Pinout: 16−Lead Plastic Package (Top View)

PIN NAMES

Pins	Function
An	Source 0 Data Inputs
Bn	Source 1 Data Inputs
$\overline{E}$	Enable Input
S	Select Input
Yn	Outputs

TRUTH TABLE

Inputs		Outputs
Output Enable	**Select**	**Y0−Y3**
H	X	H
L	L	A0−A3
L	H	B0−B3

X = Don't Care
A0−A3, B0−B3 = The levels of the respective Data−Word Inputs

PIN DESCRIPTIONS

INPUTS

A0−A3 (Pins 2, 5, 11, 14)
Nibble A inputs. The data present on these pins is transferred to the outputs when the Select input is at a low level and the Output Enable input is at a low level. The data is presented to the outputs in inverted form for the LCX158.

B0−B3 (Pins 3, 6, 10, 13)
Nibble B inputs. The data present on these pins is transferred to the outputs when the Select input is at a high level and the Output Enable input is at a low level. The data is presented to the outputs in inverted form for the LCX158.

OUTPUTS

Y0−Y3 (Pins 4, 7, 9, 12)
Data outputs. The selected input nibble is presented at these outputs when the Output Enable input is at a low level. The data present on these pins is in its inverted form for the LCX158. For the Output Enable input at a high level, the outputs are at a high level for the LCX158.

Select (Pin 1)
Nibble select. This input determines the data word to be transferred to the outputs. A low level on this input selects the A inputs and a high level selects the B inputs.

CONTROL INPUTS

Enable (Pin 15)
Output Enable input. A low level on this input allows the selected data to be presented at the outputs. A high level on this input sets all of the outputs to a high level for the LCX158.

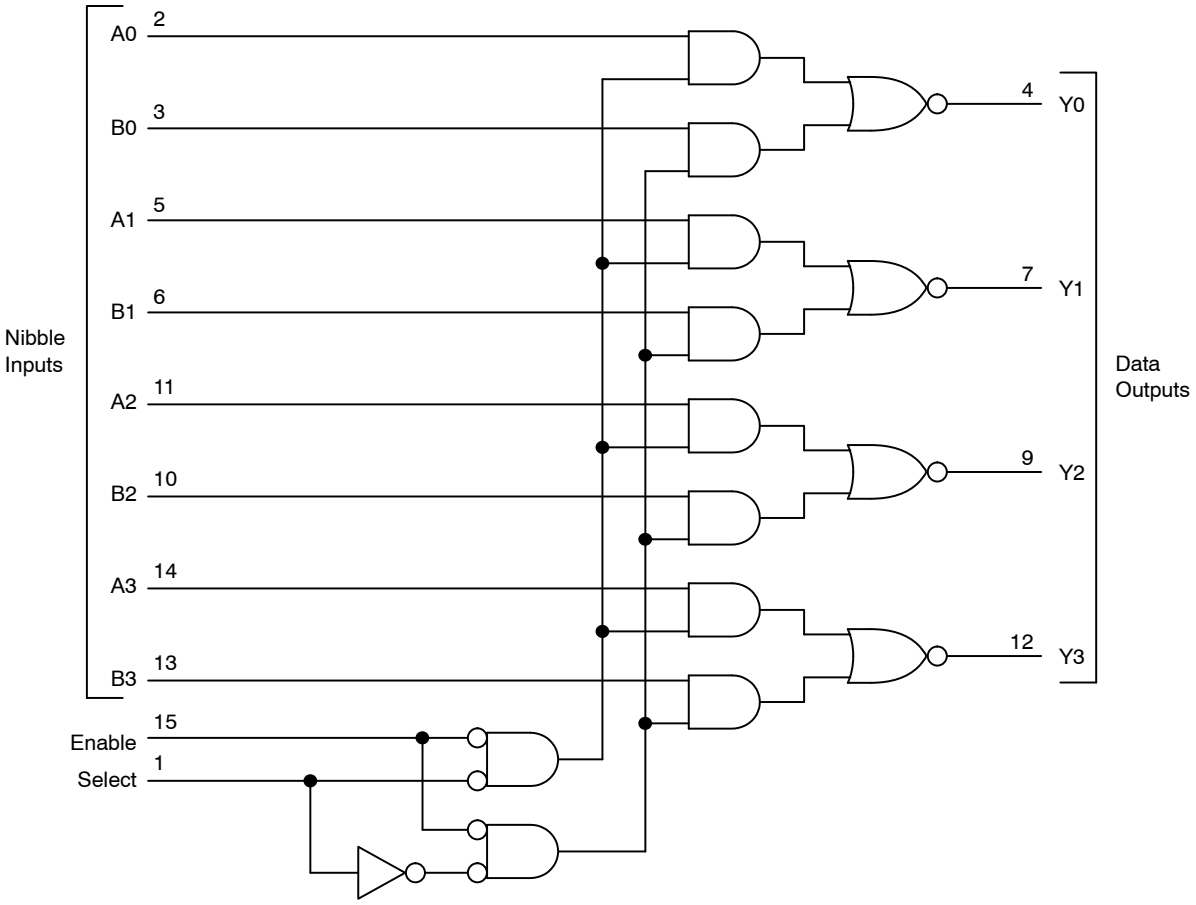


Figure 2. Expanded Logic Diagram

ORDERING INFORMATION

Device	Package	Shipping†
MC74LCX158DG	SOIC−16 (Pb−Free)	48 Units / Rail
MC74LCX158DR2G	SOIC−16 (Pb−Free)	2500 Tape & Reel
MC74LCX158DTG	TSSOP−16 (Pb−Free)	96 Units / Rail
MC74LCX158DTR2G	TSSOP−16 (Pb−Free)	2500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MAXIMUM RATINGS

Symbol	Parameter	Value	Condition	Units
V_{CC}	DC Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	$-0.5 \le V_I \le +7.0$		V
V_O	DC Output Voltage	$-0.5 \le V_O \le V_{CC} + 0.5$	Output in HIGH or LOW State (Note 1)	V
I_{IK}	DC Input Diode Current	−50	$V_I < GND$	mA
I_{OK}	DC Output Diode Current	−50	$V_O < GND$	mA
		+50	$V_O > V_{CC}$	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current Per Supply Pin	±100		mA
I_{GND}	DC Ground Current Per Ground Pin	±100		mA
T_{STG}	Storage Temperature Range	−65 to +150		°C
MSL	Moisture Sensitivity		Level 1	

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. I_O absolute maximum rating must be observed.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Units
V_{CC}	Supply Voltage Operating Data Retention Only	 2.0 1.5	 2.3 to 3.3	 3.6 3.6	V
V_I	Input Voltage	0		5.5	V
V_O	Output Voltage (HIGH or LOW State) (3−State)	 0		 V_{CC}	V
I_{OH}	HIGH Level Output Current V_{CC} = 3.0 V − 3.6 V V_{CC} = 2.7 V − 3.0 V V_{CC} = 2.3 V − 2.7 V			 −24 −12 −8	mA
I_{OL}	LOW Level Output Voltage V_{CC} = 3.0 V − 3.6 V V_{CC} = 2.7 V − 3.0 V V_{CC} = 2.3 V − 2.7 V			 +24 +12 +8	mA
T_A	Operating Free−Air Temperature	−40		+85	°C
$\Delta t/\Delta V$	Input Transition Rise or Fall Rate, V_{IN} from 0.8 V to 2.0 V, V_{CC} = 3.0 V	0		10	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic	Condition	T_A = −40°C to +85°C		Units
			Min	Max	
V_{IH}	Minimum HIGH Level Input Voltage (Note 2)	2.3 V ≤ V_{CC} ≤ 2.7 V 2.7 V ≤ V_{CC} ≤ 3.0 V 3.0 V ≤ V_{CC} ≤ 3.6 V	1.7 2.0 2.0		V
V_{IL}	Maximum LOW Level Input Voltage (Note 2)	2.3 V ≤ V_{CC} ≤ 2.7 V 2.7 V ≤ V_{CC} ≤ 3.0 V 3.0 V ≤ V_{CC} ≤ 3.6 V		0.7 0.8 0.8	V
V_{OH}	Minimum HIGH Level Output Voltage	2.3 V ≤ V_{CC} ≤ 3.6 V; I_{OH} = −100 μA V_{CC} = 2.3 V; I_{OH} = −8 mA V_{CC} = 2.7 V; I_{OH} = −12 mA V_{CC} = 3.0 V; I_{OH} = −18 mA V_{CC} = 3.0 V; I_{OH} = −24 mA	V_{CC} − 0.2 1.7 2.2 2.4 2.2		V
V_{OL}	Maximum LOW Level Output Voltage	2.3 V ≤ V_{CC} ≤ 3.6 V; I_{OH} = 100 μA V_{CC} = 2.3 V; I_{OH} = 8 mA V_{CC} = 2.7 V; I_{OH} = 12 mA V_{CC} = 3.0 V; I_{OH} = 16 mA V_{CC} = 3.0 V; I_{OH} = 24 mA		0.2 0.7 0.4 0.4 0.55	V
I_{OFF}	Power Off Leakage Current	V_{CC} = 0, V_{IN} = 5.5 V or V_{OUT} = 5.5 V		10	μA
I_{IN}	Input Leakage Current	V_{CC} = 3.6 V, V_{IN} = 5.5 V or GND		±5	μA
I_{CC}	Quiescent Supply Current	V_{CC} = 3.6 V, V_{IN} = 5.5 V or GND		10	μA
ΔI_{CC}	Increase in I_{CC} per Input	2.3 ≤ V_{CC} ≤ 3.6 V; V_{IH} = V_{CC} − 0.6 V		500	μA

2. These values of V_I are used to test DC electrical characteristics only.

AC CHARACTERISTICS

Symbol	Parameter	Limits						Units
		T_A = −40°C to +85°C						
		V_{CC} = 3.0 V ± 3.6 V		V_{CC} = 2.7 V		V_{CC} = 2.3 V to 2.7 V		
		C_L = 50 pF		C_L = 50 pF		C_L = 30 pF		
		Min	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation Delay A or B to Y	1.0 1.0	6.5 6.5	1.0 1.0	7.5 7.5	1.0 1.0	8.5 8.5	ns
t_{PLH} t_{PHL}	Propagation Delay S to Y	1.0 1.0	7.0 7.0	1.0 1.0	8.0 8.0	1.0 1.0	9.0 9.0	ns
t_{PLH} t_{PHL}	Propagation Delay Output Enable to Y	1.0 1.0	7.0 7.0	1.0 1.0	8.0 8.0	1.0 1.0	9.0 9.0	ns
t_{OSHL} t_{OSLH}	Output−to−Output Skew		1.0 1.0					ns

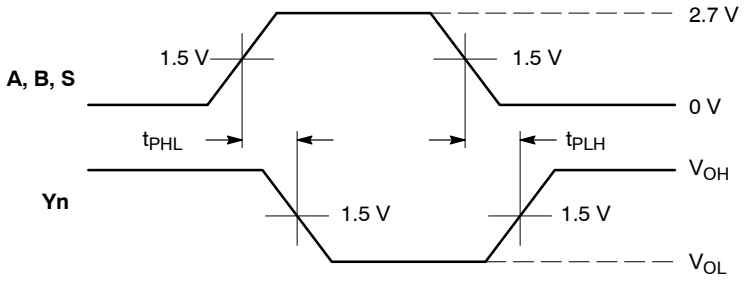
DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Characteristic	Condition	T_A = +25°C			Units
			Min	Typ	Max	
V_{OLP}	Dynamic LOW Peak Voltage (Note 3)	V_{CC} = 3.3 V, C_L = 50 pF, V_{IH} = 3.3 V, V_{IL} = 0 V		0.8		V
V_{OLV}	Dynamic LOW Valley Voltage (Note 3)	V_{CC} = 3.3 V, C_L = 50 pF, V_{IH} = 3.3 V, V_{IL} = 0 V		0.8		V

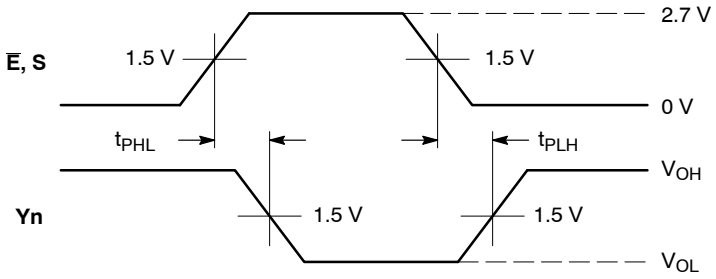
3. Number of outputs defined as “n”. Measured with “n−1” outputs switching from HIGH−to−LOW or LOW−to−HIGH. The remaining output is measured in the LOW state.

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = 3.3 V, V_I = 0 V or V_{CC}	7	pF
C_{OUT}	Output Capacitance	V_{CC} = 3.3 V, V_I = 0 V or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	10 MHz, V_{CC} = 3.3 V, V_I = 0 V or V_{CC}	25	pF

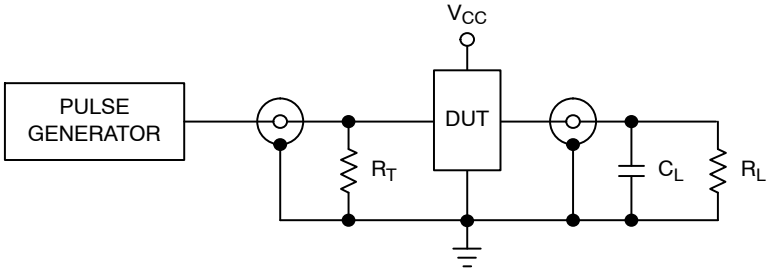


WAVEFORM 1 – INVERTING PROPAGATION DELAYS
$t_R = t_F$ = 2.5 ns, 10% to 90%; f = 1 MHz; t_W = 500 ns



WAVEFORM 2 – INVERTING PROPAGATION DELAYS
$t_R = t_F$ = 2.5 ns, 10% to 90%; f = 1 MHz; t_W = 500 ns

Figure 3. AC Waveforms



C_L = 50 pF or equivalent (Includes jig and probe capacitance)
R_L = R_1 = 500 Ω or equivalent
R_T = Z_{OUT} of pulse generator (typically 50 Ω)

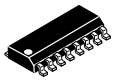
Figure 4. Test Circuit

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

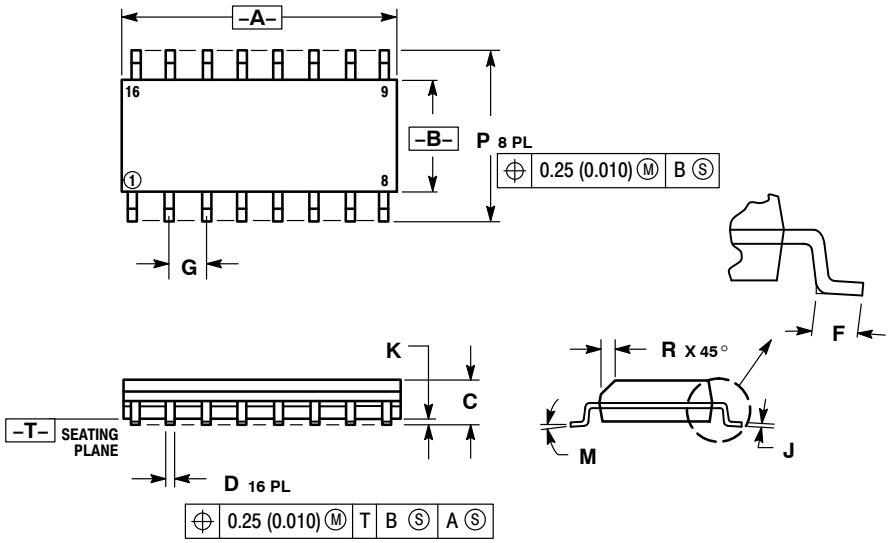
ON Semiconductor®

SOIC−16
CASE 751B−05
ISSUE K

DATE 29 DEC 2006



SCALE 1:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

STYLE 1:
PIN 1. COLLECTOR
2. BASE
3. EMITTER
4. NO CONNECTION
5. EMITTER
6. BASE
7. COLLECTOR
8. COLLECTOR
9. BASE
10. EMITTER
11. NO CONNECTION
12. EMITTER
13. BASE
14. COLLECTOR
15. EMITTER
16. COLLECTOR

STYLE 2:
PIN 1. CATHODE
2. ANODE
3. NO CONNECTION
4. CATHODE
5. CATHODE
6. NO CONNECTION
7. ANODE
8. CATHODE
9. CATHODE
10. ANODE
11. NO CONNECTION
12. CATHODE
13. CATHODE
14. NO CONNECTION
15. ANODE
16. CATHODE

STYLE 3:
PIN 1. COLLECTOR, DYE #1
2. BASE, #1
3. EMITTER, #1
4. COLLECTOR, #1
5. COLLECTOR, #2
6. BASE, #2
7. EMITTER, #2
8. COLLECTOR, #2
9. COLLECTOR, #3
10. BASE, #3
11. EMITTER, #3
12. COLLECTOR, #3
13. COLLECTOR, #4
14. BASE, #4
15. EMITTER, #4
16. COLLECTOR, #4

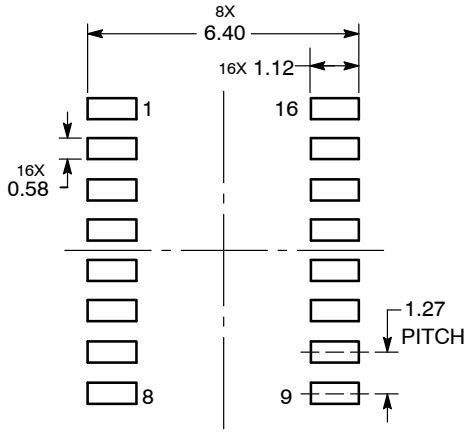
STYLE 4:
PIN 1. COLLECTOR, DYE #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. COLLECTOR, #3
6. COLLECTOR, #3
7. COLLECTOR, #4
8. COLLECTOR, #4
9. BASE, #4
10. EMITTER, #4
11. BASE, #3
12. EMITTER, #3
13. BASE, #2
14. EMITTER, #2
15. BASE, #1
16. EMITTER, #1

STYLE 5:
PIN 1. DRAIN, DYE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. DRAIN, #3
6. DRAIN, #3
7. DRAIN, #4
8. DRAIN, #4
9. GATE, #4
10. SOURCE, #4
11. GATE, #3
12. SOURCE, #3
13. GATE, #2
14. SOURCE, #2
15. GATE, #1
16. SOURCE, #1

STYLE 6:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. CATHODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE
15. ANODE
16. ANODE

STYLE 7:
PIN 1. SOURCE N-CH
2. COMMON DRAIN (OUTPUT)
3. COMMON DRAIN (OUTPUT)
4. GATE P-CH
5. COMMON DRAIN (OUTPUT)
6. COMMON DRAIN (OUTPUT)
7. COMMON DRAIN (OUTPUT)
8. SOURCE P-CH
9. SOURCE P-CH
10. COMMON DRAIN (OUTPUT)
11. COMMON DRAIN (OUTPUT)
12. COMMON DRAIN (OUTPUT)
13. GATE N-CH
14. COMMON DRAIN (OUTPUT)
15. COMMON DRAIN (OUTPUT)
16. SOURCE N-CH

SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

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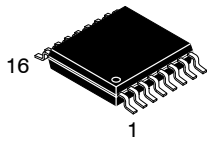
DESCRIPTION:	SOIC−16	PAGE 1 OF 1

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

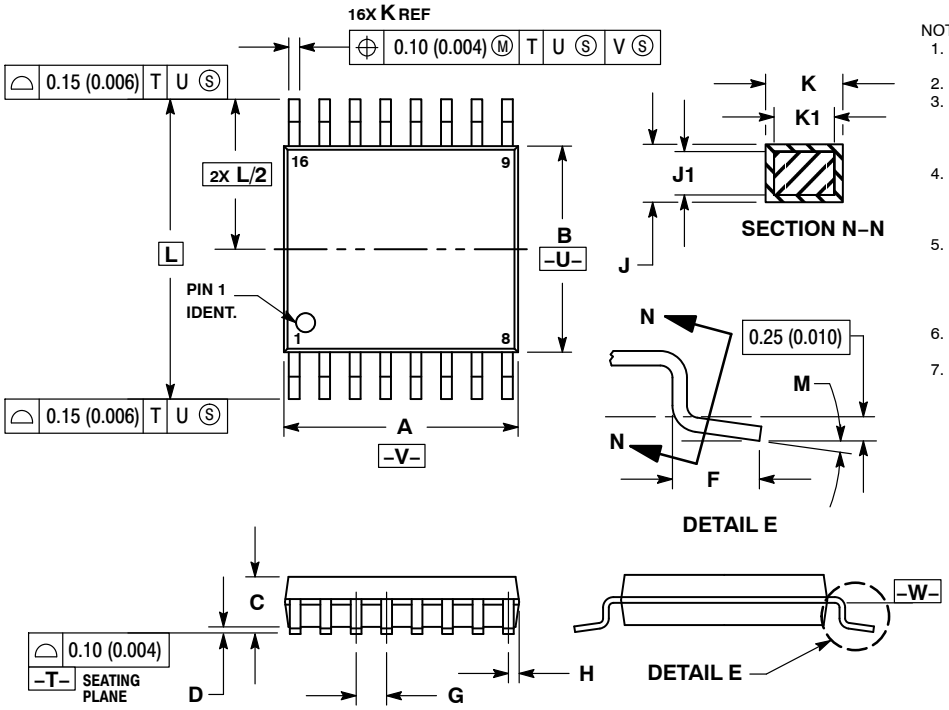
ON Semiconductor®



SCALE 2:1

TSSOP−16
CASE 948F−01
ISSUE B

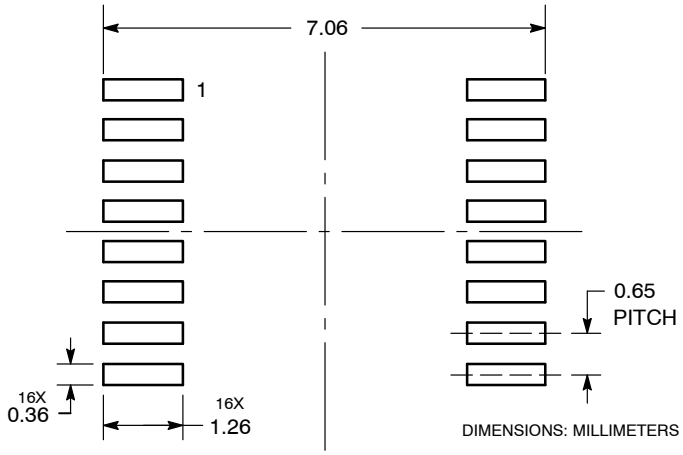
DATE 19 OCT 2006



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

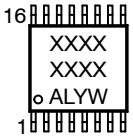
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	−−−	1.20	−−−	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

GENERIC MARKING DIAGRAM*



XXXX	= Specific Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
G or ▪	= Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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