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MOSFET – Power, Single N-Channel

60 V, 6.8 mΩ, 71 A



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NVTYS006N06CL

Features

- Small Footprint (3.3 x 3.3 mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit	
Drain-to-Source Voltage	V_{DSS}	60	V	
Gate-to-Source Voltage	V_{GS}	± 20	V	
Continuous Drain Current $R_{\theta JC}$ (Notes 1, 2, 3, 4)	Steady State	$T_C = 25^\circ\text{C}$	71	A
		$T_C = 100^\circ\text{C}$	50	
Power Dissipation $R_{\theta JC}$ (Notes 1, 2, 3)	Steady State	$T_C = 25^\circ\text{C}$	61	W
		$T_C = 100^\circ\text{C}$	31	
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 3, 4)	Steady State	$T_A = 25^\circ\text{C}$	16	A
		$T_A = 100^\circ\text{C}$	11	
Power Dissipation $R_{\theta JA}$ (Notes 1, 3)	Steady State	$T_A = 25^\circ\text{C}$	3.2	W
		$T_A = 100^\circ\text{C}$	1.6	
Pulsed Drain Current	$T_A = 25^\circ\text{C}, t_p = 10 \mu\text{s}$	I_{DM}	322	A
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to +175	$^\circ\text{C}$	
Source Current (Body Diode)	I_S	51	A	
Single Pulse Drain-to-Source Avalanche Energy ($I_{L(pk)} = 3.6 \text{ A}$)	E_{AS}	115	mJ	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	T_L	260	$^\circ\text{C}$	

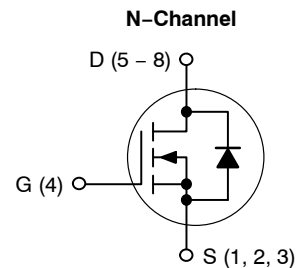
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS (Note 1)

Parameter	Symbol	Value	Unit
Junction-to-Case – Steady State (Note 3)	$R_{\theta JC}$	2.4	$^\circ\text{C}/\text{W}$
Junction-to-Ambient – Steady State (Note 3)	$R_{\theta JA}$	47	

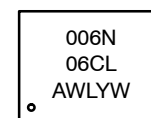
1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Psi (Ψ) is used as required per JESD51-12 for packages in which substantially less than 100% of the heat flows to single case surface.
3. Surface-mounted on FR4 board using a 650 mm², 2 oz. Cu pad.
4. Continuous DC current rating. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

$V_{(BR)DSS}$	$R_{DS(on)} \text{ MAX}$	$I_D \text{ MAX}$
60 V	6.8 mΩ @ 10 V	71 A
	10 mΩ @ 4.5 V	



LFPAK8
3.3x3.3
CASE 760AD

MARKING DIAGRAM



006N06CL = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

NVTYS006N06CL

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	60			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$			28		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = 60\text{ V}$	$T_J = 25^\circ\text{C}$		10	μA
			$T_J = 125^\circ\text{C}$		250	
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = 20\text{ V}$			100	nA

ON CHARACTERISTICS (Note 5)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 53\ \mu\text{A}$	1.2		2.0	V
Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			-4.8		mV/°C
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 35\text{ A}$		5.8	6.8	$\text{m}\Omega$
		$V_{GS} = 4.5\text{ V}, I_D = 35\text{ A}$		8.1	10	
Forward Transconductance	g_{FS}	$V_{DS} = 5\text{ V}, I_D = 35\text{ A}$		67		S

CHARGES AND CAPACITANCES

Input Capacitance	C_{ISS}	$V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = 25\text{ V}$		1330		pF
Output Capacitance	C_{OSS}			740		
Reverse Transfer Capacitance	C_{RSS}			11		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 48\text{ V}, I_D = 35\text{ A}$		8		nC
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 10\text{ V}, V_{DS} = 48\text{ V}, I_D = 35\text{ A}$		19		nC
Threshold Gate Charge	$Q_{G(TH)}$	$V_{GS} = 10\text{ V}, V_{DS} = 48\text{ V}, I_D = 35\text{ A}$		2		nC
Gate-to-Source Charge	Q_{GS}			4.3		
Gate-to-Drain Charge	Q_{GD}			1.6		
Plateau Voltage	V_{GP}			3.1		

SWITCHING CHARACTERISTICS (Note 6)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 48\text{ V}, I_D = 35\text{ A}, R_G = 2.5\ \Omega$		13.6		ns
Rise Time	t_r			7.7		
Turn-Off Delay Time	$t_{d(OFF)}$			16.3		
Fall Time	t_f			6.1		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_S = 35\text{ A}$	$T_J = 25^\circ\text{C}$		0.9	1.2	V
			$T_J = 125^\circ\text{C}$		0.8		
Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{ V}, di_S/dt = 100\text{ A}/\mu\text{s}, I_S = 35\text{ A}$		37		ns	
Charge Time	t_a			18			
Discharge Time	t_b			19			
Reverse Recovery Charge	Q_{RR}			22			nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Pulse Test: pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.

6. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

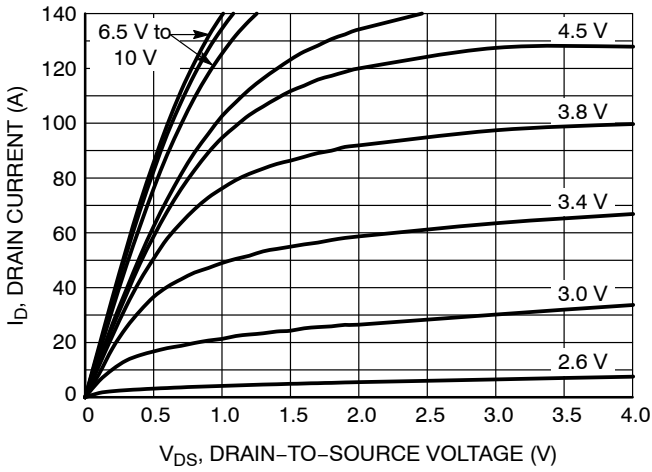


Figure 1. On-Region Characteristics

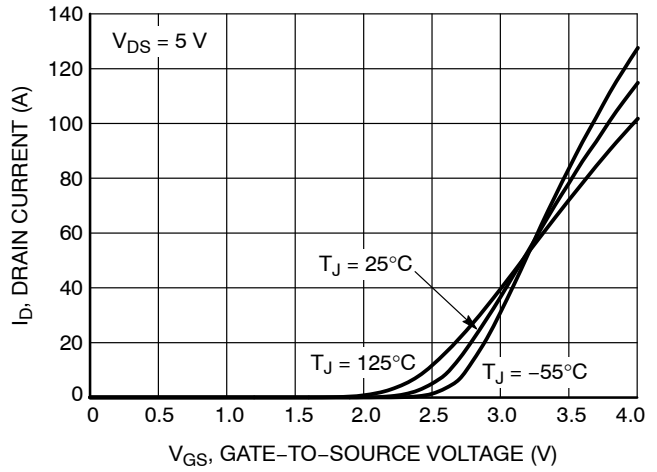


Figure 2. Transfer Characteristics

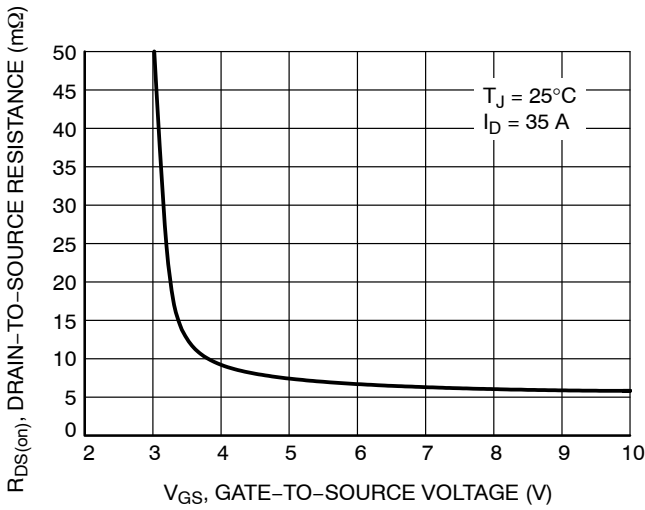


Figure 3. On-Resistance vs. Gate-to-Source Voltage

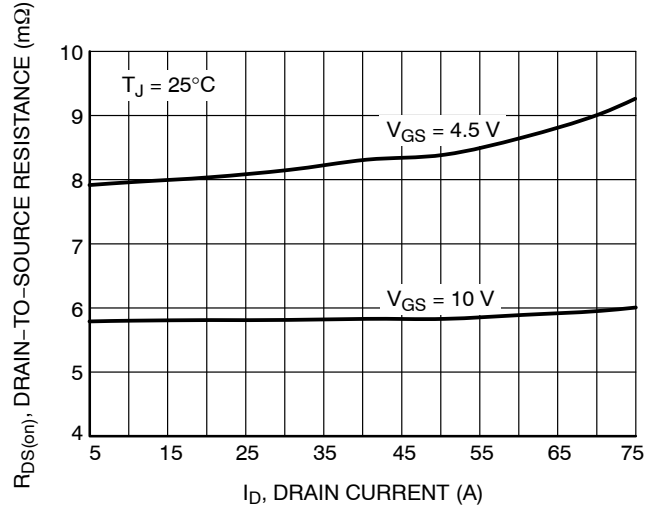


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

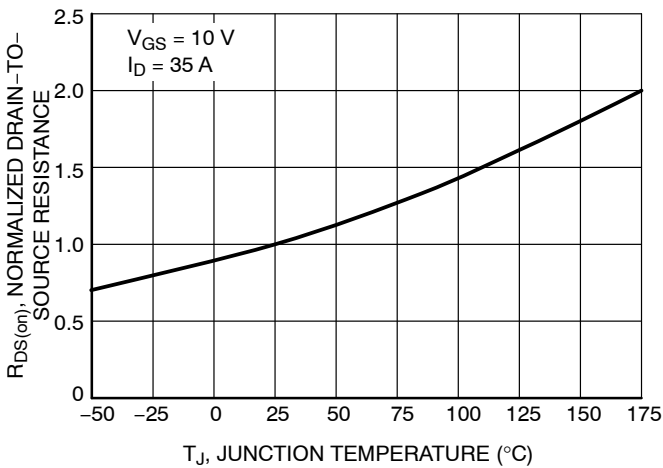


Figure 5. On-Resistance Variation with Temperature

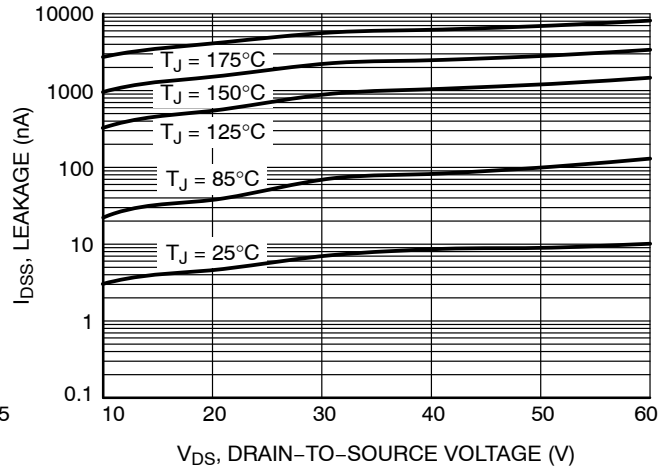


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

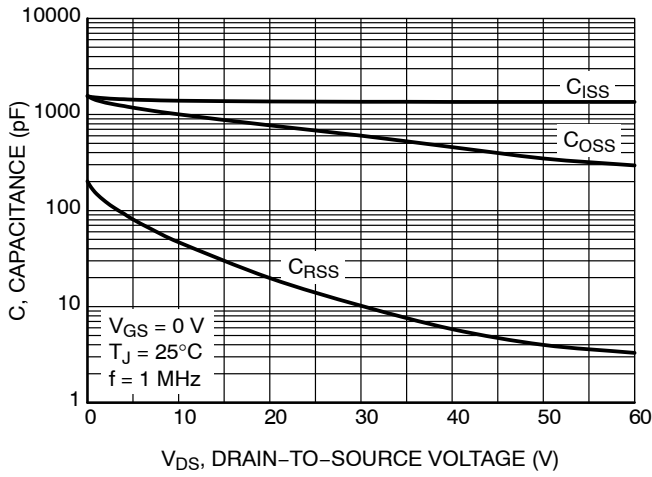


Figure 7. Capacitance Variation

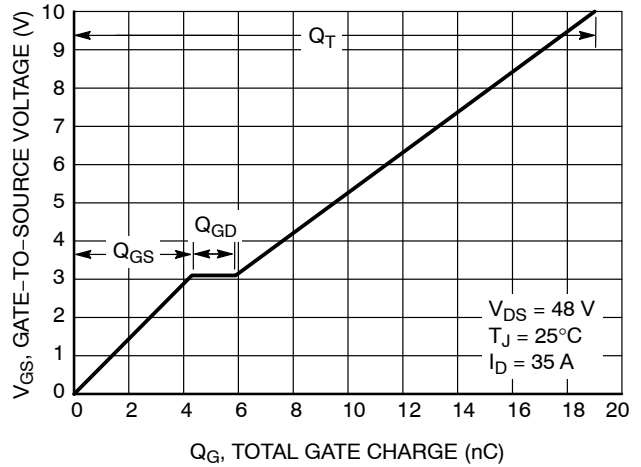


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

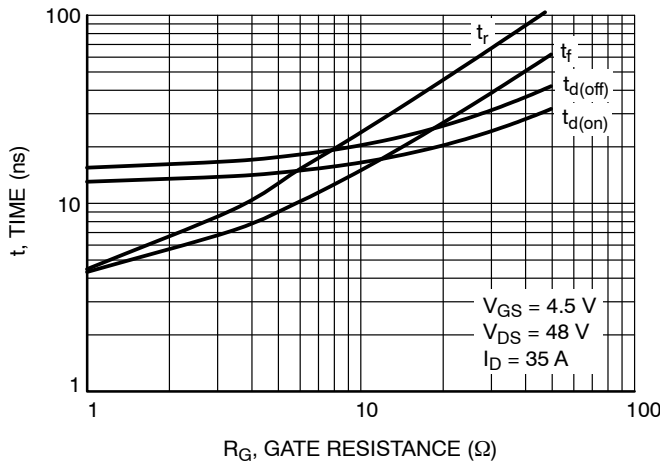


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

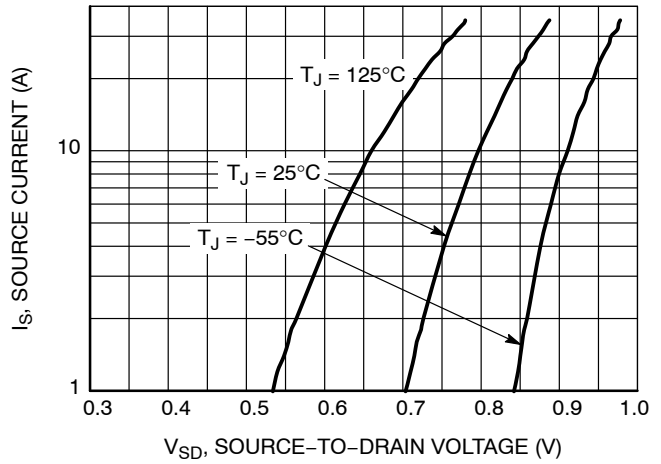


Figure 10. Diode Forward Voltage vs. Current

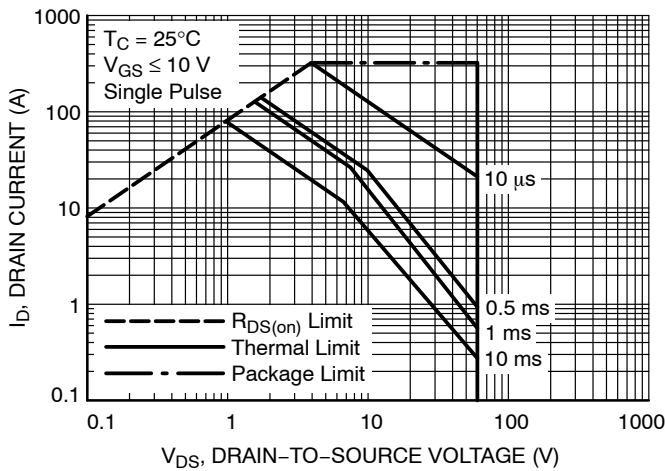


Figure 11. Maximum Rated Forward Biased Safe Operating Area

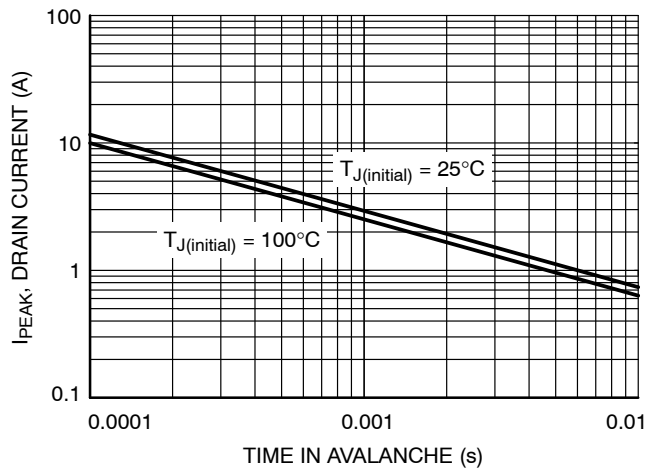


Figure 12. Maximum Drain Current vs. Time in Avalanche

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TYPICAL CHARACTERISTICS

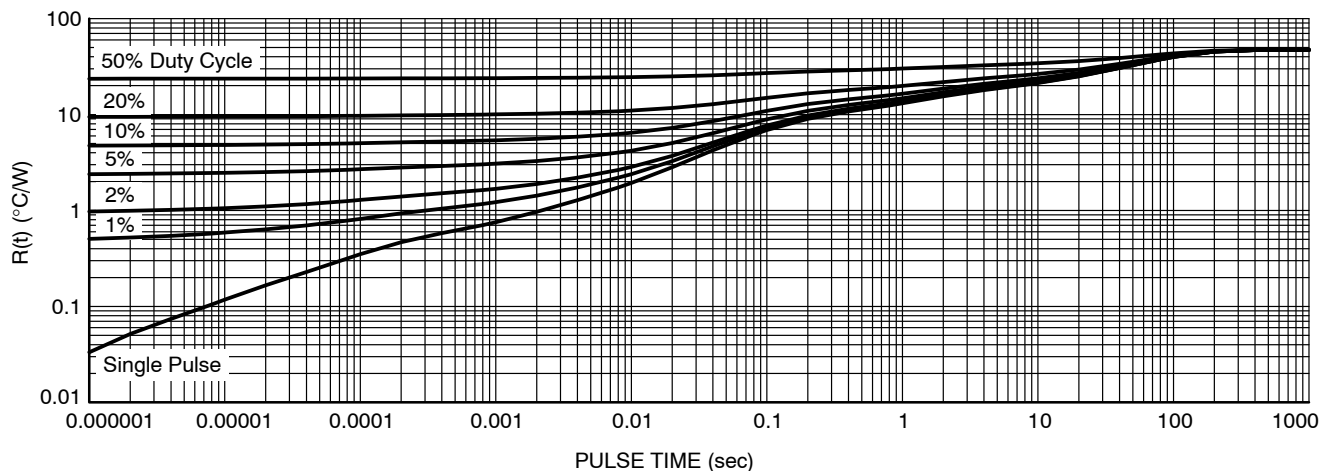


Figure 13. Thermal Characteristics

DEVICE ORDERING INFORMATION

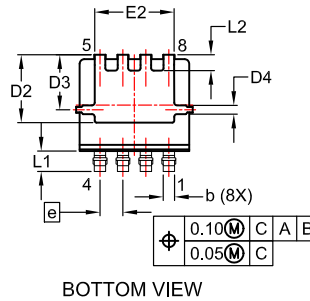
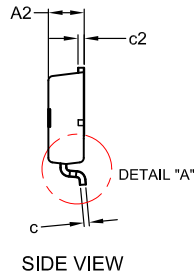
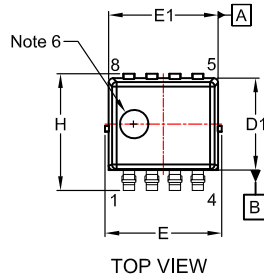
Device	Marking	Package	Shipping [†]
NVTYS006N06CLTWG	006N 06CL	LFPAK33	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

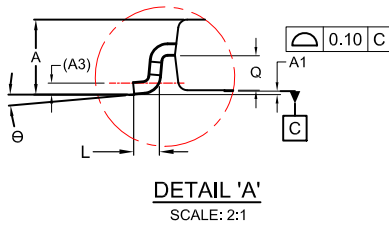
NVTYS006N06CL

PACKAGE DIMENSIONS

LFPAK8 3.3x3.3, 0.65P CASE 760AD ISSUE E

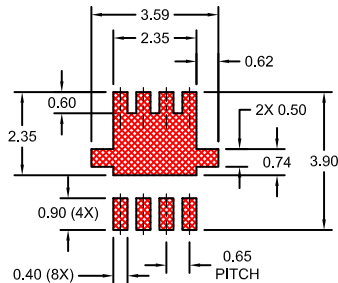


DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.95	1.05	1.15
A1	0.00	0.05	0.10
A2	0.95	1.00	1.05
A3	0.15 REF		
b	0.27	0.32	0.37
c	0.12	0.17	0.22
c2	0.12	0.17	0.22
D1	2.50	2.60	2.70
D2	1.82	1.92	2.02
D3	1.46	1.56	1.66
D4	0.20	0.25	0.30
E	3.20	3.30	3.40
E1	3.00	3.10	3.20
E2	2.15	2.25	2.35
e	0.65 BSC		
H	3.20	3.30	3.40
L	0.25	0.37	0.50
L1	0.48	0.58	0.68
L2	0.35	0.45	0.55
Q	0.45	0.50	0.55
θ	0°	4°	8°



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS OR BURRS SHALL NOT EXCEED 0.150mm PER SIDE.
4. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
5. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
6. OPTIONAL MOLD FEATURE.



LAND PATTERN RECOMMENDATION

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