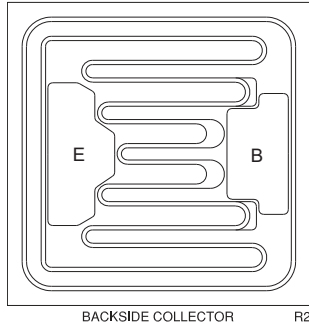


CP305-2N3019

NPN - High Current Transistor Die

The CP305-2N3019 is a silicon NPN transistor designed for high current, general purpose applications.



MECHANICAL SPECIFICATIONS:

Die Size	31 x 31 MILS
Die Thickness	9.0 MILS
Base Bonding Pad Size	5.9 x 11.8 MILS
Emitter Bonding Pad Size	6.5 x 13.8 MILS
Top Side Metalization	Al – 30,000Å
Back Side Metalization	Au – 18,000Å
Scribe Alley Width	1.96 MILS
Wafer Diameter	4 INCHES
Gross Die Per Wafer	11,212

MAXIMUM RATINGS: (T_A=25°C)

	SYMBOL		UNITS
Collector-Base Voltage	V _{CBO}	140	V
Collector-Emitter Voltage	V _{CEO}	80	V
Emitter-Base Voltage	V _{EBO}	7.0	V
Continuous Collector Current	I _C	1.0	A
Operating and Storage Junction Temperature	T _J , T _{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS: (T_A=25°C)

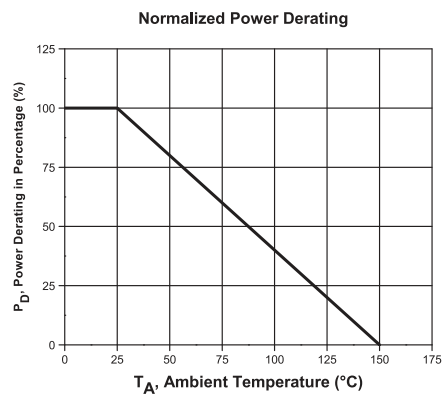
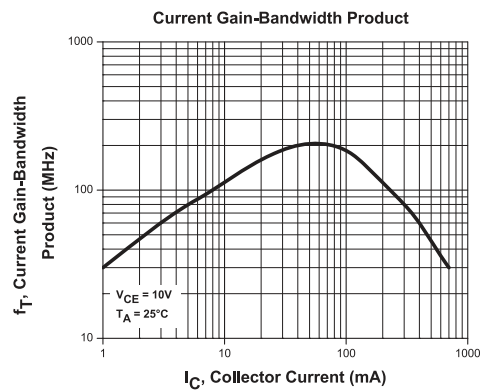
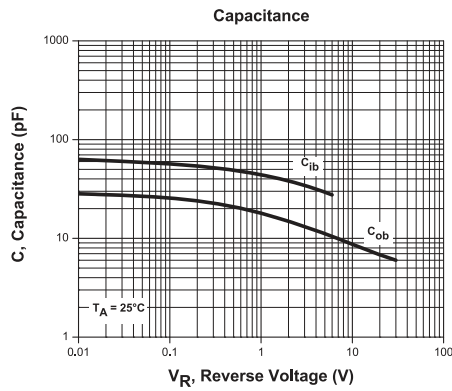
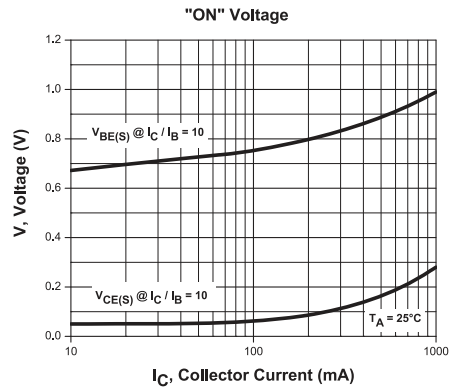
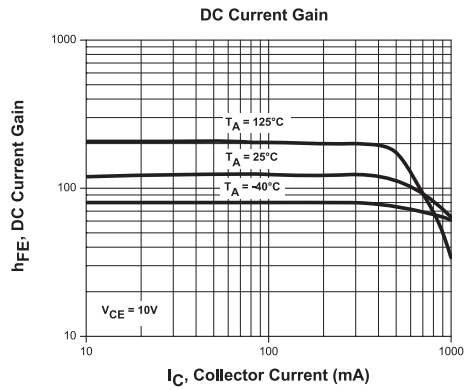
SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
I _{CBO}	V _{CB} =90V		10	nA
I _{EBO}	V _{EB} =5.0V		10	nA
BV _{CBO}	I _C =100μA	140		V
BV _{CEO}	I _C =30mA	80		V
BV _{EBO}	I _E =100μA	7.0		V
V _{CE(SAT)}	I _C =150mA, I _B =15mA		0.2	V
V _{CE(SAT)}	I _C =500mA, I _B =50mA		0.5	V
V _{BE(SAT)}	I _C =150mA, I _B =15mA		1.1	V
h _{FE}	V _{CE} =10V, I _C =100μA	50		
h _{FE}	V _{CE} =10V, I _C =10mA	90		
h _{FE}	V _{CE} =10V, I _C =150mA	100	300	
h _{FE}	V _{CE} =10V, I _C =500mA	50		
h _{FE}	V _{CE} =10V, I _C =1.0A	15		
f _T	V _{CE} =10V, I _C =50mA, f=20MHz	100		MHz
C _{ob}	V _{CB} =10V, I _E =0, f=1.0MHz		12	pF
C _{ib}	V _{EB} =0.5V, I _C =0, f=1.0MHz		60	pF

PACKING OPTIONS:

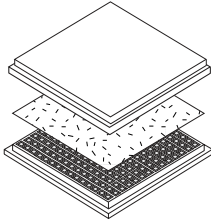
- CP305-2N3019-CT: Singulated die in waffle pack; 400 die per tray.
- CP305-2N3019-WN: Full wafer, unsawn, 100% tested with reject die inked.
- CP305-2N3019-WR: Full wafer, sawn and mounted on plastic ring, 100% tested with reject die inked.

CP305-2N3019

Typical Electrical Characteristics



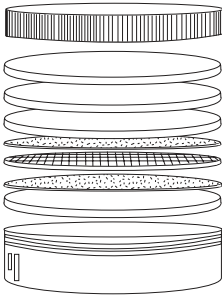
BARE DIE PACKING OPTIONS



BARE DIE IN TRAY (WAFFLE) PACK

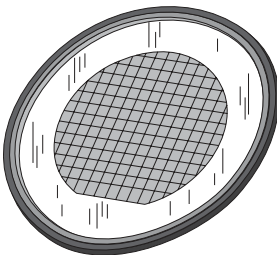
CT: Singulated die in tray (waffle) pack.
(example: CP211-PART NUMBER-CT)

CM: Singulated die in tray (waffle) pack 100% visually inspected as per MIL-STD-750, (method 2072 transistors, method 2073 diodes).
(example: CP211-PART NUMBER-CM)



UNSAWN WAFER

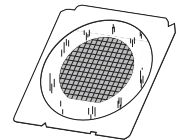
WN: Full wafer, unsawn, 100% tested with reject die inked.
(example: CP211-PART NUMBER-WN)



SAWN WAFER ON PLASTIC RING

WR: Full wafer, sawn and mounted on plastic ring,
100% tested with reject die inked.
(example: CP211-PART NUMBER-WR)

Please note: Sawn Wafer on Metal Frame (WS) is possible as a special order. Please contact your Central Sales Representative at 631-435-1110.



Visit the Central website for a complete listing of specifications:
www.centrasemi.com/bdspecs

OUTSTANDING SUPPORT AND SUPERIOR SERVICES



PRODUCT SUPPORT

Central's operations team provides the highest level of support to insure product is delivered on-time.

- Supply management (Customer portals)
- Inventory bonding
- Consolidated shipping options
- Custom bar coding for shipments
- Custom product packing

DESIGNER SUPPORT/SERVICES

Central's applications engineering team is ready to discuss your design challenges. Just ask.

- Free quick ship samples (2nd day air)
- Online technical data and parametric search
- SPICE models
- Custom electrical curves
- Environmental regulation compliance
- Customer specific screening
- Up-screening capabilities
- Special wafer diffusions
- PbSn plating options
- Package details
- Application notes
- Application and design sample kits
- Custom product and package development

REQUESTING PRODUCT PLATING

1. If requesting Tin/Lead plated devices, add the suffix "TIN/LEAD" to the part number when ordering (example: 2N2222A TIN/LEAD).
2. If requesting Lead (Pb) Free plated devices, add the suffix "PBFREE" to the part number when ordering (example: 2N2222A PBFREE).

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