FAIRCHILD SEMICONDUCTOR®

June 2011

FAB2200
Audio Subsystem with Stereo Class-G Headphone Amplifier and 1.2W Mono Class-D Speaker Amplifier

Features

- Single Supply: 2.8V – 5.25V
- Pop and Click Suppression
- Differential or Single-Ended Audio Inputs
- Rejects TDMA Noise from GSM Handsets
- Filterless Fully Differential Class-D Speaker Amplifier
  - Programmable Edge-Rate Control and Spread Spectrum Minimize EMI
  - 1.2W into 8Ω at 4.2V, THD+N < 10%
  - 970mW into 8Ω at 4.2V, THD+N < 1%
  - 90% Efficiency
  - Automatic Gain Control Limits Distortion and Protects Speakers at All Battery Voltages
  - Noise Gate Improves Audio Quality
- Headphone Amplifier
  - Power-Saving Class-G Operation
  - Audio Taper I^2C Volume Control
  - Capacitor-Free Outputs
  - Integrated Regulated Charge Pump
  - SGND Pin Eliminates Ground-Loop Noise
  - Noise Gate Improves Audio Quality
- DPST Analog Bypass Switch
- I^2C Control
- Low-Power Shutdown Mode
- Current Limit and Thermal Protection
- 25-Bump, 0.4mm Pitch WLCSP Package

Description

The FAB2200 combines a capacitor-free stereo headphone amplifier with a monolithic class-D speaker amplifier.

An integrated charge pump generates multiple supply rails for a ground-centered class-G headphone output. The charge pump is regulated for high Power Supply Rejection Ratio (PSRR).

The filterless class-D amplifier can be connected directly to a speaker without external filters.

The programmable Automatic Gain Control (AGC) limits maximum speaker output levels to protect speakers without introducing distortion. It can also dynamically limit clipping as the battery voltage falls.

The noise gate can automatically mute the speaker or headphone amplifiers to reduce noise when input signals are low.

Applications

- Cellular Handsets
- Notebook Computers
- Tablet PCs

Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
FAB2200UCX	-40 to +85°C	25-Bump, 0.4mm Pitch, Wafer-Level Chip-Scale Package (WLCSP)	3000 Units on Tape & Reel

Typical Application Circuit

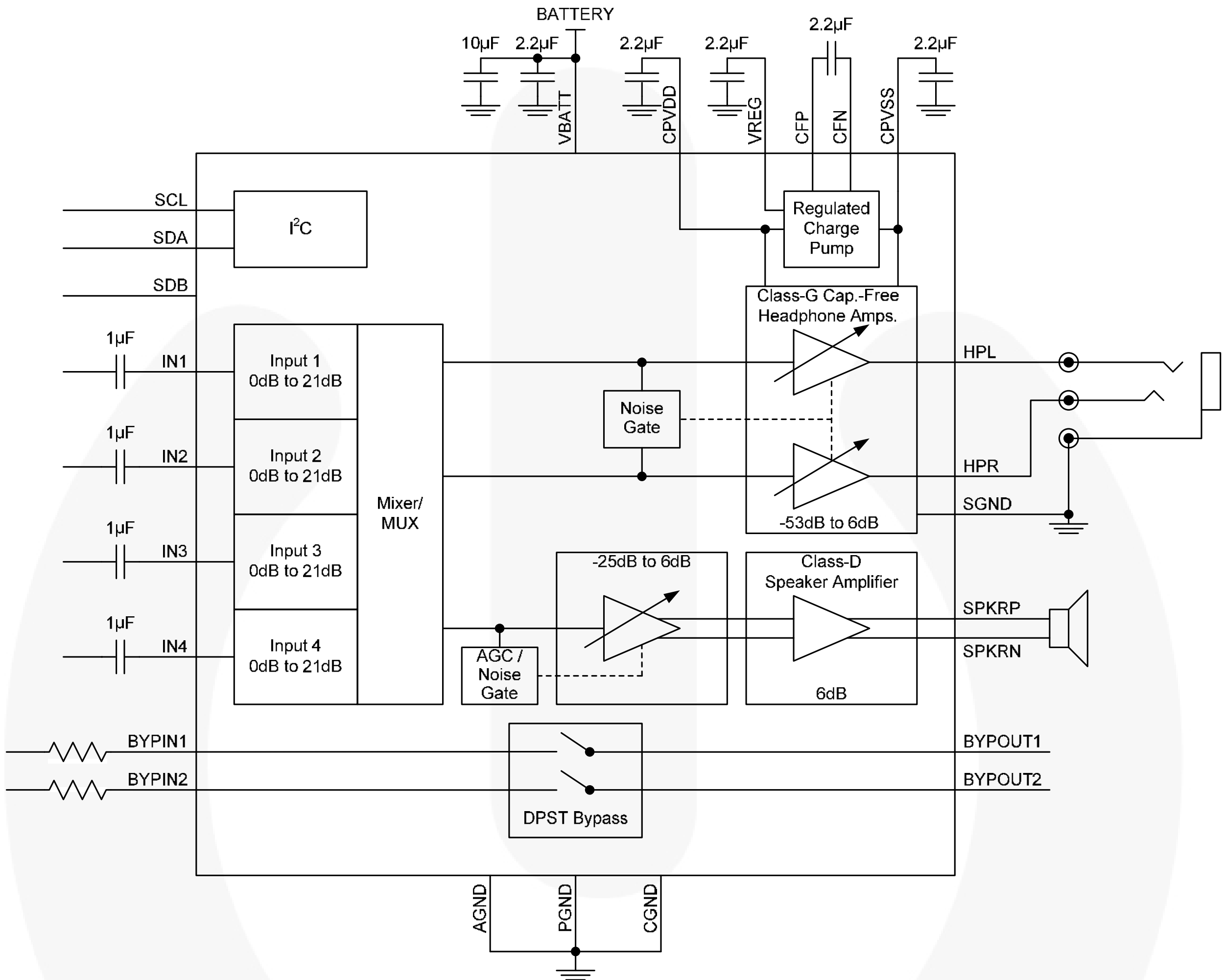

Figure 1. Typical Application Circuit

Pin Configuration

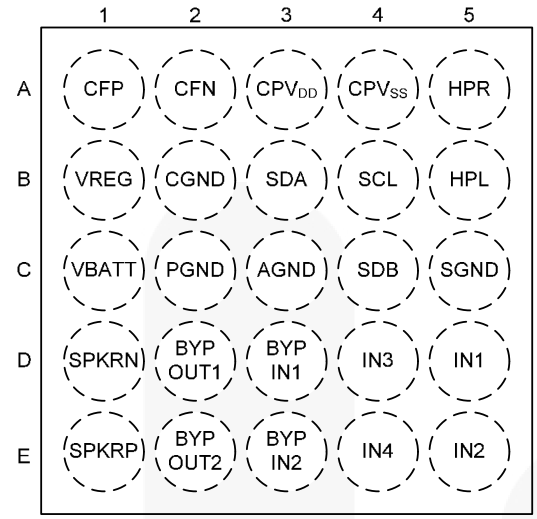

Figure 2. Top-View (Bump-Side Down)

Pin Definitions

WLCSP	Name	Description	Type
C1	VBATT	Power supply for speaker amplifier	Power
B2	PGND	Charge pump ground	Power
C2	PGND	Power ground	Power
C3	AGND	Analog ground	Power
B1	VREG	Charge pump regulator – do not connect to an external power supply	Power
A3	CPV_{DD}	Charge pump output – positive power supply for headphone amplifier	Power
A4	CPV_{SS}	Charge pump output – negative mirror of CPV_{DD}	Power
A1	CFP	Charge pump flying capacitor positive terminal	Power
A2	CFN	Charge pump flying capacitor negative terminal	Power
D5	IN1	Line level audio input	Input
E5	IN2	Line level audio input	Input
D4	IN3	Line level audio input	Input
E4	IN4	Line level audio input	Input
B5	HPL	Left headphone output	Output
A5	HPR	Right headphone output	Output
C5	SGND	Sense ground – connect to AGND close to shield terminal of headphone jack	Input
E1	SPKRP	Positive speaker output	Output
D1	SPKRN	Negative speaker output	Output
D3	BYPIN1	Analog bypass switch input	Input
E3	BYPIN2	Analog bypass switch input	Input
D2	BYPOUT1	Analog bypass switch output	Output
E2	BYPOUT2	Analog bypass switch output	Output
C4	SDB	Shutdown control	Input
B4	SCL	I^2C clock input	Input
B3	SDA	I^2C data I/O	Bi-directional

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The Absolute Maximum Ratings are stress ratings only. All voltages are referenced to GND.

Symbol	Parameter	Min.	Max.	Unit
V_{BATT}	Voltage on VBATT Pin	-0.3	6.0	V
V_{IN}	Voltage on IN1, IN2, IN3, IN4, HPL, HPR Pins	CPV_{SS}-0.3	CPV_{DD}+0.3	V
V_{SGND}	Voltage on SGND Pin	-0.3	0.3	V
V_S	Voltage on SDA, SCL, SDB Pins	-0.3	V_{BATT}+0.3	V
V_{SP}	Voltage on SPKRP, SPKRN Pins	-0.3	V_{BATT}+0.3	V
V_{BYP}	Voltage on BYPIN1, BYPIN2, BYPOUT1, BYPOUT2 Pins	-0.3	V_{BATT}+0.3	V
	Duration of SPKRP, SPKRN Short Circuit to GND or VBATT		Continuous	
	Duration of Short Circuit Between SPKRP and SPKRN		Continuous	
	Duration of HPL, HPR Short Circuit to GND		Continuous	

Reliability Information

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_J	Junction Temperature			+150	°C
T_{STG}	Storage Temperature Range	-65		+150	°C
T_L	Peak Reflow Temperature			+300	°C
θ_{JA}	Thermal Resistance, JEDEC Standard, Multilayer Test Boards, Still Air		60		°C/W
TSD	Thermal Shutdown Threshold		+150		°C
T_{HYS}	Thermal Shutdown Hysteresis		+35		°C

ESD Protection

Symbol	Parameter	Condition	Min.	Unit
HBM	Human Body Model (HBM)	JESD22-A114-B Level 2, EC61340-3-1: 2002 Level 2, ESD-STM5.1-2001 Level 2, MIL-STD-883E 3015.7 Level 2	3	kV
CDM	Charged Device Model (CDM)	JESD22-C101-C Level III, IEC61340-3-3 Level C4, ESD-STM5.3.1-1999 Level C4	2	kV

Notes:

1. Device-use-level ESD tests are conducted at the connector pins.
2. External ESD suppressor ASIP protects the amplifier outputs. Suppressor is between amplifier and connector; 15Ω serial resistance + 5nF capacitor and Zener diodes (14V breakdown voltage) connected to the ground. In addition, there is a ferrite bead in series between the suppressor and the connector.
3. The air discharge test can be ignored if the contact discharge test range is increased to the same voltages as air discharge (contact discharge is more stable and repeatable test than air discharge).

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
T_A	Operating Temperature Range	-40	+85	°C
V_{BATT}	Supply Voltage Range	2.80	5.25	V

Electrical Characteristics

Unless otherwise noted: HPA uses stereo single-ended inputs, SPA uses differential input, unused inputs AC are grounded, f_{IN} = 1KHz, AGC off, PGAINxx = 0dB, HPxVOL = 0dB, PRESENTGAIN = 6dB, ERC = 1, SSMT = 000, SHDNB = 1, SDB = 1.8V, SDA and SCL pull-up voltage = 1.8V, Z_{SPK} = 8Ω+68μH, R_{HP} = 32Ω, speaker amplifier and headphone amplifier on. Typical values are at V_{BATT} = 3.7V, T_A = 25°C. Minimum and maximum values are at V_{BATT} = 2.8V to 5.25V, T_A = -40°C to 85°C.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
I_{DD}	Quiescent Supply Current (Z_{SPK} = Open)	Headphone Amplifiers Enabled, Speaker Amplifier Disabled, DIFFIN43=1			3.5		mA
		Headphone Amplifiers Disabled, Speaker Amplifier Enabled, DIFFIN21=1			4.7		
		Headphone and Speaker Amplifiers Enabled			6.2		
I_{SD}	Shutdown Current	SHDNB = 0, SDB = 1.8V			2.2		μA
		SHDNB = 1, SDB = GND			2.2		
t_{ON}	Turn-On Time	Time from Shutdown to Full Speaker and Headphone Operation, ZCD and Ramps Disabled			1.25		ms
R_{IN}	Input Resistance	PGAINxx = 0dB			21.0		KΩ
		PGAINxx = 12dB			8.5		
	Maximum Input Signal Swing (V_{BATT} = 2.8V to 5.25V, Single-Ended Input)	PGAINxx = 0dB			2.300		V_{pk-pk}
		PGAINxx = 12dB			0.575		
Analog Bypass Switch							
R_{ON}	On Resistance	$I_{BYPOUTx}$ = 20mA, BYPx = 0V and V_{BATT}, BYPEN = 1	T_A = 25°C			1	Ω
THD	Total Harmonic Distortion	V_{DIF} = $2V_{PP}$, V_{CM}= V_{BATT}/2, f = 1kHz, BYPEN = 1, Load = 8Ω	Series Resistance is 10Ω per Switch		0.05	0.25	%
			No Series Resistors		0.10		
I_{OFF}	Off Isolation	BYPEN = 0, 10KHz $1V_{RMS}$ Sine Wave Applied Across BYPOUT1 and BYPOUT2, BYPIN1 and BYPIN2 to GND = 50Ω			94		dB

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Electrical Characteristics *(Continued)*

Unless otherwise noted: HPA uses stereo single-ended inputs, SPA uses differential input, unused inputs AC are grounded, f_{IN} = 1KHz, AGC off, PGAINxx = 0dB, HPxVOL = 0dB, PRESENTGAIN = 6dB, ERC = 1, SSMT = 000, SHDNB = 1, SDB = 1.8V, SDA and SCL pull-up voltage = 1.8V, Z_{SPK} = 8Ω+68μH, R_{HP} = 32Ω, speaker amplifier and headphone amplifier on. Typical values are at V_{BATT} = 3.7V, T_A = 25°C. Minimum and maximum values are at V_{BATT} = 2.80V to 5.25V, T_A = -40°C to 85°C.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
Speaker Amplifier							
V_{OS}	Output Offset Voltage	PRESENTGAIN = Mute			±0.5		mV
		PRESENTGAIN = 6dB			±2.5		
K_{CP}	Click-and-Pop Level	Peak Voltage, A-Weighted, 32 Samples per Second, PRESENTGAIN = Mute, Inputs AC Grounded	Into Shutdown		-70		dBV
			Out of Shutdown		-70		
PSRR	Power-Supply Rejection Ratio	Inputs AC Grounded	V_{BATT} = 2.8V to 5.25V		74		dB
			f = 217Hz, 100mV_{PP} Ripple		77		
			f = 1kHz, 100mV_{PP} Ripple		75		
P_{OUT}	Output Power	THD+N < 1%, ERC Disabled, SSMT = 100, V_{BATT} = 4.2V			970		mW
		THD+N < 10%, ERC Disabled, SSMT = 100, V_{BATT} = 4.2V			1200		
		THD+N < 10%, ERC Disabled, SSMT = 100, V_{BATT} = 3.7V			930		
		THD+N < 10%, ERC Enabled, SSMT = 000, V_{BATT} = 3.7V			945		
		THD+N < 1%, ERC Enabled, SSMT = 000	V_{BATT} = 4.2V	930	975		
			V_{BATT} = 3.7V		750		
THD+N	Total Harmonic Distortion Plus Noise	P_{OUT} = 350mW			0.030	0.075	%
SNR	Signal-to-Noise Ratio	A-Weighted, P_{OUT} = 720mW, Headphone Amplifiers Off	DIFFINxx = 0 (Single-Ended)		97		dB
			DIFFINxx = 1 (Differential)	90	97		
		A-Weighted, P_{OUT} = 720mW, Headphone Amplifiers On	DIFFINxx = 0 (Single-Ended)		97		
			DIFFINxx = 1 (Differential)		97		
V_n	Output Noise	A-Weighted, Headphone Amps Off, DIFFINxx = 0, Inputs AC Grounded			32		μV_{RMS}
	Output Frequency	Spread Spectrum, SSMT = 000			330		KHz
		Fixed Frequency, SSMT = 100			330		
I_{OUT}	Output Current Limit				1.3		A
	Efficiency	P_{OUT} = 720mW, f = 1kHz			90		%
	Mute Attenuation				100		dB

Continued on the following page…

Electrical Characteristics *(Continued)*

Unless otherwise noted: HPA uses stereo single-ended inputs, SPA uses differential input, unused inputs AC are grounded, f_{IN} = 1KHz, AGC off, PGAINxx = 0dB, HPxVOL = 0dB, PRESENTGAIN = 6dB, ERC = 1, SSMT = 000, SHDNB = 1, SDB = 1.8V, SDA and SCL pull-up voltage = 1.8V, Z_{SPK} = 8Ω+68μH, R_{HP} = 32Ω, speaker amplifier and headphone amplifier on. Typical values are at V_{BATT} = 3.7V, T_A = 25°C. Minimum and maximum values are at V_{BATT} = 2.80V to 5.25V, T_A = -40°C to 85°C.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
Headphone Amplifiers							
I_{VBATT}	Supply Current	IN1 and IN2 On, IN3 and IN4 Off, DIFFIN43=1, Speaker Amplifier Off	P_{OUT} = 2x50μW into 32Ω		4.4		mA
			P_{OUT} = 2x250μW into 32Ω		5.8		
			P_{OUT} = 2x500μW into 32Ω		6.8		
V_{OS}	Output Offset Voltage	HPxVOL = Mute			±0.15		mV
K_{CP}	Click-and-Pop Level	Peak Voltage, A-Weighted, 32 Samples per Second, HPxVOL = Mute, Inputs AC Grounded	Into Shutdown		-70		dBV
			Out of Shutdown		-70		
PSRR	Power-Supply Rejection Ratio	Inputs AC Grounded	V_{BATT} = 2.8V to 5.25V		95		dB
			f = 217Hz, V_{RIPPLE} = 200mV_{PP}		95		
			f = 1KHz, V_{RIPPLE} = 200mV_{PP}		95		
P_{OUT}	Output Power	THD+N < 1%	R_{HP} = 16Ω		39		mW
			R_{HP} = 32Ω HPxV_{OL} = 4dB	27	31		
		THD+N < 10%	R_{HP} = 32Ω HPxV_{OL} = 6dB		41		
THD+N	Total Harmonic Distortion Plus Noise	R_{HP} = 32Ω, P_{OUT} = 20mW			0.010	0.075	%
		R_{HP} = 16Ω, P_{OUT} = 10mW			0.020		
SNR	Signal-to-Noise Ratio	A-Weighted, P_{OUT} = 32mW, Speaker Amplifier Off HPxVOL = 4dB	DIFFINxx = 0 (Single-Ended)	95	100		dB
			DIFFINxx = 1 (Differential)		100		
		A-Weighted, P_{OUT} = 32mW, Speaker Amplifier On HPxVOL = 4dB	DIFFINxx = 0 (Single-Ended)		100		
			DIFFINxx = 1 (Differential)		103		
	Output Noise	A-Weighted, Speaker Amplifier Off, DIFFINxx = 0			6.5		μV_{RMS}
C_L	Capacitive Drive				100		pF
X_{TALK}	Crosstalk	HPL to HPR, HPR to HPL, P_O = 15mW			-85		dB
f_P	Charge-Pump Frequency				1.3		MHz
A_V	Headphone Gain Accuracy	Across All Gain Stages			±0.4		dB
	Channel-to-Channel Gain Tracking	HPL to HPR, HPxVOL = 0dB			±0.3		%
	Channel-to-Channel Gain Tracking	HPL to HPR Across Entire Pre-Amplifier and Volume Range			±1		%
	Mute Attenuation				100		dB

I²C DC Electrical Characteristics

Unless otherwise noted, V_{BATT} = 2.80V to 5.25V and T_A = -40°C to 85°C.

Symbol	Parameter	Conditions	Fast Mode (400kHz)		
			Min.	Max.	Unit
V_{IL}	Low-Level Input Voltage	V_{BATT} 2.80V to 5.25V	-0.3	0.6	V
V_{IH}	High-Level Input Voltage	V_{BATT} 2.80V to 5.25V	1.3		V
V_{OL}	Low-level Output Voltage	at 3mA Sink Current (Open-Drain or Open-Collector)	0	0.4	V
I_{IH}	High-Level Input Current	Each I/O Pin, Input Voltage = V_{BATT}	-1	1	µA
I_{IL}	Low-Level Input Current	Each I/O Pin, Input Voltage = 0V	-1	1	µA

I²C AC Electrical Characteristics

Unless otherwise noted, V_{BATT} = 2.80V to 5.25V and T_A = -40°C to 85°C.

Symbol	Parameter	Fast Mode		
		Min.	Max.	Unit
f_{SCL}	SCL Clock Frequency	0	400	kHz
$t_{HD;STA}$	Hold Time (Repeated) START Condition	0.6		µs
t_{LOW}	LOW Period of SCL Clock	1.3		µs
t_{HIGH}	HIGH Period of SCL Clock	0.6		µs
$t_{SU;STA}$	Set-up Time for Repeated START Condition	0.6		µs
$t_{HD;DAT}$	Data Hold Time	0	0.9	µs
$t_{SU;DAT}$	Data Set-up Time[4]	100		ns
t_r	Rise Time of SDA and SCL Signals[5]	$20+0.1C_b$	300	ns
t_f	Fall Time of SDA and SCL Signals[5]	$20+0.1C_b$	300	ns
$t_{SU;STO}$	Set-up Time for STOP Condition	0.6		µs
t_{BUF}	Bus Free Time between STOP and START Conditions	1.3		µs
t_{SP}	Pulse Width of Spikes that Must Be Suppressed by the Input Filter	0	50	ns

Notes:

4. A fast-mode I²C-Bus® device can be used in a standard-mode system, but the requirement $t_{SU;DAT} \geq 250ns$ must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r\_max} + t_{SU;DAT}$ = 1000 + 250 = 1250ns (according to the standard-mode I²C bus specification) before the SCL line is released.
5. C_b equals the total capacitance of one bus line in pf. If mixed with high-speed mode devices, faster fall times are allowed according to the I²C specification.

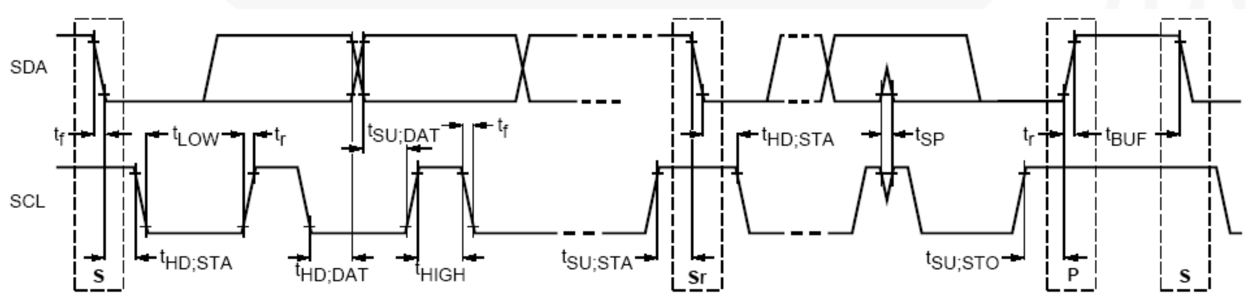

Figure 3. Definition of Timing for Full-Speed Mode Devices on the I²C-Bus®

Typical Performance Characteristics

System

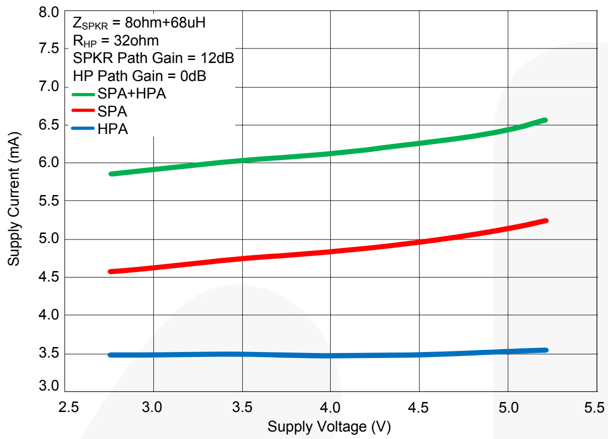

Figure 4. Quiescent Supply Current vs. Supply Voltage

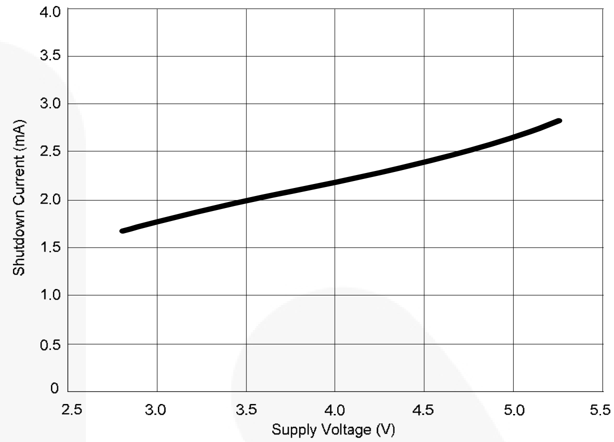

Figure 5. Hardware and Software Shutdown Current vs. Supply Voltage

Speaker Amplifier

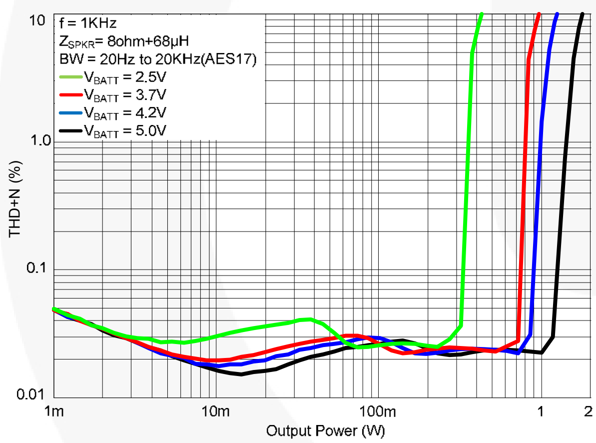

Figure 6. THD+N vs. Output Power

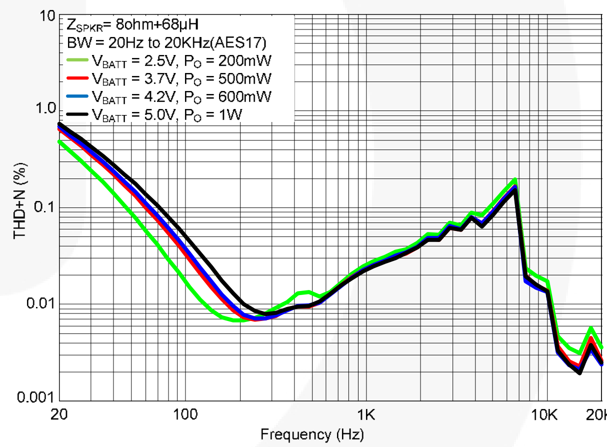

Figure 7. THD+N vs. Frequency

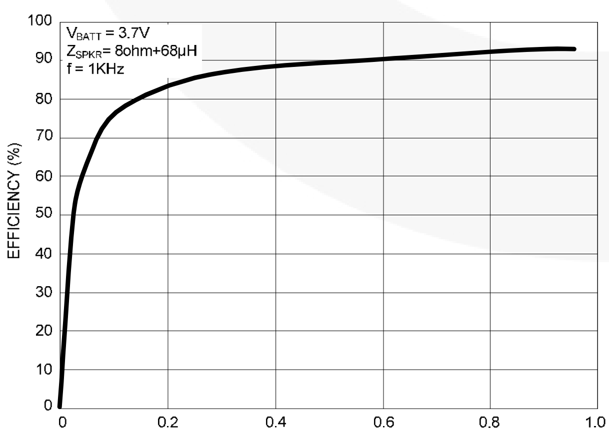

Figure 8. Efficiency vs. Output Power

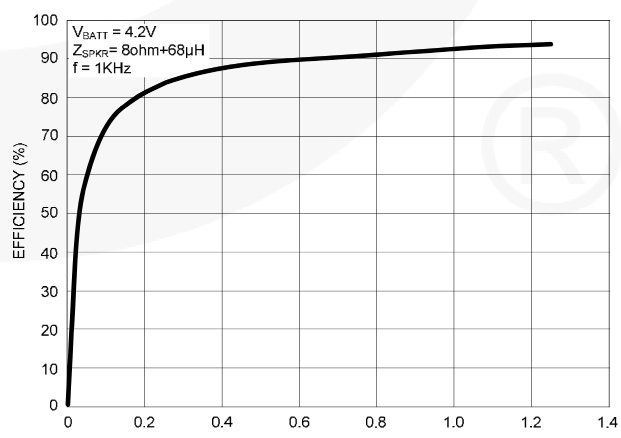

Figure 9. Efficiency vs. Output Power

Typical Performance Characteristics

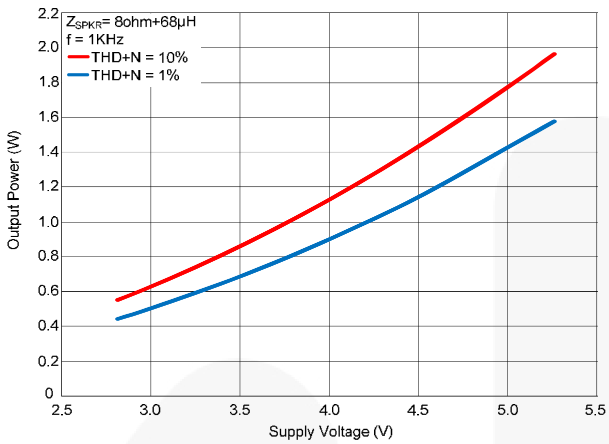

Figure 10. Output Power vs. Supply Voltage

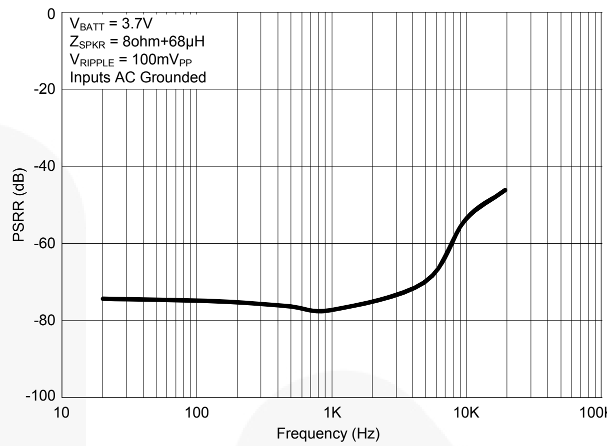

Figure 11. PSRR vs. Frequency

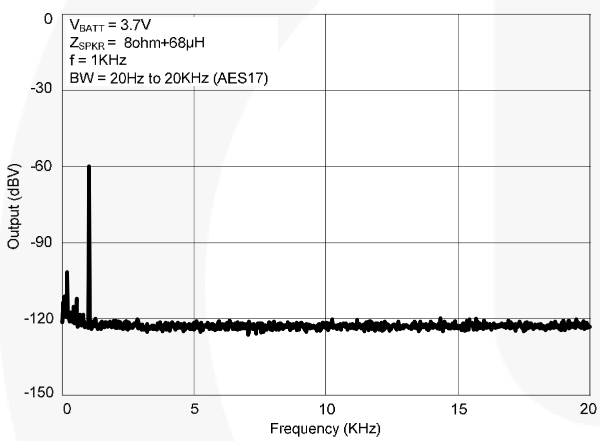

Figure 12. Output vs. Frequency

Headphone Amplifier

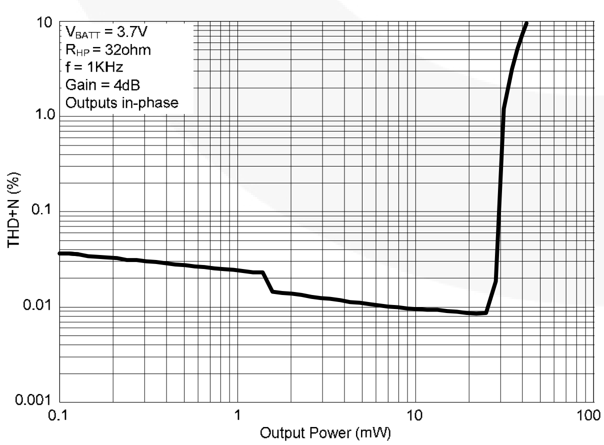

Figure 13. THD+N vs. Output Power

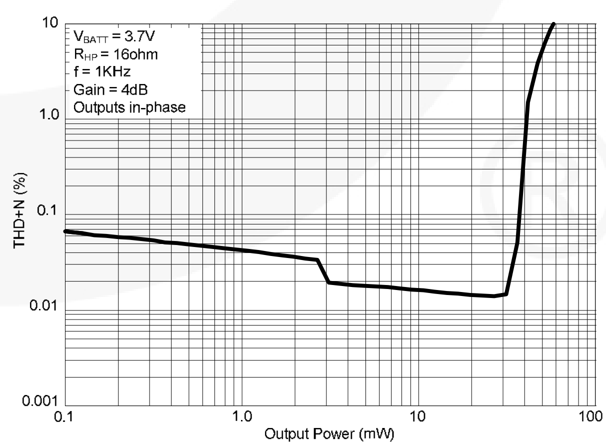

Figure 14. THD+N vs. Output Power

Typical Performance Characteristics

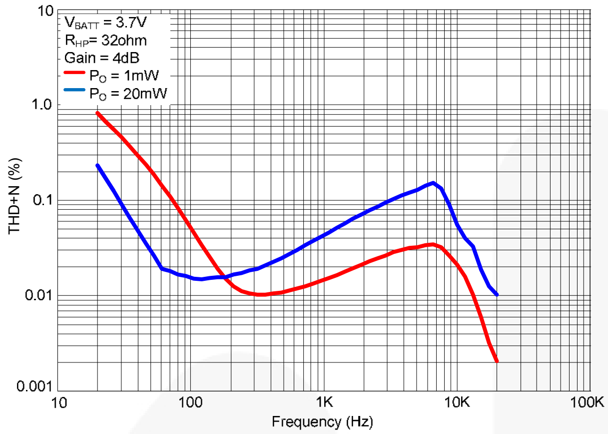

Figure 15. THD+N vs. Frequency

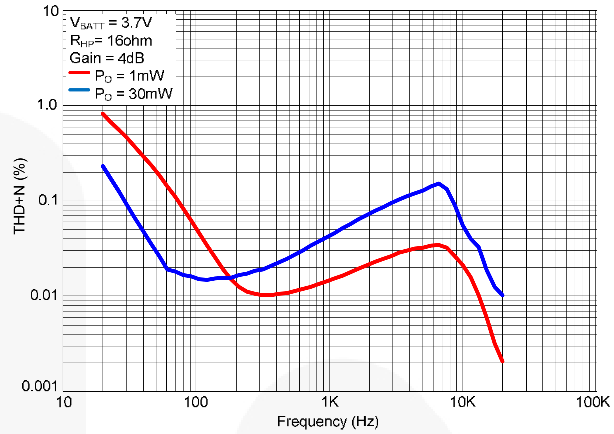

Figure 16. THD+N vs. Frequency

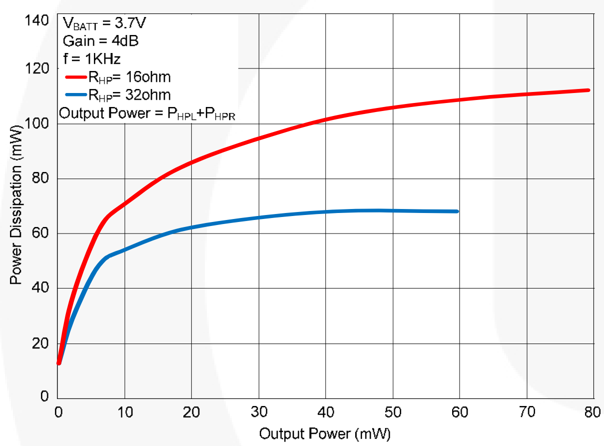

Figure 17. Power Dissipation vs. Total Output Power

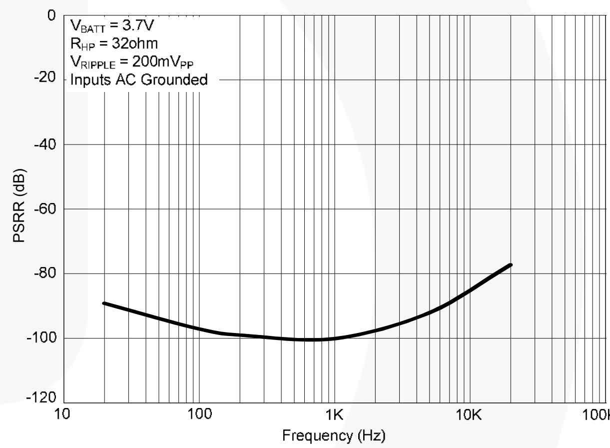

Figure 18. PSRR vs. Frequency

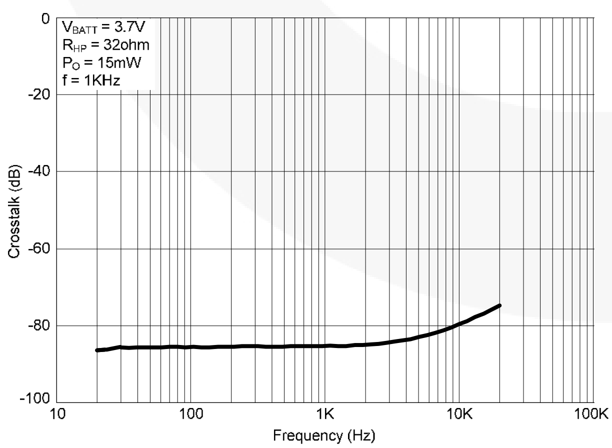

Figure 19. Crosstalk vs. Frequency

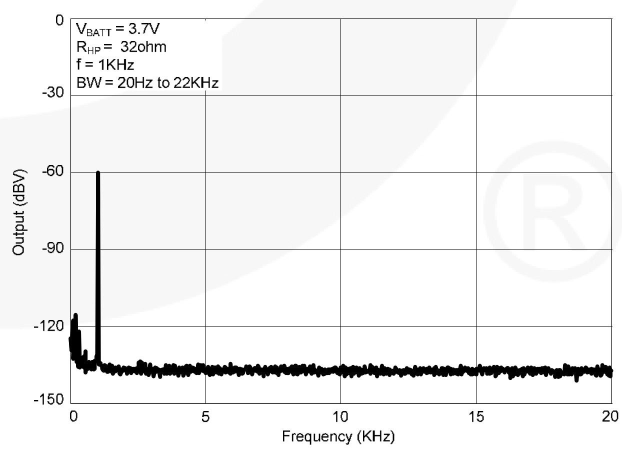

Figure 20. Output vs. Frequency

Functional Description

Shutdown Mode

When SHDNB bit is set to 0 or the SDB pin is grounded, the FAB2200 enters low-power Shutdown Mode.

While SHDNB=0 and SDB is HIGH, I^2C communication is available. I^2C values are preserved. Values are not reset on exiting Shutdown Mode.

If the SDB pin is grounded, I^2C communication is unavailable. I^2C values are not preserved. Values are reset to default values after SDB goes HIGH.

Inputs During Shutdown

To achieve low supply current during shutdown, all inputs must be at DC levels (except the BYPASS pins). Audio inputs must be AC grounded. V_{BATT} must be within recommended operating conditions. I^2C pins must be grounded or pulled HIGH with no toggling. If AC is presented to the inputs during shutdown, standby current may increase slightly, but there are no other negative effects.

Thermal Shutdown

If the junction temperature of the device exceeds the thermal shutdown threshold (s*ee Electrical Characteristics table*), the device protects itself by shutting down. The device remains shut down until the junction temperature falls below the thermal shutdown hysteresis.

The I^2C port remains functional and the OVRTEMP bit is set to O. This bit remains set until it is read. If the device is still in thermal shutdown when the bit is read, it remains set to 1. Otherwise, the bit is cleared to 0.

Over-Current Shutdown

If the output current limit of either amplifier is exceeded (*see the Electrical Characteristics table*), the amplifier in question shuts down for approximately one second. After one second, the amplifier is re-enabled. If the amplifier output current exceeds the limit again, the cycle repeats.

During current-limit shutdown, the I^2C port remains functional. If the current-limit shutdown was caused by the speaker amplifier, the OVRCURSP bit is set to 1. This bit remains set until it is read. If the speaker amplifier is still in current-limit shutdown when the bit is read, it remains set to 1. Otherwise, the bit is cleared to 0.

Signal Path

The input channels have a pre-amplifier stage that can be set from 0dB to 21dB of gain. The headphone amplifiers have separate volume controls that range from -53dB to 6dB. The speaker amplifier has a volume control that ranges from -25dB to 6dB. In addition, the speaker amplifier has a fixed gain of 6dB.

A variety of combinations of these signals can be routed to the headphone amplifiers or the speaker amplifier (*see Table 1*). For example, to connect the left headphone amplifier channel to IN3 and IN1, set the SELHPL3 and SELHPL1 bits to 1. SELHPL4 and SELHPL2 should be set to 0.

The DIFFIN43 and DIFFIN21 bits configure the inputs as differential pairs. When configured as differential, the even-numbered selection bit should be 1 and the odd-numbered selection bit should be 0. For example, if channels 4 and 3 are a differential pair that should be connected to the speaker amplifier, DIFFIN43 and SELSPA4 should be set to 1. SELSPA3, SELSPA2, and SELSPA1 should be set to 0.

Amplifier channels that have no inputs selected should be muted (HPxVOL = 00000 or STARTGAIN = 000000). If an amplifier channel has no input selection bits set to 1, the amplifier channel is turned off. When the speaker amplifier is turned off, the SPKRP and SPKRN outputs stop switching.

Unused audio input pins must be AC grounded.

An integrated Dual-Pole Single-Throw (DPST) analog bypass switch can be used to route system audio signals. For example, baseband audio can be routed to the speaker by connecting the BYPOUTx pins to the SPKRx pins. Baseband audio outputs would then be connected to the BYPINx pins through optional external resistors if the baseband device expects a higher impedance than the existing speaker.

Gain for the headphone amplifier signal path is defined by PGAINxx + HPxVOL.

Gain for the speaker amplifier signal path is defined by PGAINxx + PRESENTGAIN + 6dB.

Internal signal amplitude should not exceed $2.3V_{PP}$. Extra caution should be taken when mixing signals. For example, if IN1 is mixed with IN3, the maximum peak to peak amplitude of IN1 plus the maximum peak to peak amplitude of IN3 should not exceed $2.3V_{PP}$.

Table 1. Input Channel Selection

DIFFIN43	DIFFIN21	SELxxx4	SELxxx3	SELxxx2	SELxxx1	xxx Amplifier Input
X	X	0	0	0	0	xxx Amplifier Channel Off
0	0	0	0	0	1	IN1
0	0	0	0	1	0	IN2
0	0	0	0	1	1	IN2 + IN1
0	0	0	1	0	0	IN3
0	0	0	1	0	1	IN3 + IN1
0	0	0	1	1	0	IN3 + IN2
0	0	0	1	1	1	IN3 + IN2 + IN1
0	0	1	0	0	0	IN4
0	0	1	0	0	1	IN4 + IN1
0	0	1	0	1	0	IN4 + IN2
0	0	1	0	1	1	IN4 + IN2 + IN1
0	0	1	1	0	0	IN4 + IN3
0	0	1	1	0	1	IN4 + IN3 + IN1
0	0	1	1	1	0	IN4 + IN3 + IN2
0	0	1	1	1	1	IN4 + IN3 + IN2 + IN1
0	1	0	0	0	0	xxx Amplifier Channel Off
0	1	0	0	0	1	Not Supported
0	1	0	0	1	0	IN2 - IN1
0	1	0	0	1	1	Not Supported
0	1	0	1	0	0	IN3
0	1	0	1	0	1	Not Supported
0	1	0	1	1	0	IN3 + (IN2 - IN1)
0	1	0	1	1	1	Not Supported
0	1	1	0	0	0	IN4
0	1	1	0	0	1	Not Supported
0	1	1	0	1	0	IN4 + (IN2 - IN1)
0	1	1	0	1	1	Not Supported
0	1	1	1	0	0	IN4 + IN3
0	1	1	1	0	1	Not Supported
0	1	1	1	1	0	IN4 + IN3 + (IN2 - IN1)
0	1	1	1	1	1	Not Supported
1	0	0	0	0	0	xxx Amplifier Channel Off
1	0	0	0	0	1	IN1
1	0	0	0	1	0	IN2
1	0	0	0	1	1	IN2 + IN1
1	0	0	1	0	0	Not Supported
1	0	0	1	0	1	Not Supported
1	0	0	1	1	0	Not Supported
1	0	0	1	1	1	Not Supported
1	0	1	0	0	0	IN4 - IN3
1	0	1	0	0	1	(IN4 - IN3) + IN1
1	0	1	0	1	0	(IN4 - IN3) + IN2
1	0	1	0	1	1	(IN4 - IN3) + IN2 + IN1
1	0	1	1	0	0	Not Supported
1	0	1	1	0	1	Not Supported
1	0	1	1	1	0	Not Supported
1	0	1	1	1	1	Not Supported
1	1	0	0	0	0	xxx Amplifier Channel Off
1	1	0	0	0	1	Not Supported
1	1	0	0	1	0	IN2 - IN1
1	1	0	0	1	1	Not Supported
1	1	0	1	0	0	Not Supported
1	1	0	1	0	1	Not Supported
1	1	0	1	1	0	Not Supported
1	1	0	1	1	1	Not Supported
1	1	1	0	0	0	IN4 - IN3
1	1	1	0	0	1	Not Supported
1	1	1	0	1	0	(IN4 - IN3) + (IN2 - IN1)
1	1	1	0	1	1	Not Supported
1	1	1	1	0	0	Not Supported
1	1	1	1	0	1	Not Supported
1	1	1	1	1	0	Not Supported
1	1	1	1	1	1	Not Supported

Class-G Headphone Amplifier with Capacitor Free Outputs

The FAB2200 includes a regulated charge pump that derives CPV_{DD} and CPV_{SS} (the headphone amplifier power supplies) from VBATT. When the headphone output amplitude is low, the CPV_{DD} is 1.3V and CPV_{SS} is -1.3V. When needed, CPV_{DD} and CPV_{SS} dynamically increase to 1.8V and -1.8V, respectively, to allow for higher output amplitudes. The combination of an efficient regulated charge pump and class-G operation allows low headphone amplifier power dissipation, resulting in longer battery run time.

The negative CPV_{SS} rail allows the headphone amplifier output to be centered at 0V and eliminates the need for output DC blocking capacitors.

The FAB2200 headphone outputs can be placed in High-Impedance Mode by setting the HIZx bits to 1 (*see Table 2*). This can be useful if the system's headphone jack is shared with other devices. For proper high-impedance operation, the device must not be in Shutdown Mode. Voltages on HPL and HPR must not exceed ±1.8V.

Table 2. Headphone Amplifier Output Impedance, HIZx=1

Output Impedance (Ω)	Frequency (KHz)
11800	40
760	6000
470	13000

Headphone Volume Control Ramp and Zero-Crossing Detection

The HPRAMP, HPRAMPSPEED, and HPZCD bits control the headphone amplifiers' volume controls when $HPxV_{OL}$ is changed.

Table 3. Headphone Volume Change Behavior

HPRAMP	HPZCD	Behavior When HPxVOL Changes
0	0	Volume changes immediately.
0	1	For each channel, wait until a zero crossing occurs in the input before changing volume. If a zero crossing does not occur within HPRAMPSPEED, volume is forced to the new setting.
1	0	Volume is ramped to the new setting at a rate of HPRAMPSPEED per step.
1	1	Volume is changed by one step when a zero crossing occurs. If a zero crossing does not occur within HPRAMPSPEED, a step is forced. Only the first zero crossing within HPRAMPSPEED triggers a volume change – volume does not change again until the next HPRAMPSPEED.

Table 4. Headphone Volume Change Timing

HPRAMPSPEED[1:0]	Ramp and ZCD Time Between Steps (ms)
00	0.25
01	2.00
10	16.00
11	128.00

Programmable Headphone Amplifier Noise Gate

The headphone noise gate automatically mutes the headphone amplifier when its input amplitudes are low to reduce noise during inactivity. This function is not recommended for music playback, but is effective for speech. The amplitude is measured after input pre-amplifiers and before the headphone amplifier volume controls. The headphone noise gate threshold level is set by the HPNGTHRESH register. The amplitudes of both channels must be less than the noise gate threshold for a time determined by the HPNGTIME register. When the noise gate mutes the amplifier, the HPNGTRIP bit is set to 1.

If either channel's input amplitude goes above the headphone noise gate threshold, both amplifiers are un-muted and the HPNGTRIP bit is set to 0. The amplifiers are returned to the former HPxVOL values.

If either channel is in High-Impedance Mode (HIZx=1), all inputs to that headphone should be deselected (SELHPxx=0) so the noise gate ignores the HIZ channel.

If the HPNGZRA bit is set to 0, the headphone noise gate attack (mute) function occurs immediately rather than waiting for zero-crossing detection or ramping. If the HPNGZRA bit is set to 1, the headphone noise gate attack function obeys headphone zero-crossing detection and ramp settings.

If the HPNGZRR bit is set to 0, the headphone noise gate release (un-mute) function occurs immediately rather than waiting for zero-crossing detection or ramping. If the HPNGZRR bit is set to 1, the headphone noise gate release (un-mute) function obeys headphone zero crossing detection and ramp settings.

Table 5. Headphone Noise Gate Threshold Voltage

HPNGTHRESH [2:0]	Noise Gate Threshold (mV_{pk})
000	Headphone Noise Gate Disabled
001	2.8
010	5.7
011	11.3
100	22.6
101	45.3
110	90.5
111	181.0

Table 7. Headphone Noise Gate Timing

HPNGTIME [2:0]	Time (ms)
000	10
001	20
010	40
011	80
100	160
101	320
110	640
111	Reserved

Certain combinations of HPRAMP, HPZCD, HPNGZRA, and HPNGZRR are valid as shown in Table 8. Combinations not listed may produce unpredictable results (X = don't care).

Table 8. Valid Headphone Amplifier Ramp / Zero Crossing / Noise Gate Combinations

HPRAMP	HPZCD	HPNGZRA	HPNGZRR
0	0	X	X
X	X	1	1
1	X	1	0

Class-D Speaker Amplifier

The class-D amplifier achieves greater than 90% efficiency.

Programmable spread spectrum and edge rate control minimize electromagnetic interference (EMI). Rise and fall times are limited to 20ns per transition at all power levels.

Programmable Automatic Gain Control (AGC)

The speaker amplifier's AGC can be used to limit output amplitude and reduce clipping as supply voltage varies. The AGC allows high-volume settings while minimizing distortion and protecting the speaker element.

AGC works by comparing the threshold voltage against a proposed output amplitude (the signal's amplitude after all gain stages, before the PWM modulator). If the threshold is exceeded, gain is dynamically reduced until the output voltage level no longer exceeds the threshold or the minimum gain setting. When the output voltage level no longer exceeds the threshold, gain is slowly increased until either the output voltage level exceeds the threshold again or the starting gain is reached.

AGC settings should not be changed while the speaker amplifier is on. Before making changes to THMAX, THVBATT, AGCATTACK, AGCRELEASE, or AGCMIN; the speaker amplifier should be turned off by clearing all SELSPAn bits to 0 or clearing SHDNB to 0.

AGC Threshold

The AGC threshold can be thought of as a target for the maximum output amplitude. It is defined by the THMAX and THVBATT registers.

THMAX defines the maximum threshold value regardless of V_{BATT} supply voltage. This is useful for protecting speakers from high amplitudes. Table 9 shows the THMAX threshold settings as well as the corresponding maximum RMS power (assuming a 1KHz sine wave into an 8Ω load).

Table 9. THMAX Threshold

THMAX [3:0]	Maximum Output Threshold (V_{pk})	Maximum Power with Sine Wave and 8Ω Load (mW)	THMAX [3:0]	Maximum Output Threshold (V_{pk})	Maximum Power with Sine Wave and 8Ω Load (mW)
0000	THMAX Threshold Disabled		1000	3.6	810.0
0001	2.2	302.5	1001	3.8	902.5
0010	2.4	360.0	1010	4.0	1000.0
0011	2.6	422.5	1011	4.2	1102.5
0100	2.8	490.0	1100	4.4	1210.0
0101	3.0	562.5	1101	4.6	1322.5
0110	3.2	640.0	1110	4.8	1440.0
0111	3.4	722.5	1111	5.0	1562.5

THVBATT limits the amount of clipping allowed by the AGC. As V_{BATT} falls, the maximum output amplitude falls. THVBATT defines the threshold as a fraction of the V_{BATT} supply voltage. When the fraction is less than 1, the AGC attempts to adjust gain to prevent clipping. For values greater than 1, some clipping is allowed before the AGC reduces gain (*see Table 10*).

Table 10. THVBATT Threshold

THVBATT [4:0]	V_{BATT} Fraction (V/V)	THD with 1KHz Sine Wave (%) (V_{BATT}=3.7V, 8Ω Load)	THVBATT [4:0]	V_{BATT} Fraction (V/V)	THD with 1KHz Sine Wave (%) (V_{BATT}=3.7V, 8Ω Load)
0000	THVBATT Threshold Disabled		1000	1.25	13.0
0001	0.90	1.0	1001	1.30	14.4
0010	0.95	3.0	1010	1.35	15.6
0011	1.00	4.9	1011	1.40	16.7
0100	1.05	6.7	1100	1.45	17.7
0101	1.10	8.5	1101	1.50	18.7
0110	1.15	10.0	1110	1.55	19.6
0111	1.20	11.6	1111	1.60	20.5

Ultimately, the AGC threshold is whichever voltage is lower between THVBATT and THMAX. For example, if THMAX = 0111, THVBATT = 0001, and V_{BATT} = 4.2V, the AGC threshold is 3.4V as defined by THMAX. If V_{BATT} falls to 3.6V, the AGC threshold falls to 3.24V as defined by THVBATT (*see Figure 21).* If THVBATT and THMAX are both set to 0, the AGC is disabled.

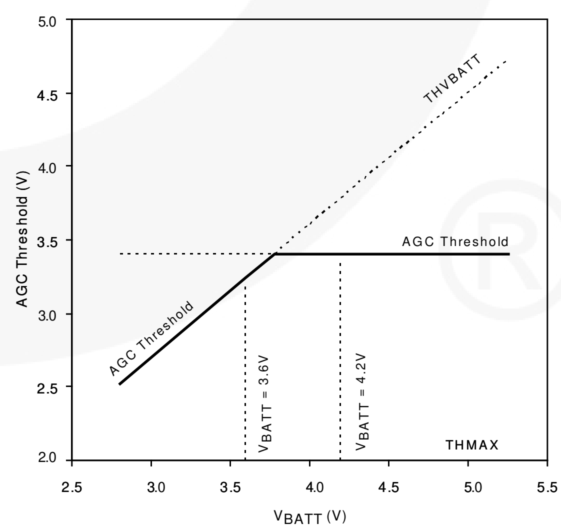

Figure 21. AGC Threshold, THMAX = 0111, THVBATT = 0001

Starting Gain

Starting gain is the amount of speaker gain applied when the AGC is not active. It can also be thought of as maximum gain when the AGC is active. Starting gain is controlled by the STARTGAIN register (*see Table 11).*

Table 11. Speaker Gain Values

Gain Register [5:0]	Gain (dB)	Gain Register [5:0]	Gain (dB)
000000	Mute	100000	-9.5
000001	-25.0	100001	-9.0
000010	-24.5	100010	-8.5
000011	-24.0	100011	-8.0
000100	-23.5	100100	-7.5
000101	-23.0	100101	-7.0
000110	-22.5	100110	-6.5
000111	-22.0	100111	-6.0
001000	-21.5	101000	-5.5
001001	-21.0	101001	-5.0
001010	-20.5	101010	-4.5
001011	-20.0	101011	-4.0
001100	-19.5	101100	-3.5
001101	-19.0	101101	-3.0
001110	-18.5	101110	-2.5
001111	-18.0	101111	-2.0
010000	-17.5	110000	-1.5
010001	-17.0	110001	-1.0
010010	-16.5	110010	-0.5
010011	-16.0	110011	0
010100	-15.5	110100	0.5
010101	-15.0	110101	1.0
010110	-14.5	110110	1.5
010111	-14.0	110111	2.0
011000	-13.5	111000	2.5
011001	-13.0	111001	3.0
011010	-12.5	111010	3.5
011011	-12.0	111011	4.0
011100	-11.5	111100	4.5
011101	-11.0	111101	5.0
011110	-10.5	111110	5.5
011111	-10.0	111111	6.0

AGC Attack

AGC attack occurs when the AGC determines that, after applying present gain, the output signal amplitude would be too high and gain should be stepped down by 1dB. The AGC checks an approximation of the amplitude of the output signal that includes present gain, but excludes clipping that may occur in the final output stage. All of the following conditions must be true to trigger an AGC attack:

- The amplitude is above the AGC threshold, AND
- Present gain is above the minimum gain point, AND
- Attack speed is not exceeded.

The minimum gain is determined by the AGCMIN register. The rate of gain reduction is determined by the AGCATTACK register.

AGC Release

When the output signal is below the AGC threshold, gain is stepped up by 1dB. The rate of gain increase is determined by the AGCRELEASE registers. Gain is increased until it reaches the starting gain or an AGC attack is triggered again.

Table 12. AGC Attack Speed

AGCATTACK [2:0]	AGC Attack Speed (µs/Step)	AGCATTACK [2:0]	AGC Attack Speed (µs/Step)
000	12.5	100	200
001	25.0	101	400
010	50.0	110	800
011	100.0	111	1600

Table 13. AGC Release Speed

AGCRELEASE [2:0]	AGC Release Speed (ms/Step)	AGCRELEASE [2:0]	AGC Release Speed (ms/Step)
000	12.5	100	200
001	25.0	101	400
010	50.0	110	800
011	100.0	111	1600

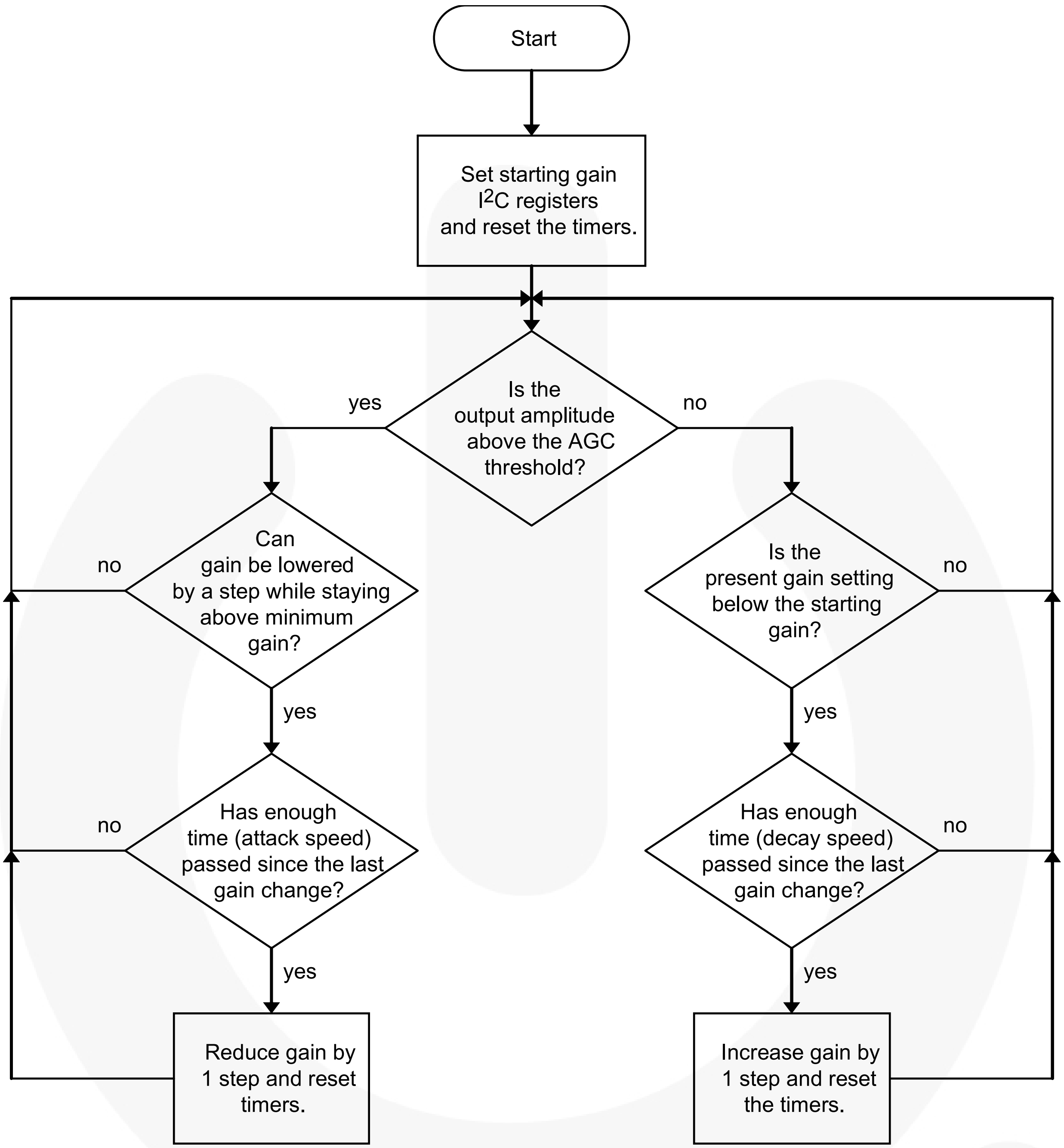

Figure 22. AGC Flow Chart

Programmable Speaker Amplifier Noise Gate

The speaker noise gate automatically mutes the speaker amplifier when its input amplitude is low to reduce noise during inactivity. This function is not recommended for music playback, but is effective for speech. The amplitude is measured after input pre-amplifiers, but before the speaker amplifier's volume control. The speaker noise gate's threshold level is set by the SPNGTHRESH register. The amplitude must be less than the speaker noise gate threshold for a time determined by the SPNGTIME register. When the speaker noise gate mutes the speaker amplifier, the SPNGTRIP bit is set to 1.

If the input amplitude goes above the speaker noise gate threshold, the speaker amplifier is un-muted and the SPNGTRIP bit is set to 0. If the AGC is not enabled, the speaker amplifier is returned to its former PRESENTGAIN value. If the AGC is enabled, AGCRELEASE speed determines the new PRESENTGAIN value.

Table 14. Speaker Noise Gate Threshold Voltage

SPNGTHRESH [2:0]	Speaker Noise Gate Threshold (mVpk)
000	Speaker Noise Gate Disabled
001	2.8
010	5.7
011	11.3
100	22.6
101	45.3
110	90.5
111	181.0

Table 15. Speaker Noise Gate Timing

SPNGTIME [2:0]	Time (ms)
000	10
001	20
010	40
011	80
100	160
101	320
110	640
111	Reserved

Speaker Amplifier Gain Ramp and Zero-Crossing Detection (ZCD)

The SPRAMP, SPRAMPSPEED, and SPZCD bits control the speed at which PRESENTGAIN is changed when STARTGAIN is changed.

Table 16. Speaker Gain Change Behavior

SPRAMP	SPZCD	Behavior When STARTGAIN Is Changed
0	0	STARTGAIN changes immediately.
0	1	Wait until a zero crossing occurs in the input before changing STARTGAIN. If a zero crossing does not occur within SPRAMPSPEED, STARTGAIN is forced to the new setting.
1	0	STARTGAIN is ramped to the new setting at a rate of SPRAMPSPEED per step.
1	1	STARTGAIN is changed by one step when a zero crossing occurs. If a zero crossing does not occur within SPRAMPSPEED, a step is forced. Only the first zero crossing within SPRAMPSPEED triggers a gain change – gain does not change again until the next SPRAMPSPEED.

Table 17. Speaker Gain Change Timing

SPRAMPSPEED[1:0]	Ramp and ZCD Time Between Steps (ms)
00	0.25
01	2.00
10	16.00
11	128.00

SPRAMP, SPRAMPSPEED, and SPZCD have no effect on AGC and noise gate timing. AGC and noise gate timing have no effect on speaker amplifier gain ramp and zero-crossing detection. In the event of a conflict between these systems, PRESENTGAIN chooses the lowest gain setting. For example, SPRAMP is enabled with a slow SPRAMPSPEED and a fast AGCATTACK. The user changes STARTGAIN from 111111 to 000001. As the ramp function begins to ramp PRESENTGAIN down slowly (as defined by SPRAMPSPEED), a loud sound surpasses the AGC threshold. This forces PRESENTGAIN to react quickly (as defined by AGCATTACK). If the sound's amplitude falls below the AGC threshold before PRESENTGAIN reaches 000001, the quick gain reduction halts and the slow gain reduction resumes.

Valid combinations of SPRAMP, SPZCD, SPNGZRA, and SPNGZRR are shown in Table 18. Combinations not listed may produce unpredictable results.

Table 18. Valid Speaker Amplifier Ramp / Zero Crossing / Noise Gate Combinations

SPRAMP	SPZCD	SPNGZRA	SPNGZRR
0	0	X	X
X	X	1	1
1	X	1	0

Note:
6. X = don't care.

If the SPNGZRA bit is set to 0, the speaker noise gate attack (mute) function occurs immediately rather than waiting for zero-crossing detection or ramping. If the SPNGZRA bit is set to 1, the speaker noise gate attack function obeys speaker zero crossing detection and ramp settings.

If the SPNGZRR bit is set to 0, the speaker noise gate release (un-mute) function occurs immediately rather than waiting for zero-crossing detection or ramping. If the SPNGZRR bit is set to 1, the speaker noise gate release (un-mute) function obeys speaker zero-crossing detection and ramp settings.

I^2C Control

Writing to and reading from the FAB2200 registers is accomplished via the I^2C interface. The I^2C protocol requires that one device on the bus initiates and controls all read and write operations. This device is called the "master" device. The master device also generates the SCL signal, which is the clock signal for all other devices on the bus, called "slave" devices. The FAB2200 is a slave device. Both the master and slave devices can send and receive data on the bus.

During I^2C operations, one data bit is transmitted per clock cycle. All I^2C operations follow a repeating nine-clock-cycle pattern that consists of eight bits (one byte) of transmitted data followed by an acknowledge (ACK) or not acknowledge (NACK) from the receiving device. Note that there are no unused clock cycles during any operation – therefore, there must be no breaks in the stream of data and ACKs/NACKs during data transfers.

For most operations, I^2C protocol requires the SDA line to remain stable (unmoving) whenever SCL is HIGH;- i.e., transitions on the SDA line can only occur when SCL is LOW. The exceptions to this rule are when the master device issues a START or STOP condition. A slave device cannot issue a START or STOP condition.

START Condition: This condition occurs when the SDA line transitions from HIGH to LOW while SCL is HIGH. The master device uses this condition to indicate that a data transfer is about to begin.

STOP Condition: This condition occurs when the SDA line transitions from LOW to HIGH while SCL is HIGH. The master device uses this condition to signal the end of a data transfer.

Acknowledge and Not Acknowledge: When data is transferred to the slave device, it sends an acknowledge (ACK) after receiving every byte of data. The receiving (slave) device sends an ACK by pulling SDA LOW for one clock cycle.

When the master device is reading data from the slave device, the master sends an ACK after receiving every byte of data. Following the last byte, a master device sends a "not acknowledge" (NACK) instead of an ACK, followed by a STOP condition. A NACK is indicated by leaving SDA HIGH during the clock after the last byte.

Slave Address

Each slave device on the bus has a unique address so the master can identify which device is sending or receiving data. The FAB2200 slave address is 1001101X binary where "X" is the read/write bit. Master write operations are indicated when X=0. Master read operations are indicated when X=1.

Writing to and Reading from the FAB2200

All read and write operations must begin with a START condition generated by the master device. After the START condition, the master device must immediately send a slave address (7 bits), followed by a read/write bit. If the slave address matches the address of the FAB2200, the FAB2200 sends an ACK by pulling the SDA line LOW for one clock cycle.

Setting the Pointer

For all operations, the pointer stored in the command register must be pointing to the register that is going to be written to or read from. To change the pointer value in the Command register, the read/write bit following the address must be 0. This indicates that the master writes new information into the Command register.

After the FAB2200 sends an ACK in response to receiving the address and read/write bit, the master device must transmit an appropriate 8-bit pointer value, as explained in the I^2C Registers section. The FAB2200 sends an ACK after receiving the new pointer data.

The pointer set operation is illustrated in Figure 25 and Figure 26. Any time a pointer set is performed, it must be immediately followed by a read or write operation. The Command register retains the current pointer value between operations; therefore subsequent read operations do not require a pointer set cycle. Write operations always require the pointer be reset.

Reading

If the pointer is already pointing to the desired register, the master can read from that register by setting the read/write bit (following the slave address) to 1. After sending an ACK, FAB2200 begins transmitting data during the following clock cycle. The master should respond with a NACK, followed by a STOP condition *(see Figure 23).*

The master reads multiple bytes by responding to the data with an ACK instead of a NACK and continuing to send SCL pulses, as shown in Figure 24. The FAB2200 increments the pointer by one and sends the data from the next register. The master indicates the last data byte by responding with a NACK, followed by a STOP.

To read from a register other than the one currently indicated by the Command register, a pointer to the desired register must be set. Immediately following the pointer set, the master must perform a REPEAT START condition (*see Figure 26*), which indicates to the FAB2200 that a new operation is about to occur. If the REPEAT START condition does not occur, the FAB2200 assumes that a write is taking place and the selected register is overwritten by the upcoming data on the data bus. After the START condition, the master must again send the device address and read/write bit. This time, the read/write bit must be set to 1 to indicate a read. The rest of the read cycle is the same as described in the previous paragraphs for reading from a preset pointer location.

Writing

All writes must be preceded by a pointer set, even if the pointer is already pointing to the desired register. Immediately following the pointer set, the master must begin transmitting the data to be written. After transmitting each byte of data, the master must release the Serial Data (SDA) line for one clock cycle to allow the FAB2200 to acknowledge receiving the byte. The write operation should be terminated by a STOP condition from the master *(see Figure 25).*

As with reading, the master can write multiple bytes by continuing to send data. The FAB2200 increments the pointer by 1 and accepts data for the next register. The master indicates the last data byte by issuing a STOP.

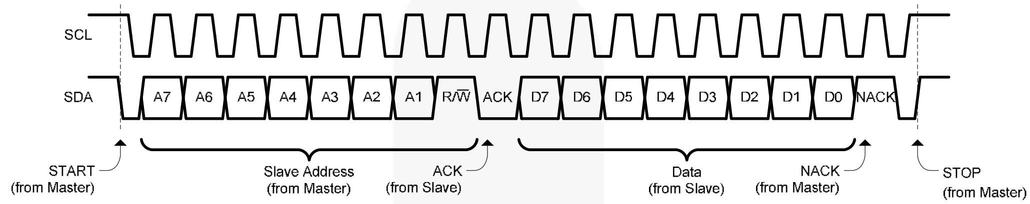

Figure 23. I^{2}C Read

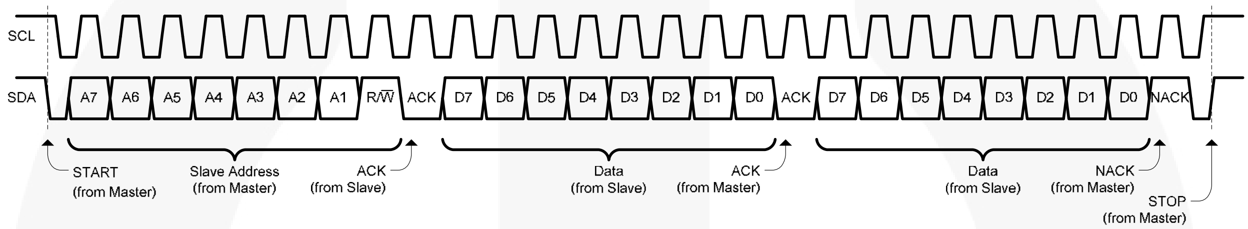

Figure 24. I^{2}C Multiple-Byte Read

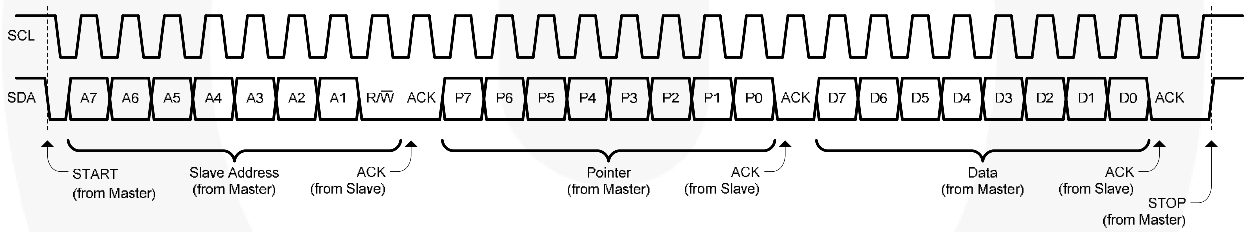

Figure 25. I^{2}C Write

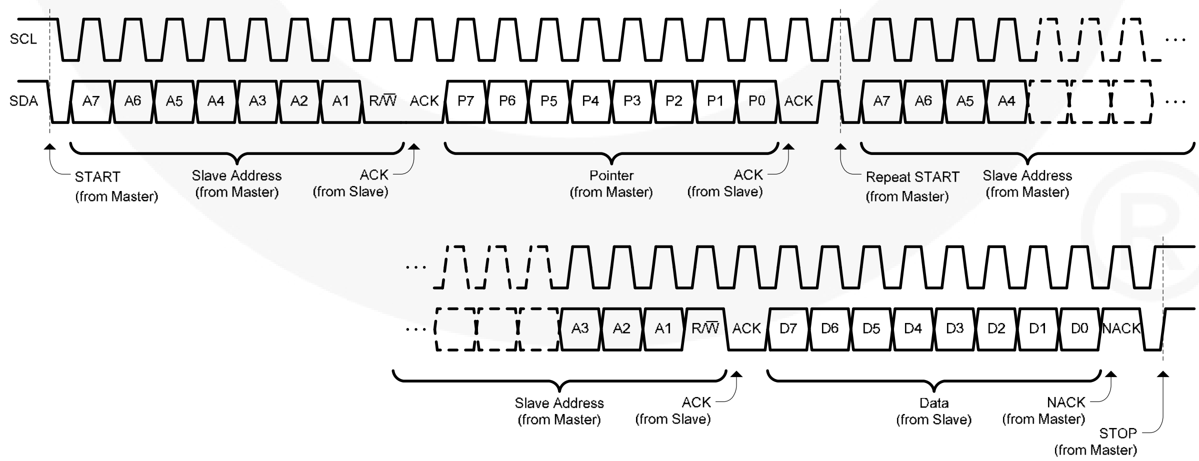

Figure 26. I^{2}C Write Followed by Read

Register Map

The I^2C slave address is 1001101x, where x=0 for write operations and x=1 for read operations.

Address	B7	B6	B5	B4	B3	B2	B1	B0
0x00	VERSION			HPNGTRIP	SPNGTRIP	OVRTEMP	OVRCURSP	0
0x01	HIZL	HIZR	0	BYPEN	0	0	0	SHDNB
0x02	DIFFIN43	DIFFIN21	PGAIN43			PGAIN21		
0x03	SELSPA4	SELSPA3	SELSPA2	SELSPA1	HPRAMPSPEED		HPZCD	HPRAMP
0x04	SELHPL4	SELHPL3	SELHPL2	SELHPL1	SELHPR4	SELHPR3	SELHPR2	SELHPR1
0x05	0	0	HPLVOL					0
0x06	0	0	HPRVOL					0
0x07	HPNGZRA	HPNGTHRESH			HPNGZRR	HPNGTIME		
0x08	ERC	0	0	0	SPRAMPSPEED		SPZCD	SPRAMP
0x09	SPNGZRA	SPNGTHRESH			SPNGZRR	SPNGTIME		
0x0A	THMAX				THVBATT			
0x0B	0	AGCATTACK			0	AGCRELEASE		
0x0C	0	0	AGCMIN					
0x0D	0	0	PRESENTGAIN					
0x0E	0	0	STARTGAIN					
0x0F	0	0	MCSSMT			SSMT		

Bits labeled “0” have no effect if written. When read, the value is always 0.

Bits and addresses not listed in the register map are for testing only. These bits should never be written. When read, they may return any value.

Register Descriptions

Address	B7	B6	B5	B4	B3	B2	B1	B0
0x00	VERSION			HPNGTRIP	SPNGTRIP	OVRTEMP	OVRCURSP	0
default	010			0	0	0	0	0

VERSION (Read only)

Indicates the silicon revision number.

HPNGTRIP (Read only)

1 = Headphone amplifiers are being muted by the noise gate.

0 = Normal operation.

SPNGTRIP (Read only)

1 = Speaker amplifier is being muted by the noise gate.

0 = Normal operation.

OVRTEMP (Read/Clear)

1 = The junction temperature of the device has exceeded the thermal shutdown threshold. (This bit remains set until it is read.)

0 = Normal operation.

OVRCURSP (Read/Clear)

1 = The output current limit of the speaker amplifier has been exceeded. (This bit remains set until it is read.)

0 = Normal operation.

Address	B7	B6	B5	B4	B3	B2	B1	B0
0x01	HIZL	HIZR	0	BYPEN	0	0	0	SHDNB
default	0	0	0	0	0	0	0	0

HIZx

1 = HPx is muted and output is in High-Impedance Mode *(see Table 2)*.

0 = Normal operation.

BYPEN

1 = DPST analog bypass switch is closed.

0 = DPST analog bypass switch is open.

SHDNB

1 = Normal operation.

0 = Low-power Shutdown Mode.

Address	B7	B6	B5	B4	B3	B2	B1	B0
0x02	DIFFIN43	DIFFIN21	PGAIN43			PGAIN21		
default	0	0	0	0	0	0	0	0

DIFFIN43

1 = IN4 and IN3 are configured as a differential pair.

0 = IN4 and IN3 are independent.

DIFFIN21

1 = IN2 and IN1 are configured as a differential pair.

0 = IN2 and IN1 are independent.

PGAIN43

PGAIN43 sets the pre-amplifier gain for IN4 and IN3.

PGAIN21

PGAIN21 sets the pre-amplifier gain for IN2 and IN1.

PGAINxx [2:0]	Pre-Amplifier Gain (dB)	PGAINxx [2:0]	Pre-Amplifier Gain (dB)
000	0	100	12
001	3	101	15
010	6	110	18
011	9	111	21

Address	B7	B6	B5	B4	B3	B2	B1	B0
0x03	SELSPA4	SELSPA3	SELSPA2	SELSPA1	HPRAMPSPEED		HPZCD	HPRAMP
default	0	0	0	0	0	0	0	0
0x04	SELHPL4	SELHPL3	SELHPL2	SELHPL1	SELHPR4	SELHPR3	SELHPR2	SELHPR1
default	0	0	0	0	0	0	0	0

SELSPAx

1 = Channel INx is added to the speaker amplifier’s input.

0 = Channel INx is disconnected from the speaker amplifier’s input.

If all four SELSPAx bits are 0, the speaker amplifier is turned off and the SPKRP and SPKRN outputs stop switching.

SELHPLx

1 = Channel INx is added to the left headphone amplifier’s input.

0 = Channel INx is disconnected from left headphone amplifier’s input.

If all four SELHPLx bits are 0, the left headphone amplifier is turned off.

SELHPRx

1 = Channel INx is added to the right headphone amplifier’s input.

0 = Channel INx is disconnected from right headphone amplifier’s input.

If all four SELHPRx bits are 0, the right headphone amplifier is turned off.

HPRAMPSPEED

HPRAMPSPEED sets timing for the headphone amplifiers’ ramp function according to Table 4.

HPZCD

1 = Headphone amplifier zero-crossing detection is enabled.

0 = Headphone amplifier zero-crossing detection is disabled.

HPRAMP

1 = Headphone amplifier volume ramping is enabled.

0 = Headphone amplifier volume ramping is disabled.

Address	B7	B6	B5	B4	B3	B2	B1	B0
0x05	0	0	HPLVOL					0
default	0	0	0	0	0	0	0	0
0x06	0	0	HPRVOL					0
default	0	0	0	0	0	0	0	0

HPxVOL

HPxVOL sets the gain of the headphone amplifiers according to Table 19.

HPxVOL does not include PGAINxx. Gain for the entire headphone amplifier signal path is defined by PGAINxx + HPxVOL.

Table 19. Headphone Amplifier Gain Settings

HPxVOL [4:0]	Gain (dB)	HPxVOL [4:0]	Gain (dB)
00000	mute	10000	-9
00001	-53	10001	-8
00010	-49	10010	-7
00011	-45	10011	-6
00100	-41	10100	-5
00101	-37	10101	-4
00110	-33	10110	-3
00111	-29	10111	-2
01000	-25	11000	-1
01001	-23	11001	0
01010	-21	11010	1
01011	-19	11011	2
01100	-17	11100	3
01101	-15	11101	4
01110	-13	11110	5
01111	-11	11111	6

Address	B7	B6	B5	B4	B3	B2	B1	B0
0x07	HPNGZRA	HPNGTHRESH			HPNGZRR	HPNGTIME		
default	0	0	0	0	0	0	0	0

HPNGZRA

1 = The headphone noise gate attack function obeys headphone zero-crossing detection and ramp settings.

0 = The headphone noise gate attack (mute) function occurs immediately rather than waiting for zero-crossing detection or ramping.

HPNGTHRESH

HPNGTHRESH sets the threshold voltage for the headphone amplifiers' noise gate function according to Table 1.

HPNGZRR

1 = The headphone noise gate release (un-mute) function obeys headphone zero-crossing detection and ramp settings.

0 = The headphone noise gate release (un-mute) function occurs immediately rather than waiting for zero-crossing detection or ramping.

HPNGTIME

HPNGTIME sets the timing for the headphone amplifiers' noise gate function according to Table 6.

Address	B7	B6	B5	B4	B3	B2	B1	B0
0x08	ERC	0	0	0	SPRAMPSPEED		SPZCD	SPRAMP
default	0	0	0	0	0	0	0	0

ERC

1 = Speaker amplifier edge-rate control is enabled.

0 = Speaker amplifier edge-rate control is disabled.

SPRAMPSPEED

SPRAMPSPEED sets timing for the speaker amplifier's ramp function according to Table 17.

SPZCD

1 = Speaker amplifier zero-crossing detection is enabled.

0 = Speaker amplifier zero-crossing detection is disabled.

SPRAMP

1 = Speaker amplifier gain ramping is enabled.

0 = Speaker amplifier gain ramping is disabled.

Address	B7	B6	B5	B4	B3	B2	B1	B0
0x09	SPNGZRA	SPNGTHRESH			SPNGZRR	SPNGTIME		
default	0	0	0	0	0	0	0	0

SPNGZRA

1 = The speaker noise gate attack function obeys speaker zero-crossing detection and ramp settings.

0 = The speaker noise gate attack (mute) function occurs immediately rather than waiting for zero-crossing detection or ramping.

SPNGTHRESH

SPNGTHRESH sets the threshold voltage for the speaker amplifier's noise gate function according to Table 14.

SPNGZRR

1 = The speaker noise gate release (un-mute) function obeys speaker zero-crossing detection and ramp settings.

0 = The speaker noise gate release (un-mute) function occurs immediately rather than waiting for zero-crossing detection or ramping.

SPNGTIME

SPNGTIME sets the timing for the speaker amplifier's noise gate function according to Table 15.

Address	B7	B6	B5	B4	B3	B2	B1	B0
0x0A	THMAX				THVBATT			
default	0	0	0	0	0	0	0	0

THMAX

THMAX sets the maximum threshold voltage for the speaker amplifier's AGC according to Table 9.

THVBATT

THVBATT sets the clipping level relative to V_{BATT} for the speaker amplifier's AGC according to Table 10.

Address	B7	B6	B5	B4	B3	B2	B1	B0
0x0B	0	AGCATTACK			0	AGCRELEASE		
default	0	0	0	0	0	0	0	0

AGCATTACK

AGCATTACK sets the attack speed for the speaker amplifier's AGC according to Table 12.

AGCRELEASE

AGCRELEASE sets the release speed for the speaker amplifier's AGC according to Table 13.

Address	B7	B6	B5	B4	B3	B2	B1	B0
0x0C	0	0	AGCMIN					
default	0	0	0	0	0	0	0	0

AGCMIN

AGCMIN sets the minimum gain for the speaker amplifier's AGC according to Table 11.

Address	B7	B6	B5	B4	B3	B2	B1	B0
0x0D	0	0	PRESENTGAIN					

PRESENTGAIN

(Read only)

PRESENTGAIN is the actual gain setting for the speaker amplifier according to Table 11. The target value for PRESENTGAIN is set by STARTGAIN. However, PRESENTGAIN may be changed automatically by the AGC or the noise gate.

PRESENTGAIN does not include PGAINxx. Gain for the entire speaker amplifier signal path is defined by PGAINxx + PRESENTGAIN.

Address	B7	B6	B5	B4	B3	B2	B1	B0
0x0E	0	0	STARTGAIN					
default	0	0	0	0	0	0	0	0

STARTGAIN

STARTGAIN is the volume setting for the speaker amplifier according to Table 11.

Address	B7	B6	B5	B4	B3	B2	B1	B0
0x0F	0	0	MCSSMT			SSMT		
default	0	0	1	0	0	0	0	0

SSMT

Sets the spread-spectrum modulation of the class-D amplifier. *See Table 20 for the amount of modulation*. A setting of 000 results in a ±5.3% modulation in the speaker amplifier's output frequency. A setting of 100 disables spread-spectrum modulation.

Table 20. Class-D Spread-Spectrum Modulation Trim

SSMT [2:0]	Class-D Spread-Spectrum Modulation Trim (±%)
000	5.3
001	7.0
010	10.6
011	21.2
100	0.0
101	3.0
110	3.6
111	4.2

MCSSMT [5:3]

Sets the spread-spectrum modulation of the master clock. *See Table 21 for amount of modulation*. Modulating the master clock does not modulate the class-D output frequency because the triangle wave generator is PLL controlled.

Table 21. Master Clock Spread-Spectrum Modulation Trim

MCSSMT [2:0]	Master Clock Spread-Spectrum Modulation Trim (± %)
000	5.3
001	7.0
010	10.6
011	21.2
100	0.0
101	3.0
110	3.6
111	4.2

Applications Information

Layout Considerations

General layout and supply bypassing play a major role in analog performance and thermal characteristics. Fairchild offers a demonstration board to guide layout and aid device evaluation (contact Fairchild for details). Following this layout configuration provides optimum performance for the device. For the best results, follow the steps and recommended routing rules listed below.

Recommended Routing / Layout Rules

- Do not run analog and digital signals in parallel.
- Use separate analog and digital power planes to supply power.
- Place the speaker amplifier output as close as possible to the speaker element to reduce EMI.
- Traces should be run on top of the ground plane at all times.
- No trace should run over ground / power splits.
- Avoid routing at 90-degree angles.
- Place bypass capacitors within 0.1 inches of the device power pin.
- Minimize all trace lengths to reduce series inductance.

Physical Dimensions

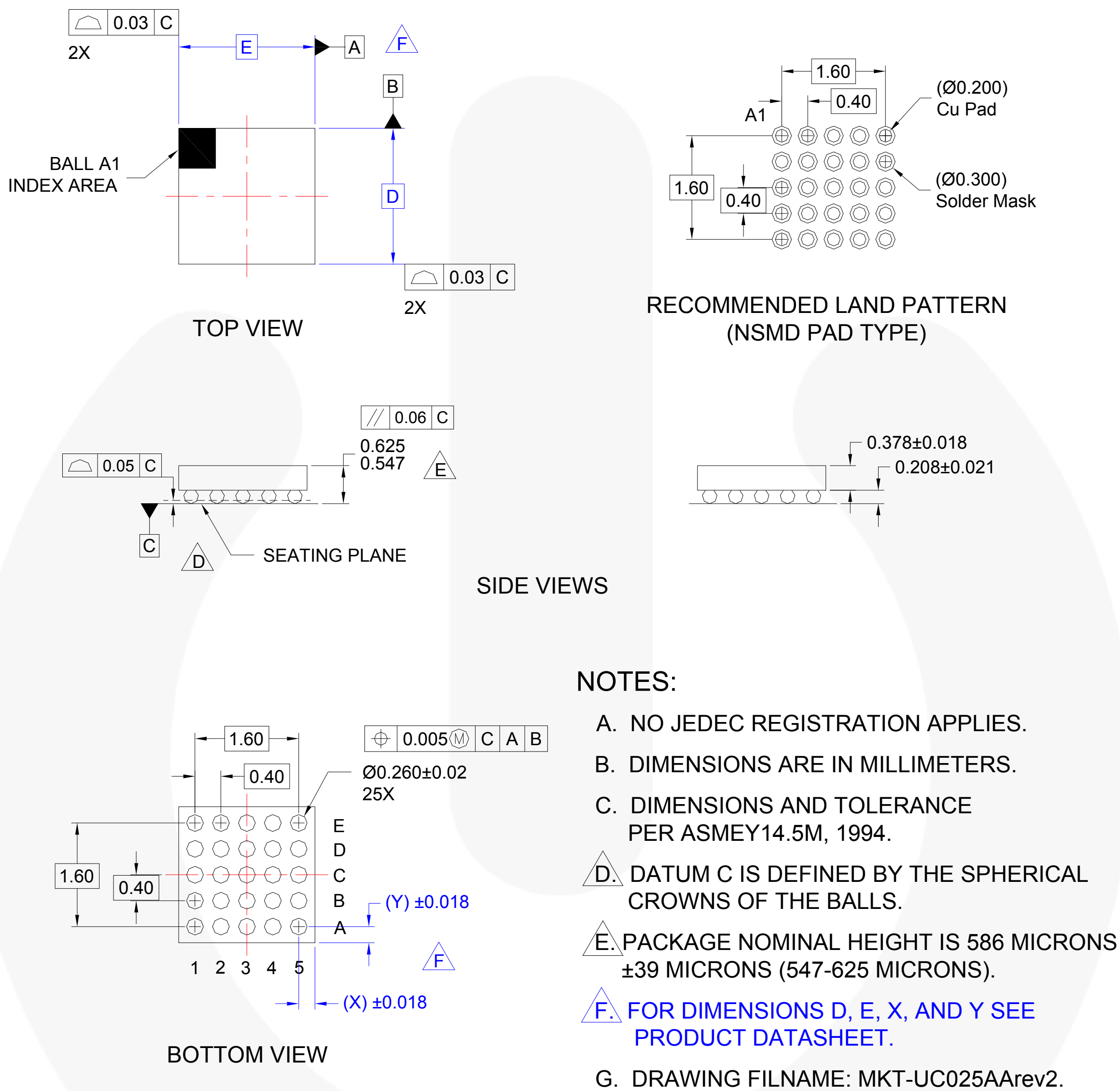

Figure 27. 25-Bump, 0.4mm Pitch, Wafer-Level Chip-Scale Package (WLCSP)

Product	D	E	X	Y
FAB2200UCX	2.06mm	2.38mm	0.39mm	0.23mm

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Datasheet Identification	Product Status	Definition
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