TEXAS INSTRUMENTS

LM5026

SNVS363E – AUGUST 2005 – REVISED NOVEMBER 2015

LM5026 Active Clamp Current Mode PWM Controller

1 Features

- Current-Mode Control
- Internal 100-V Start-Up Bias Regulator
- 3-A Compound Main Gate Driver
- High Bandwidth Optocoupler Interface
- Programmable Line Undervoltage Lockout (UVLO) With Adjustable Hysteresis
- Versatile Dual Mode Overcurrent Protection With Hiccup Delay Timer
- Programmable Overlap or Deadtime between the Main and Active Clamp Outputs
- Programmable Maximum Duty Cycle Clamp
- Programmable Soft-Start
- Leading Edge Blanking
- Resistor Programmed 1-MHz Capable Oscillator
- Oscillator Sync I/O Capability
- Precision 5-V Reference

2 Applications

- Server Power Supplies
- 48-V Telecom Power Supplies
- High Efficiency DC–DC Power Supplies

3 Description

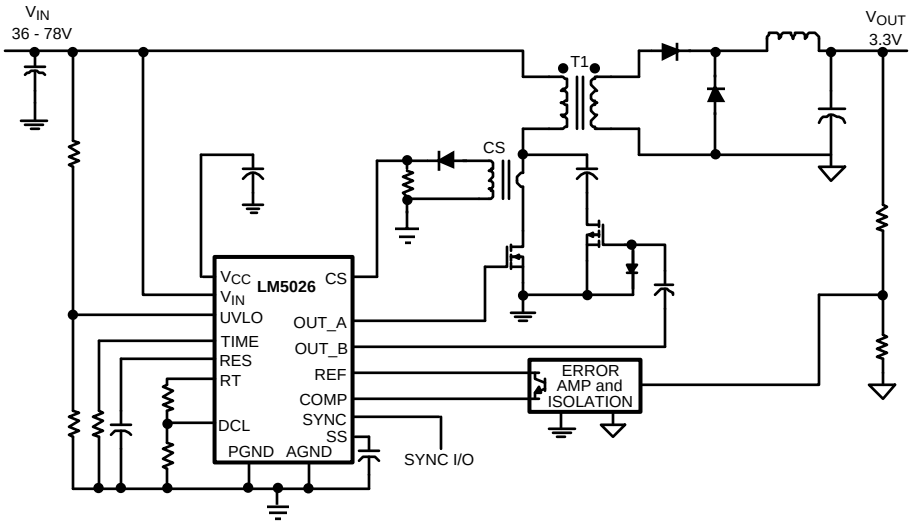
The LM5026 PWM controller contains all of the features necessary to implement power converters utilizing the active clamp and reset technique with current-mode control. With the active clamp technique, higher efficiencies and greater power densities can be realized compared to conventional catch winding or RDC clamp and reset techniques. Two control outputs are provided, the main power switch control (OUT_A) and the active clamp switch control (OUT_B). The device can be configured to control either a P-Channel or N-Channel clamp switch. The main gate driver features a compound configuration, consisting of both MOS and Bipolar devices, providing superior gate drive characteristics. The LM5026 can be configured to operate with bias voltages over a wide input range of 8 V to 100 V. Additional features include programmable maximum duty cycle, line undervoltage lockout, cycle-by-cycle current limit, hiccup mode fault operation with adjustable timeout delay, PWM slope compensation, soft-start, 1-MHz capable oscillator with synchronization input and output capability, precision reference, and thermal shutdown.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM5026	WSON (16)	5.00 mm × 5.00 mm
	TSSOP (16)	4.40 mm × 5.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Circuit



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (April 2013) to Revision E — **Page**

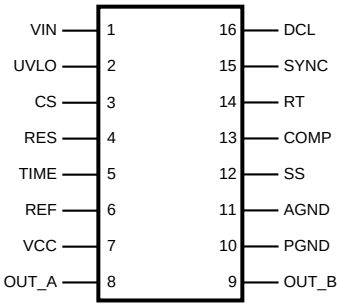
- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1

Changes from Revision C (April 2013) to Revision D — **Page**

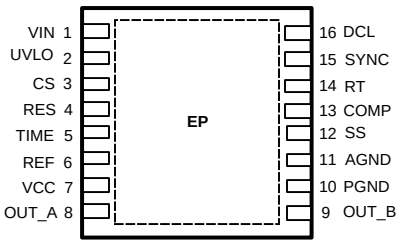
- Changed layout of National Data Sheet to TI format ... 25

5 Pin Configuration and Functions

PW Package
16-Pin TSSOP
Top View



NHQ Package
16-Pin WSON
Top View



Pin Functions

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
1	VIN	I	Input voltage source. Input to the start-up regulator. Operating input range is 13 V to 100 V with transient capability to 105 V. For power sources outside of this range, the LM5026 can be biased directly at VCC by an external regulator.
2	UVLO	I	Line undervoltage lockout. An external voltage divider from the power source sets the shutdown and standby comparator levels. When UVLO reaches the 0.4-V threshold the VCC and REF regulators are enabled. At the 1.25-V threshold the SS pin is released and the device enters the active mode.
3	CS	I	Current Sense input for current mode control and current limit. If CS exceeds 0.5 V, the output pulse will be terminated, entering cycle-by-cycle current limit. An internal switch holds CS low for 100 nS after OUT_A switches high to blank leading edge transients.
4	RES	I	Restart Timer. If cycle-by-cycle current limit is reached during any cycle, a 10-µA current is sourced to the RES pin capacitor. If the RES capacitor voltage reaches 2.5 V, the soft-start capacitor will be fully discharged and then released with a pullup current of 1 µA. After the first output pulse at OUT_A (when SS = 1.4 V), the SS pin charging current will revert back to 50 µA.
5	TIME	I	Gate drive overlap or deadtime control. An external resistor (RSET) sets either the overlap time or deadtime for the active clamp output. An RSET resistor connected between TIME and AGND produces in-phase OUT_A and OUT_B pulses with overlap. An RSET resistor connected between TIME and REF produces out-of-phase OUT_A and OUT_B pulses with deadtime.
6	REF	O	Output of 5-V reference. Maximum output current is 10 mA. Locally decouple with a 0.1-µF capacitor.
7	VCC	P	Output of the high voltage start-up regulator. The VCC voltage is regulated to 7.6 V. If an auxiliary winding raises the voltage on this pin above the regulation setpoint, the internal start-up regulator will shutdown, thus reducing the IC power dissipation.
8	OUT_A	O	Main output driver. Output of the main switch PWM gate driver. Capable of 3-A peak sink current.
9	OUT_B	O	Active clamp output driver. Output of the active clamp switch gate driver. Capable of 0.5-A peak source and sink current.
10	PGND	G	Power ground. Connect directly to analog cround.
11	AGND	G	Analog return. Connect directly to power cround.
12	SS	I	Soft-start. An external capacitor and an internal 50-µA current source set the soft-start ramp. The SS current source is reduced to 1 µA following a restart event. The soft-stop discharge current is 50 µA.
13	COMP	I	Input to the pulse width modulator. The external optocoupler connected to the COMP pin sources current into an internal NPN current mirror. The PWM duty cycle is maximum with zero input current, while 1 mA reduces the duty cycle to zero. The current mirror improves the frequency response by reducing the ac voltage across the optocoupler detector.

(1) P = Power, G = Ground, I = Input, O = Output, I/O = Input/Output

Pin Functions (continued)

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
14	RT	I	Oscillator frequency control. Normally biased at 2 V. The total external resistance connected between RT and AGND sets the internal oscillator frequency.
15	SYNC	I/O	Oscillator synchronization input/output. The internal oscillator can be synchronized to an external clock with an external pulldown device. Multiple LM5026 devices can be synchronized together by connection of their SYNC pins.
16	DCL	I	Maximum duty cycle control. An external resistor divider connected from RT to AGND sets the maximum output duty cycle for OUT_A.
EP	Exposed Pad (WSON Package Only)	G	Exposed Pad, underside of WSON package. Connect to system ground plane for reduced thermal resistance.

6 Specifications

6.1 Absolute Maximum Ratings

See (1)(2).

	MIN	MAX	UNIT
V_{IN} to GND	–0.3	105	V
V_{CC} to GND	–0.3	16	V
CS to GND	–0.3	1	V
COMP input current		10	mA
All other inputs to GND	–0.3	7	V
Junction temperature		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)(2)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (3)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions. Pins listed as ±2000 V may actually have higher performance.
(2) The human body model is a 100-pF capacitor discharged through a 1.5-kΩ resistor into each pin.
(3) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted) (1)

	MIN	MAX	UNIT
V_{IN} voltage	13	100	V
External voltage applied to V_{CC}	8	15	V
Operating junction temperature	–40	125	°C

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is intended to be functional. For specifications and test conditions, see the *Electrical Characteristics*.

6.4 Thermal Information

THERMAL METRIC[1]		LM5026 NHQ (WSON) 16 PINS	LM5026 PW (TSSOP) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	29.9	98.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	25.8	27.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	9.2	44.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	1.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	9.5	43.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.3	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

Specification typical values are for T_J = 25°C unless otherwise noted. V_{IN} = 48 V, V_{CC} = 10 V, RT = 30.0 kΩ, Rset = 34.8 kΩ unless otherwise stated. Minimum and maximum specifications apply over full operating junction temperature range.[1]

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
START-UP REGULATOR							
V_{CC} Reg	V_{CC} regulation	No Load	T_J = 25°C		7.6		V
			over full operating junction temperature range	7.3		7.9	
	V_{CC} current limit	See [2]	T_J = 25°C		25		mA
			over full operating junction temperature range	20			
I-V_{IN}	Start-up regulator leakage (external V_{CC} supply)	V_{IN} = 100 V	T_J = 25°C		165		µA
			over full operating junction temperature range			500	
	Shutdown current (Iin)	UVLO = 0 V	T_J = 25°C		350		µA
			over full operating junction temperature range			450	
V_{CC} SUPPLY							
	V_{CC} undervoltage lockout voltage (positive going V_{cc})	T_J = 25°C			V_{CC} Reg – 120 mV		V
		over full operating junction temperature range		V_{CC} Reg – 220 mV			
	V_{CC} undervoltage hysteresis	T_J = 25°C			1.5		V
		over full operating junction temperature range		1		2	
	V_{CC} supply current (I_{CC})	C_{gate} = 0, UVLO = 1.3 V, over full operating junction temperature range				4.2	mA
REFERENCE SUPPLY							
V_{REF}	Ref voltage	I_{REF} = 0 mA	T_J = 25°C		5		V
			over full operating junction temperature range	4.85		5.15	
	Ref voltage regulation	I_{REF} = 0 to 10 mA	T_J = 25°C		25		mV
			over full operating junction temperature range			50	
	Ref current limit	T_J = 25°C			20		mA
		over full operating junction temperature range		10			
UVLO SHUTDOWN/STANDBY							
	Undervoltage shutdown threshold	T_J = 25°C			0.4		V
		over full operating junction temperature range		0.3		0.5	

(1) Minimum and maximum limits are 100% production tested at 25ºC. Limits over the operating temperature range are specified through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate Average Outgoing Quality Level (AOQL). All electrical characteristics having room temperature limits are tested during production with T_A = T_J = 25°C. All hot and cold limits are specified by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(2) Device thermal limitations may limit usable range.

Electrical Characteristics (continued)

Specification typical values are for T_J = 25°C unless otherwise noted. V_{IN} = 48 V, V_{CC} = 10 V, RT = 30.0 kΩ, Rset = 34.8 kΩ unless otherwise stated. Minimum and maximum specifications apply over full operating junction temperature range.(1)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Undervoltage shutdown hysteresis				0.1		V
Undervoltage standby threshold	T_J = 25°C			1.25		V
	over full operating junction temperature range		1.21		1.29	
Undervoltage sandby hysteresis current source	T_J = 25°C			20		µA
	over full operating junction temperature range		16		24	
CURRENT LIMIT						
Cycle-by-cycle threshold voltage	T_J = 25°C			0.5		V
	over full operating junction temperature range		0.45		0.55	
ILIM delay-to-output	CS step from 0 to 0.6 V Time to onset of OUT transition (90%) Cgate=0			40		ns
Leading edge blanking time	T_J = 25°C			100		ns
	over full operating junction temperature range		70		130	
CS sink impedance (clocked)	I_{CS} = 10 mA	T_J = 25°C		30		Ω
		over full operating junction temperature range			65	
OVERCURRENT RESTART						
Restart threshold	T_J = 25°C			2.55		V
	over full operating junction temperature range		2.4		2.7	
Fault-charging current	T_J = 25°C			10		µA
	over full operating junction temperature range		7.5		12.5	
Discharging current	T_J = 25°C			10		µA
	over full operating junction temperature range		7.5		12.5	
SOFT-START						
Soft-start current source	T_J = 25°C			50		µA
	over full operating junction temperature range		38		58	
Soft-stop current sink	T_J = 25°C			50		
	over full operating junction temperature range		38		58	
Soft-start current source following a restart event	T_J = 25°C			1		
	over full operating junction temperature range		0.6		1.3	
OSCILLATOR						
Frequency1	RT = 30 kΩ	T_J = 25°C		200		kHz
		over full operating junction temperature range	180		220	
Frequency2	RT = 10 kΩ	T_J = 25°C		590		kHz
		over full operating junction temperature range	520		660	
SYNC source current				200		µA
SYNC sink impedance	Can sync up to 5 like controllers minimum			100		Ω
Sync threshold (falling)				1.4		V
Sync pulse width minimum	over full operating junction temperature range		15			ns
PWM COMPARATOR						
Delay-to-output	CS stepped, time to onset of OUT_A transition low			40		ns
Mimimum duty cycle	I_{COMP} = 1 mA, over full operating junction temperature range				0%	
Maximum duty cycle limit 1	UVLO = 1.3 V, COMP = open, V_{DCL} = 2.5 V			80%		
Maximum duty cycle limit 2	UVLO = 1.3 V, COMP = open, V_{DCL} = V_{RT} × 0.875			70%		

Electrical Characteristics (continued)

Specification typical values are for T_J = 25°C unless otherwise noted. V_{IN} = 48 V, V_{CC} = 10 V, RT = 30.0 kΩ, Rset = 34.8 kΩ unless otherwise stated. Minimum and maximum specifications apply over full operating junction temperature range.(1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
	Maximum duty cycle limit 3	UVLO = 2.92 V, COMP = open, V_{DCL} = 2.5 V			40%		
	SS to PWM offset				1.4		V
	COMP input impedance	Small signal impedance			1700		Ω
	Slope compensation amplitude	Delta increase at PWM comparator to CS	T_J = 25°C		90		mV
			over full operating junction temperature range	75		115	
OUTPUT SECTION							
	OUT_A high saturation	MOS Device at I_{OUT} = –10 mA,	T_J = 25°C		5		Ω
			over full operating junction temperature range			10	
	OUTPUT_A peak current sink	Bipolar Device at V_{CC}/2			3		A
	OUT_A low saturation	MOS Device at I_{OUT} = 10 mA,	T_J = 25°C		6		Ω
			over full operating junction temperature range			9	
	OUTPUT_A rise time	C_{gate} = 2.2 nF			20		ns
	OUTPUT_A fall time	C_{gate} = 2.2 nF			15		ns
	OUT_B high saturation	I_{OUT} = –10 mA	T_J = 25°C		10		Ω
			over full operating junction temperature range			20	
	OUT_B low saturation	I_{OUT} = 10 mA	T_J = 25°C		10		Ω
			over full operating junction temperature range			20	
	OUTPUT_B rise time	C_{gate} = 470 pF			15		ns
	OUTPUT_B fall time	C_{gate} = 470 pF			15		ns
OUTPUT TIMING CONTROL							
	Overlap time	R_{SET} = 34.8 kΩ connected to GND, 50% to 50% transitions	T_J = 25°C		100		ns
			over full operating junction temperature range	70		130	
	Deadtime	R_{SET} = 30 kΩ connected to REF, 50% to 50% transitions	T_J = 25°C		100		ns
			over full operating junction temperature range	70		130	
THERMAL SHUTDOWN							
T_{SD}	Thermal shutdown temp.			150	165		°C
	Thermal shutdown hysteresis				25		°C

6.6 Typical Characteristics

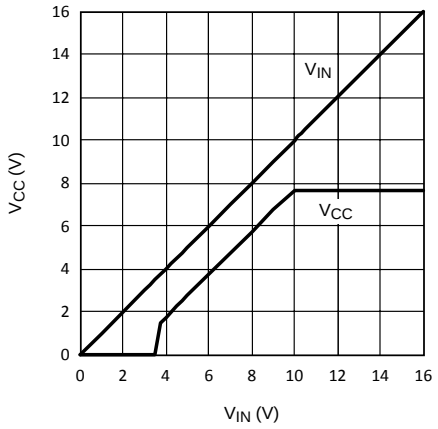


Figure 1. V_{CC} Regulator Start-Up Characteristics, V_{CC} vs V_{IN}

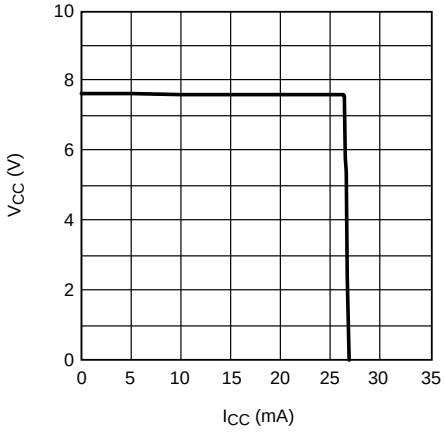


Figure 2. V_{CC} vs I_{CC}

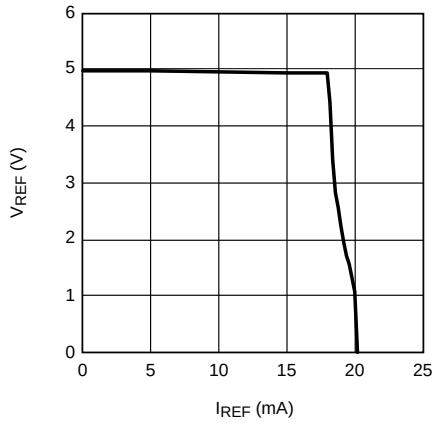


Figure 3. V_{REF} vs I_{REF}

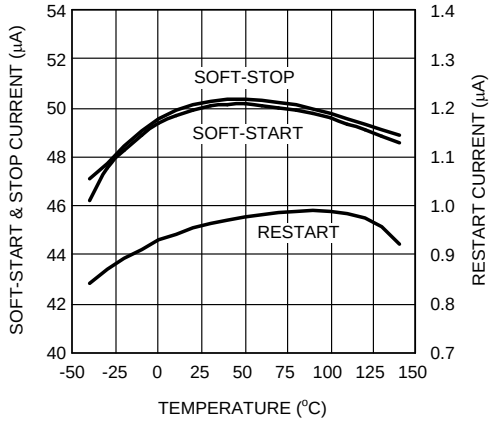


Figure 4. Soft-Start, Soft-Stop and Restart Current vs Temperature

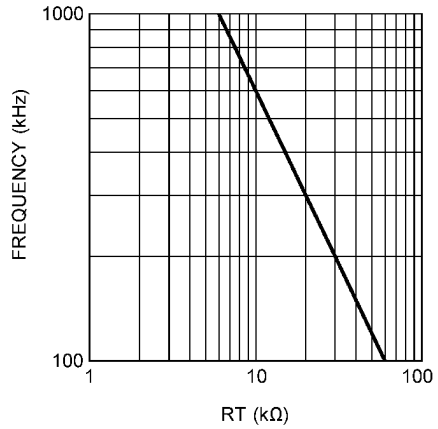


Figure 5. Oscillator Frequency vs RT

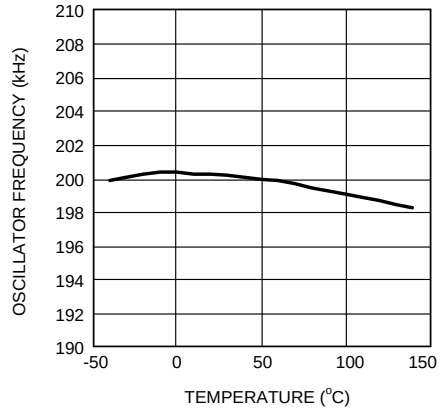


Figure 6. Oscillator Frequency vs Temperature

Typical Characteristics (continued)

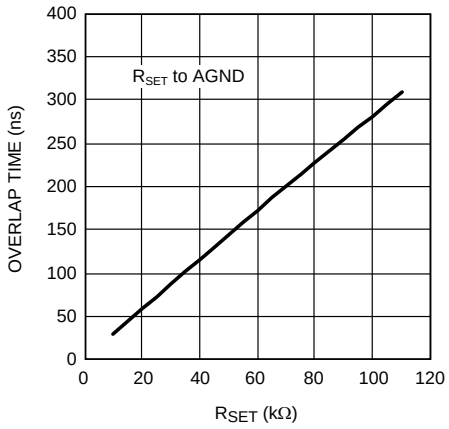


Figure 7. Overlap Time vs R_{SET}

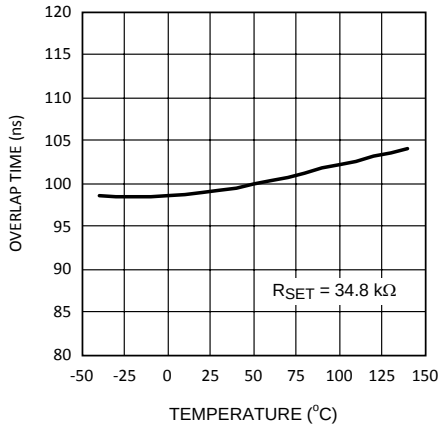


Figure 8. Overlap Time vs Temperature

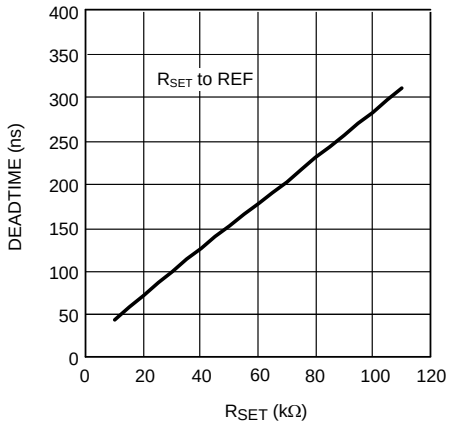


Figure 9. Deadtime vs R_{SET}

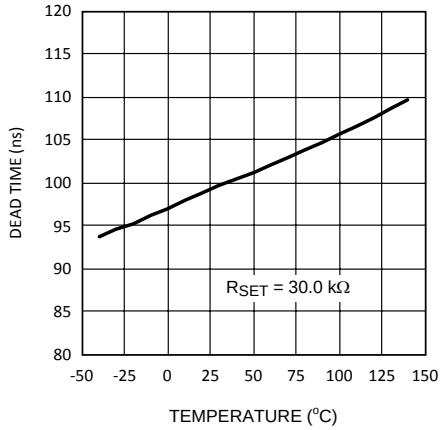


Figure 10. Deadtime vs Temperature

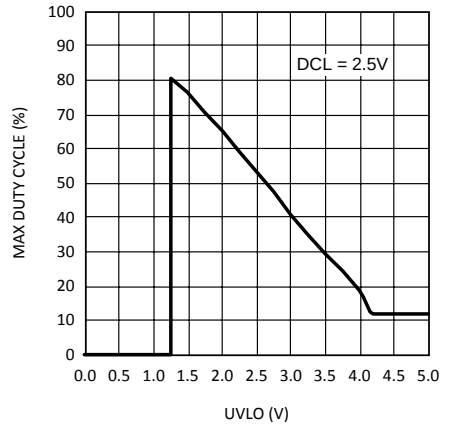


Figure 11. Max Duty Cycle vs UVLO

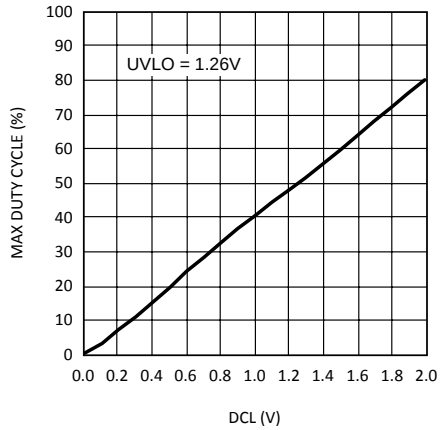


Figure 12. Max Duty Cycle vs DCL

Typical Characteristics (continued)

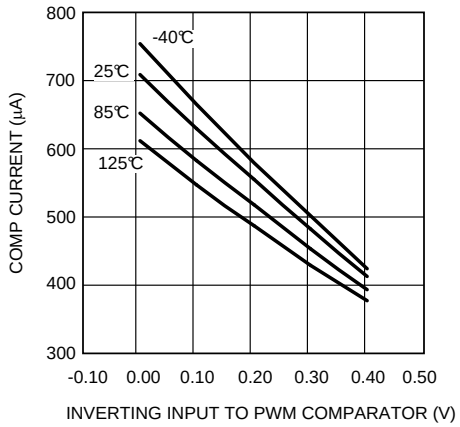


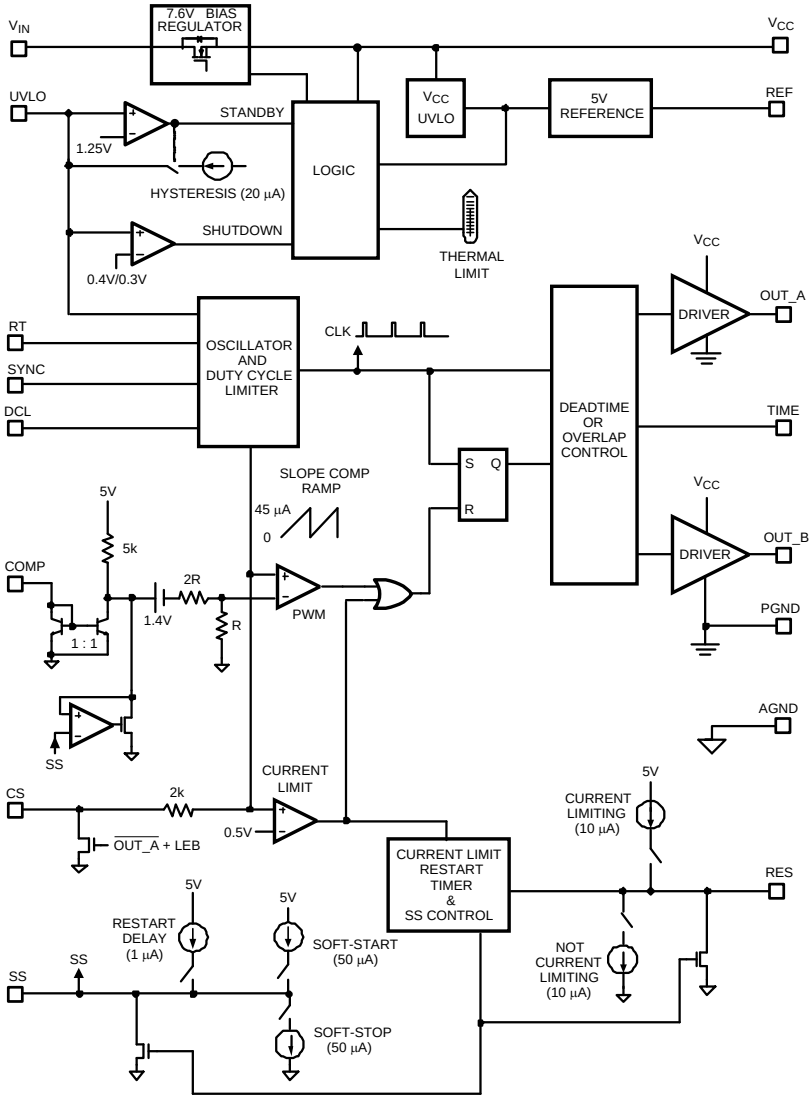
Figure 13. COMP Current vs INV PWM Comparator Voltage

7 Detailed Description

7.1 Overview

The LM5026 PWM controller contains all of the features necessary to implement power converters utilizing the active clamp reset technique with current mode control. With the active clamp reset, higher efficiencies and greater power densities can be realized compared to conventional catch winding or RDC clamp reset techniques. The LM5026 provides two control outputs, the main power switch control (OUT_A) and the active clamp switch control (OUT_B). The device can be configured to drive either a P-Channel or N-Channel clamp switch. The main switch gate driver features a compound configuration consisting of both MOS and bipolar devices, which provide superior gate drive characteristics. The LM5026 can be configured to operate with bias voltages over a wide input range from 8 V to 100 V. Additional features include programmable maximum duty cycle, line undervoltage lockout, cycle-by-cycle current limit, hiccup mode fault protection with adjustable delays, PWM slope compensation, soft-start, a 1-MHz capable oscillator with synchronization input and output capability, precision reference, and thermal shutdown.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 High Voltage Start-Up Regulator

The LM5026 contains an internal high voltage start-up regulator that allows the input pin (VIN) to be connected directly to a nominal 48-V DC line voltage. The regulator output (VCC) is internally current limited to 20 mA. When power is applied and the UVLO pin potential is greater than 0.4 V, the regulator is enabled and sources current into an external capacitor connected to the VCC pin. The recommended capacitance range for the VCC regulator is 0.1 µF to 100 µF. The VCC regulator provides power to the internal voltage reference, PWM controller and gate drivers. The controller outputs are enabled when the voltage on the VCC pin reaches the regulation point of 7.6 V, the internal voltage reference (REF) reaches its regulation point of 5 V and the UVLO voltage is greater than 1.25 V. In typical applications, an auxiliary transformer winding is connected through a diode to the VCC pin. This winding must raise the VCC voltage above 8 V to shut off the internal start-up regulator. Powering VCC from an auxiliary winding improves efficiency while reducing the controller's power dissipation.

The external VCC capacitor must be sized such that the current delivered from the capacitor and the VCC regulator will maintain a VCC voltage greater than 6.2 V during the initial start-up. During a fault mode when the converter auxiliary winding is inactive, external current draw on the VCC line should be limited such that the power dissipated in the start-up regulator does not exceed the maximum power dissipation of the IC package. An external start-up or bias regulator can be used to power the LM5026 instead of the internal start-up regulator by connecting the VCC and the VIN pins together and connecting an external bias supply to these two pins.

7.3.2 Line Undervoltage Detector

The LM5026 contains a dual level undervoltage lockout (UVLO) circuit. When the UVLO pin voltage is below 0.4 V, the controller is in a low current shutdown mode. When the UVLO pin voltage is greater than 0.4 V but less than 1.25 V, the controller is in standby mode. In standby mode the VCC and REF bias regulators are active while the controller outputs are disabled. When the VCC and REF outputs exceed the VCC and REF undervoltage thresholds and the UVLO pin voltage is greater than 1.25 V, the outputs are enabled and normal operation begins. An external set-point voltage divider from VIN to GND can be used to set the operational range of the converter. The divider must be designed such that the voltage at the UVLO pin will be greater than 1.25 V when VIN is in the desired operating range. UVLO hysteresis is accomplished with an internal 20-µA current source that is switched on or off into the impedance of the set-point divider. When the UVLO threshold is exceeded, the current source is activated to instantly raise the voltage at the UVLO pin. When the UVLO pin voltage falls below the 1.25-V threshold, the current source is turned off causing the voltage at the UVLO pin to fall. The hysteresis of the 0.4-V shutdown comparator is fixed at 100 mV.

The UVLO pin can also be used to implement various remote enable and disable functions. Pulling the UVLO pin below the 0.4-V threshold totally disables the controller. Pulling the UVLO pin to a potential between 1.25 and 0.4 V places the controller in standby with the VCC and REF regulators operating. Turning off a converter by forcing the UVLO pin to the standby condition provides a controlled soft-stop. The controller outputs are not directly disabled in standby mode, rather the soft-start capacitor is discharged with a 50-µA sink current. Discharging the soft-start capacitor gradually reduces the PWM duty cycle to zero, providing a slow controlled discharge of the power converter output filter. This controlled discharge can help prevent uncontrolled behavior of self-driven synchronous rectifiers during turnoff.

7.3.3 PWM Outputs

The relative phase of the main switch gate driver OUT_A and active clamp gate driver OUT_B can be configured for multiple applications. For active clamp configurations utilizing a ground referenced P-Channel clamp switch, the two outputs should be in phase, with the active clamp output overlapping the main output. For active clamp configurations utilizing a high-side N-Channel switch, the active clamp output should be out of phase with main output and there should be a dead time between the two gate drive pulses. A distinguishing feature of the LM5026 is the ability to accurately configure either deadtime (both off) or overlap time (both on) of the gate driver outputs. The overlap / deadtime magnitude is controlled by the resistor value (RSET) connected to the TIME pin of the controller. The opposite end of the resistor can be connected to either REF for deadtime control or to AGND for overlap control. The internal configuration detector senses the direction of current flow in the TIME pin resistor and configures the phase relationship of the main and active clamp outputs.

Feature Description (continued)

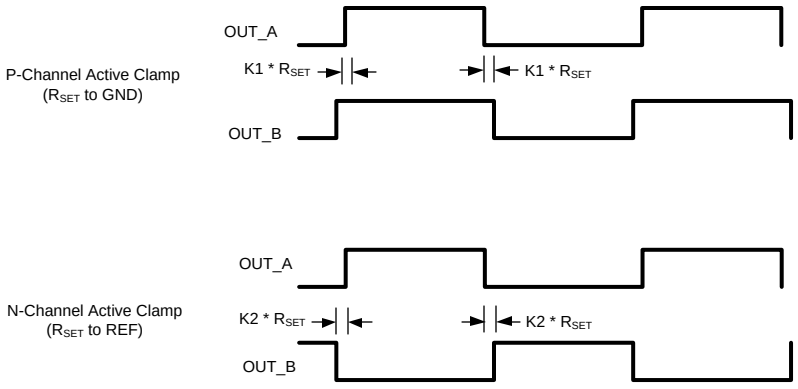


Figure 14. PWM Output Phasing / Timing

The rising edge overlap or deadtime and the falling edge overlap or deadtime are identical and are independent of operating frequency or duty cycle. The magnitude of the overlap/deadtime can be calculated in Equation 1 and Equation 2:

$$\text{Overlap Time} = 2.8 \times R_{SET} + 2 \quad (1)$$

where

- R_{SET} in kΩ
- overlap is in ns

$$\text{Deadtime} = 2.9 \times R_{SET} + 14 \quad (2)$$

where

- R_{SET} in kΩ
- deadtime is in ns

7.3.4 Gate Driver Outputs

The LM5026 provides two-gate driver outputs, the main power switch control (OUT_A) and the active clamp switch control (OUT_B). The main gate driver features a compound configuration, consisting of both MOS and bipolar devices, which provide superior gate drive characteristics. The bipolar device provides most of the drive current capability and sinks a relatively constant current, which is ideal for driving large-power MOSFETs. As the switching event nears conclusion and the bipolar device saturates, the internal MOS device provides a low impedance to compete the switching event.

During turnoff at the Miller plateau region, typically between 2 V to 4 V, the voltage differential between the output and PGND is small and the current source characteristic of the bipolar device is beneficial to reduce the transition time. During turnon, the resistive characteristics of a purely MOS gate driver is adequate since the supply to output voltage differential is fairly large in the Miller region.

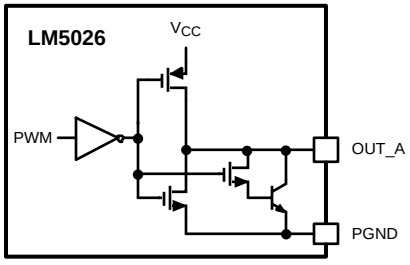


Figure 15. Compound Gate Driver

Feature Description (continued)

7.3.5 PWM Comparator/Slope Compensation

The PWM comparator modulates the pulse width of the controller output by comparing the current sense ramp signal to the loop error signal. This comparator is optimized for speed in order to achieve minimum controllable duty cycles. The loop error signal is input into the controller in the form of a control current into the COMP pin. The COMP pin control current is internally mirrored by a matched pair of NPN transistors which sink current through a 5-kΩ resistor connected to the 5-V reference. The resulting error signal passes through a 1.4-V level shift and a gain reducing 3:1 resistor divider before being applied to the pulse width modulator.

The optocoupler detector can be connected between the REF pin and the COMP pin. Because the COMP pin is controlled by a current input, the potential difference across the optocoupler detector is nearly constant. The bandwidth limiting phase delay which is normally introduced by the significant capacitance of the optocoupler is greatly reduced. Greater system loop bandwidth can be realized, since the bandwidth-limiting pole associated with the optocoupler is now at a much higher frequency. The PWM comparator polarity is configured such that with no current into the COMP pin, the controller produces the maximum duty cycle at the main gate driver output.

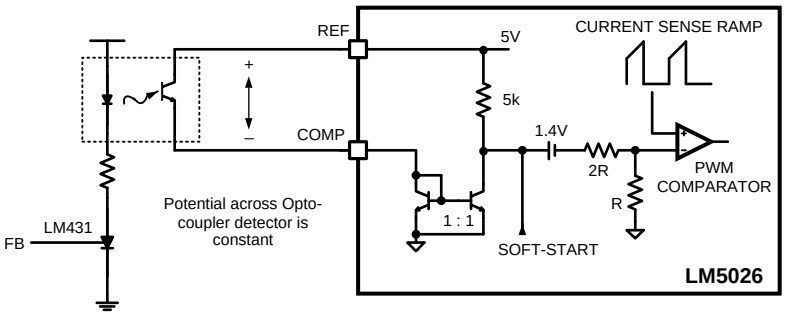


Figure 16. Optocoupler to LM5026 COMP Interface

For duty cycles greater than 50 percent, current mode control circuits are subject to sub-harmonic oscillation. By adding an additional fixed slope voltage ramp signal (slope compensation) to the current sense signal, this oscillation can be avoided. The LM5026 integrates this slope compensation by summing a current ramp generated by the oscillator with the current sense signal. The PWM comparator ramp signal is a combination of the current waveform at the CS pin, and an internally generated slope compensation ramp derived from the oscillator. The internal ramp has an amplitude of 0 to 45 µA which is sourced into an internal 2-kΩ resistor, plus the external impedance at the CS pin. Additional slope compensation may be added by increasing the source impedance of the current sense signal.

7.3.6 Maximum Duty Cycle Clamp

Controlling the maximum duty cycle of an active clamp reset PWM controller is necessary to limit the voltage stress on the main and active clamp MOSFETs. The relationship between the maximum drain-source voltage of the MOSFETs and the maximum PWM duty cycle is provided by Equation 3:

$$Vds(\max) = \frac{V_{IN}}{1 - D(\max)} \tag{3}$$

The main output (OUT_A) duty cycle is normally controlled by the control current sourced into the COMP pin from the external feedback circuit. When the feedback demands maximum output from the converter, the duty cycle will be limited by one of two circuits within the LM5026: the user programmable duty cycle clamp and the voltage-dependent duty cycle limiter, which varies inversely with the input line voltage.

Programmable Duty Cycle Clamp – The maximum allowed duty cycle can be programmed by setting a voltage at the DCL pin to a value less than 2 V. The recommended method to set the DCL pin voltage is with a resistor divider connected from the RT pin to AGND. The voltage at the RT pin is internally regulated to 2 V, while the current sourced from the RT pin sets the oscillator frequency. The maximum duty can be programmed, according to Equation 4:

$$\textit{Programmable Duty Cycle Clamp} = 80\% \times \frac{RT2}{RT1 + RT2} \tag{4}$$

Feature Description (continued)

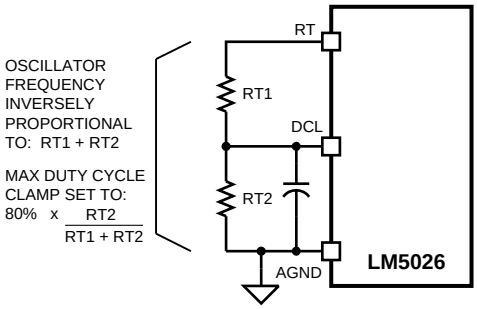


Figure 17. Programming Oscillator Frequency and Maximum Duty Cycle Clamp

Line Voltage Duty Cycle Limiter - The maximum duty cycle for the main output driver is also limited by the voltage at the UVLO pin, which is normally proportional to VIN. The controller outputs are disabled until the UVLO pin voltage exceeds 1.25 V. At the minimum operating voltage (when UVLO = 1.25 V) the maximum duty cycle starts at the duty cycle clamp level programmed by the DCL pin voltage (80% or less). As the line voltage increases, the maximum duty cycle decreases linearly with increasing UVLO voltage, as shown in Figure 18. Ultimately the duty cycle of the main output is controlled to the least of the following three variables: the duty cycle controlled by the PWM comparator, the programmable maximum duty cycle clamp, or the line voltage dependent duty cycle limiter.

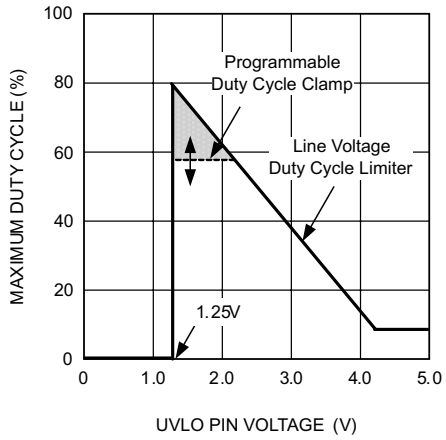


Figure 18. Maximum Duty Cycle vs UVLO Voltage

7.3.7 Soft-Start / Soft-Stop

The soft-start circuit allows the regulator to gradually reach a steady-state operating point, thereby reducing start-up stresses and current surges. Upon turnon, the SS pin capacitor is discharged by an internal switch. When the UVLO, VCC and REF pins reach their operating thresholds, the SS capacitor is released and charged with a 50-µA current source. The PWM comparator control voltage is clamped to the SS pin voltage. When the PWM input reaches 1.4 V, output pulses commence with slowly increasing duty cycle. The voltage at the SS pin eventually increases to 5 V, while the voltage at the PWM comparator increases to the value required for regulation determined by the voltage feedback loop.

If the UVLO pin voltage falls below the 1.25-V standby threshold but above the 0.4-V shutdown threshold, the 50-µA SS pin source current is disabled and a 50-µA sink current discharges the soft-start capacitor. As the SS voltage falls and clamps the PWM comparator input, the PWM duty cycle will gradually fall to zero. This soft-stop feature produces a gradual reduction of the power converter output voltage. This gradual discharge of the output filter prevents oscillations in the self-driven synchronous rectifiers on the secondary side of the converter during turnoff.

Feature Description (continued)

7.3.8 Current Sense and Current Limit

The CS input provides a control ramp for the pulse width modulator and current limit detection for overload protection. If the sensed voltage at the CS comparator exceeds 0.5 V, the present cycle is terminated (cycle-by-cycle current limit mode).

A small RC filter, located near the controller, is recommended for the CS input pin. An internal FET connected to the CS input discharges the current sense filter capacitor at the conclusion of every cycle to improve dynamic performance. This same FET remains on for an additional 100 nS at the start of each main switch cycle to attenuate the leading edge spike in the current sense signal.

The CS comparator is very fast and may respond to short duration noise pulses. Layout considerations are critical for the current sense filter and sense resistor. The capacitor associated with the CS filter must be placed very close to the device and connected directly to the pins of the LM5026 (CS and AGND pins). If a current sense transformer is used, both leads of the transformer secondary should be routed to the filter network, which should be located close to the IC. If a sense resistor located in the source of the main switch MOSFET is used for current sensing, a low inductance type of resistor is required. When designing with a current sense resistor, all of the noise-sensitive, low-power ground connections should be connected together near the AGND pin and a single connection should be made to the power ground (sense resistor ground point).

7.3.9 Overload Protection Timer

The LM5026 provides a current limit restart timer to disable the outputs and force a delayed restart (hiccup mode) if a current limit condition is repeatedly sensed. The number of cycle-by-cycle current limit events required to trigger the restart is programmable by means of an external capacitor at the RES pin. During each PWM cycle the LM5026 either sources or sinks current from the RES pin capacitor. If no current limit is detected during a cycle, a 10-µA discharge current sink is enabled to hold the RES pin at ground. If a current limit is detected, the 10-µA sink current is disabled and a 10-µA current source causes the voltage at RES pin to gradually increase. In the event of an extended overload condition, the LM5026 protects the converter with cycle-by-cycle current limiting while the voltage at RES pin increases. If the RES voltage reaches the 2.5-V threshold, the following restart sequence occurs (see Figure 19):

- The RES capacitor and SS capacitors are fully discharged.
- The soft-start current source is reduced from 50 µA to 1 µA
- The SS capacitor voltage slowly increases. When the SS voltage reaches 1.4 V, the PWM comparator will produce the first output pulse. After the first pulse occurs, the SS source current reverts to the normal 50 µA level. The SS voltage increases at its normal rate gradually increasing the duty cycle of the output drivers
- If the overload condition persists after restart, cycle-by-cycle current limiting will cause the voltage on the RES capacitor to increase again, repeating the hiccup mode sequence.
- If the overload condition no longer exists after restart, the RES pin will be held at ground by the 10-µA current sink and normal operation resumes.

The overload timer function is very versatile and can be configured for the following modes of protection:

1. **Cycle-by-cycle only:** The hiccup mode can be completely disabled by connecting the RES pin to AGND. In this configuration, the cycle-by-cycle protection will limit the output current indefinitely and no hiccup sequences will occur.
2. **Hiccup only:** The timer can be configured for immediate activation of a hiccup sequence upon detection of an overload by leaving the RES pin open circuit.
3. **Delayed Hiccup:** The most common configuration as previously described, is a programmed interval of cycle-by-cycle limiting before initiating a hiccup mode restart. The advantage of this configuration is short-term overload conditions will not cause a hiccup mode restart, however during extended overload conditions the average dissipation of the power converter will be very low.
4. **Externally Controlled Hiccup:** The RES pin can also be used as an input. By externally driving the pin to a level greater than the 2.5-V hiccup threshold, the controller will be forced into the delayed restart sequence. If the RES pin is used as an input, the driving source should be current limited to less than 5 mA. For example, the external trigger for a delayed restart sequence could come an overtemperature protection circuit.

Feature Description (continued)

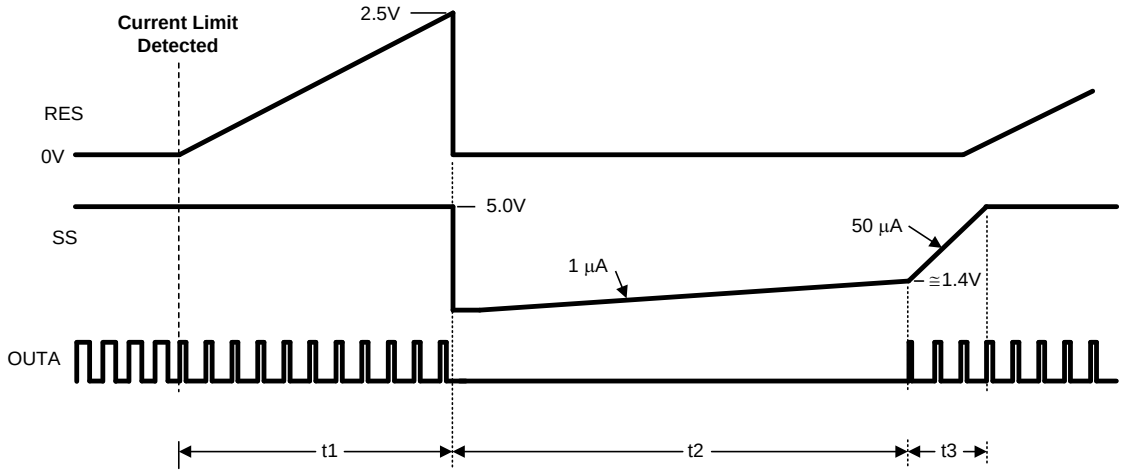


Figure 19. Hiccup Overload Restart Timing

7.3.10 Oscillator and Sync Capability

The LM5026 oscillator frequency is set by the external resistance connected between the RT pin and ground (AGND). To set a desired oscillator frequency (F) the necessary value of total R_T resistance can be calculated from Equation 5:

$$R_T = \frac{1}{F \times 167 \times 10^{-12}} \quad (5)$$

The R_T resistor(s) should be located very close to the device and connected directly to the pins of the IC (RT and AGND).

The SYNC pin can be used to synchronize the internal oscillator to an external clock. An open drain output is the recommended interface between the external clock to the LM5026 SYNC pin as illustrated in Figure 20. The clock pulse width must be greater than 15 ns. The external clock frequency must be a higher than the free running frequency set by the R_T resistance.

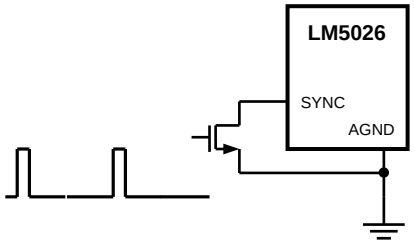


Figure 20. Sync from External Clock

Feature Description (continued)

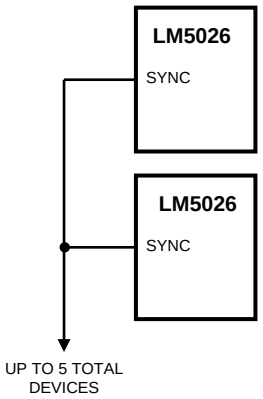


Figure 21. Sync from Multiple Devices

Multiple LM5026 devices can be synchronized together simply by connecting the devices SYNC pins together as shown in Figure 21. Take care to ensure the ground potential differences between devices are minimized. In this configuration all of the devices will be synchronized to the highest frequency device. The internal block diagram of the oscillator and synchronization circuit is shown in Figure 22. The SYNC I/O pin is a CMOS buffer with pullup current limited to 200 µA. If an external device forces the SYNC pin low before the internal oscillator ramp completes its charging cycle, the ramp will be reset and another cycle begins. If the SYNC pins of multiple LM5026 devices are connected together, the first SYNC pin that pulls low will reset the oscillator RAMP of all other devices. All controllers will operate in phase when synchronized using the SYNC I/O feature. Up to five LM5026 devices can be synchronized using this technique.

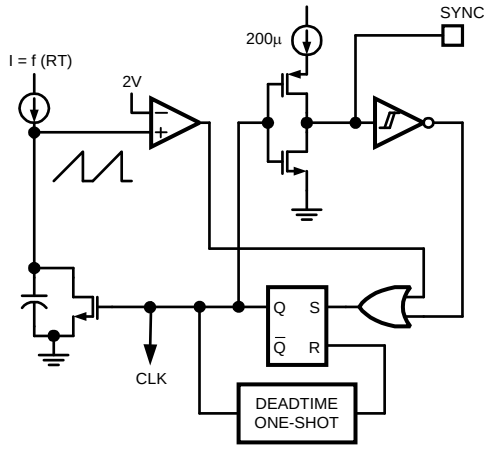


Figure 22. Oscillator Sync I/O Block Diagram

7.3.11 Thermal Protection

Internal Thermal Shutdown circuitry is provided to protect the integrated circuit in the event the maximum junction temperature is exceeded. When activated, typically at 165°C, the controller is forced into a low power standby state with the output drivers and the bias regulator disabled. The device will restart after the thermal hysteresis (typically 25°C). During thermal shutdown, the soft-start capacitor is fully discharged and the controller follows a normal start-up sequence after the junction temperature falls to the operating level.

7.4 Device Functional Modes

The LM5026 has five functional modes. Figure 23 shows the mode transition diagram.

- UVLO mode
- Soft-start mode
- Normal operation mode
- Hiccup mode
- Thermal shutdown mode

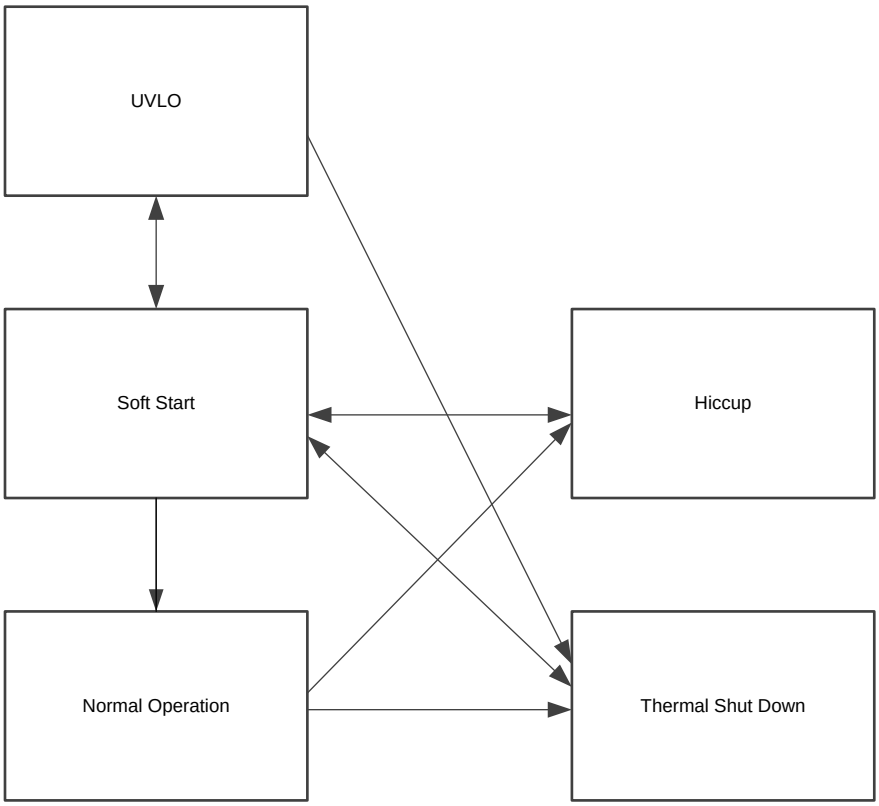


Figure 23. Mode Transition Diagram

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Line Input (VIN)

The LM5026 contains an internal high voltage start-up regulator that allows the input pin (VIN) to be connected directly to a nominal 48-V line voltage. The voltage applied to the VIN pin can vary in the range of 13 to 100 V with transient capability to 105 V. When power is applied and the UVLO pin potential is greater than 0.4 V, the VCC regulator is enabled and sources current into an external capacitor connected to the VCC pin. When the voltage on the VCC pin reaches the regulation point of 7.7 V, the internal voltage reference (REF) is enabled. The reference regulation set-point is 5 V. The controller outputs are enabled when the UVLO pin potential is greater than 1.25 V. In typical applications, an auxiliary transformer winding is connected through a diode to the VCC pin. This winding must raise the VCC voltage above 8 V to shut off the internal start-up regulator. TI recommends a filtering circuit shown in Figure 24 be used to suppress transients, which may occur at the input supply, in particular when VIN is operated close to the maximum operating rating.

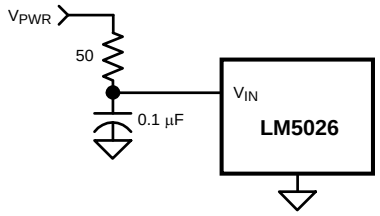


Figure 24. Input Transient Protection

8.1.2 For Application > 100 V

For applications where the system input voltage exceed 100 V or IC power dissipation is a concern, the LM5026 can be powered from an external start-up regulator as shown in Figure 25. In this configuration, the VIN and the VCC pins should be connected together, which allows the LM5026 to be operated below 13 V. The voltage at the VCC pin must be greater than 8 V yet not exceed 15 V. An auxiliary winding can be used to reduce the dissipation in the external regulator once the power converter is active.

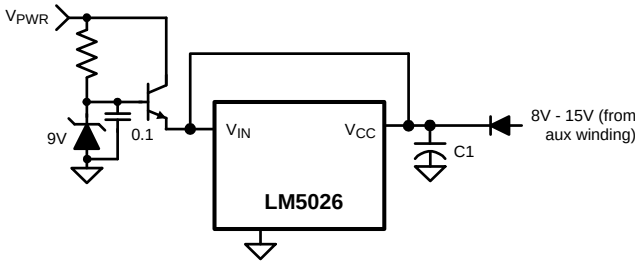


Figure 25. Start-Up Regulator for V_{PWR} >100 V

Application Information (continued)

8.1.3 Undervoltage Lockout (UVLO)

When the UVLO pin voltage is below 0.4 V, the controller is in a low current shutdown mode. When the UVLO pin voltage is greater than 0.4 V but less than 1.25 V, the controller is in standby mode. When the UVLO pin voltage is greater than 1.25 V, the controller is fully enabled. Typically, two external resistors program the minimum operational voltage for the power converter as shown in Figure 26. When UVLO pin voltage is above the 1.25-V threshold, an internal 20-µA current source is enabled to raise the voltage at the UVLO pin, thus providing threshold hysteresis. Resistance values for R1 and R2 can be determined from Equation 6 and Equation 7:

$$R1 = \frac{V_{HYS}}{20\,\mu A} \tag{6}$$

where

- V_{HYS} is the desired UVLO hysteresis at V_{PWR}

$$R2 = \frac{1.25 \times R1}{V_{PWR} - 1.25} \tag{7}$$

where

- V_{PWR} is the desired turnon voltage

For example, if the LM5026 is to be enabled when V_{PWR} reaches 33 V, and disabled when V_{PWR} is decreased to 30 V, R1 calculates to 150 kΩ, and R2 calculates to 5.9 kΩ. The voltage at the UVLO pin should not exceed 6 V at any time. Be sure to check both the power and voltage rating for the selected R1 resistor.

Remote configuration of the controller's operational modes can be accomplished with open drain device(s) connected to the UVLO pin as shown in Figure 27.

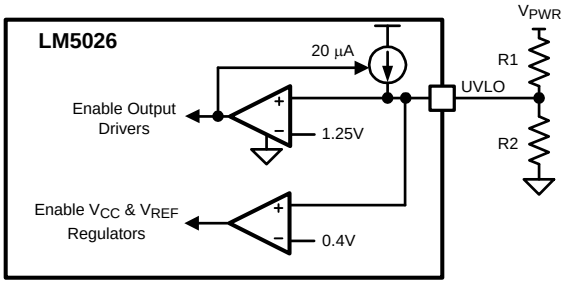


Figure 26. Basic UVLO Configuration

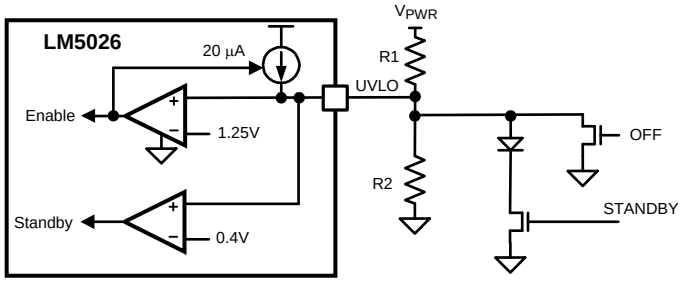


Figure 27. Remote Standby and Disable Control

Application Information (continued)

8.1.4 Oscillator (RT, SYNC)

Oscillator (RT, SYNC) The oscillator frequency is generally selected in conjunction with the design of the system magnetic components along with the volume and efficiency goals for a given power converter design. The total RT resistance at the RT pin sets the oscillator frequency. The RT resistors should be one of the first components placed and connected when designing the PCB. Direct, short connections to each side of the RT resistors (RT, DCL and AGND pins) are recommended .

The SYNC pin can be used to synchronize the internal oscillator to an external clock. An open-drain output is the recommended interface from the external clock to the SYNC pin. The clock pulse width should be greater than 15 ns. The external clock must be a **higher frequency** than the free-running frequency set by the RT resistor. Multiple LM5026 devices can be synchronized together simply by connecting the devices SYNC pins together. Take care to ensure the ground potential differences between devices are minimized. In this configuration all of the devices will be synchronized to the highest frequency device.

8.1.5 Voltage Feedback (COMP)

The COMP pin is designed to accept the voltage loop feedback error signal from the regulated output through an error amplifier and (typically) an optocoupler. In a typical configuration, VOUT is compared to a precision reference voltage by the error amplifier. The output of the amplifier drives the optocoupler, which in turn drives the COMP pin. The parasitic capacitance of the optocoupler often limits the achievable loop bandwidth for a given power converter. The optocoupler LED and detector junction capacitance produce a low-frequency pole in the voltage regulation loop. The LM5026 current controlled optocoupler interface (COMP) previously described, greatly increases the pole frequency associated with the optocoupler.

8.1.6 Current Sense (CS)

The CS pin receives an input signal representative of the transformer primary current, either from a current sense transformer (Figure 28) or from a resistor in series with the source of the primary switch (Figure 29). In both cases the sensed current creates a ramping voltage across R1, while the R_F/C_F filter suppresses noise and transients. R1, R_F and C_F should be as physically close to the LM5026 as possible, and the ground connection from the current sense transformer, or R1, should be a dedicated track to the AGND pin. The current-sense components must provide > 0.5 V at the CS pin when an overcurrent condition exists.

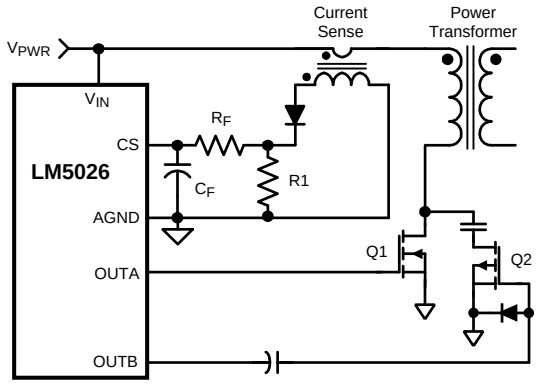


Figure 28. Current Sense Using a Current-Sense Transformer

Application Information (continued)

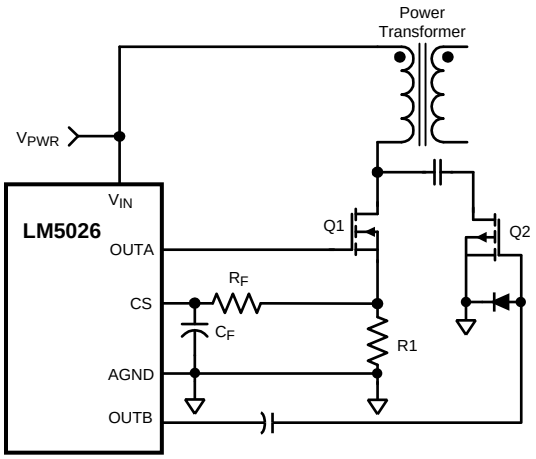


Figure 29. Current Sense Using a Source-Sense Resistor (R1)

8.1.7 Hiccup Mode Current Limit Restart (RES)

The basic operation of the hiccup mode current limit restart is described in the functional description. The delay time to restart is programmed with the selection of the RES pin capacitor C_{RES} as shown in Figure 19. In the case of continuous cycle-by-cycle current limit detection at the CS pin, the time required for C_{RES} to reach the 2.5-V hiccup mode threshold is calculated by Equation 8 :

$$t1 = \frac{C_{RES} \times 2.5}{10 \mu A} = 2.5 \times 10^5 \times C_{RES} \quad (8)$$

For example, if C_{RES} = 0.01 µF, the time t1 is approximately 2.5 ms.

The cool down time, t2 is set by the soft-start capacitor (C_{SS}) and the internal 1-µA SS current source, and is equal to Equation 9:

$$t2 = \frac{C_{SS} \times 1.4V}{1 \mu A} = 1.4 \times 10^6 \times C_{SS} \quad (9)$$

If C_{SS} = 0.01 µF, t2 is approximately 14 ms.

The soft-start time t3 is set by the internal 50-µA current source, and is equal to Equation 10:

$$t3 = \frac{C_{SS} \times 3.5V}{50 \mu A} = 7 \times 10^4 \times C_{SS} \quad (10)$$

The time t2 provides a periodic cool-down time for the power converter in the event of a sustained overload or short circuit. This results in lower average input current and lower power dissipated within the power components. It is recommended that the ratio of t2/(t1 + t3) be in the range of 5 to 10 to make good use of this feature. If the application requires no delay from the first detection of a current limit condition to the onset of the hiccup mode (t1 = 0), the RES pin can be left open (no external capacitor). If it is desired to disable the hiccup mode current limit operation, the RES pin should be connected to ground (AGND).

8.1.8 Soft-Start (SS)

An internal current source and an external soft-start capacitor determines the time required for the output duty cycle to increase from zero to its final value for regulation. The minimum acceptable time is dependent on the output capacitance and the response of the feedback loop. If the soft-start time is too quick, the output could overshoot its intended voltage before the feedback loop can regulate the PWM controller. After power is applied and the controller is fully enabled, the voltage at the SS pin ramps up as C_{SS} is charged by an internal 50-µA current source. The voltage at the output of the COMP pin current mirror is clamped to the same potential as the SS pin by a voltage buffer with a sink-only output stage. When the SS voltage reaches approximately 1.4 V, PWM pulses appear at the driver output with very low duty cycle. The PWM duty cycle gradually increases as the voltage at the SS pin charges to approximately 5.0 V.

Application Information (continued)

8.1.9 Voltage-Dependent Maximum Duty Cycle

As the input source V_{PWR} increases the voltage at the UVLO pin increases proportionately. To limit the Volt × Seconds applied to the transformer, the maximum allowed PWM duty cycle decreases as the UVLO voltage increases. If it is desired to increase the slope of the voltage limited duty cycle characteristic, two possible configurations are shown in Figure 30. After the LM5026 is enabled, the zener diode causes the UVLO pin voltage to increase more rapidly with increasing input voltage (V_{PWR}). The voltage dependent maximum duty cycle clamp varies with the UVLO pin voltage according to Equation 11:

$$\text{Voltage-Dependent Duty Cycle (\%)} = 107 - 21.8 \times \text{UVLO} \quad (11)$$

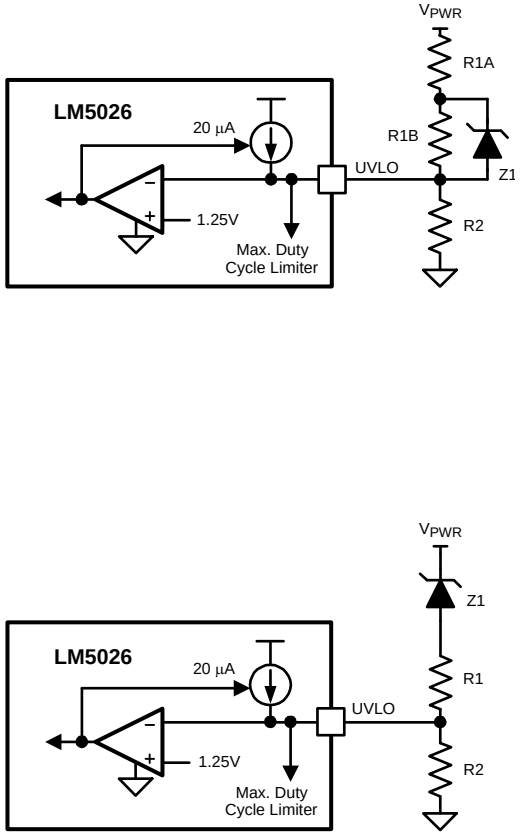


Figure 30. Altering the Slope of Duty Cycle vs V_{PWR}

8.1.9.1 Programmable Maximum Duty Cycle Clamp (DCL)

When the UVLO pin is biased at 1.25 V (minimum operating level), the maximum duty cycle of OUT_A is limited by the duty cycle of the internal clock signal. The duty cycle of the internal clock can be adjusted by programming a voltage set at the DCL pin. The default maximum duty cycle (80%) can be selected by connecting the DCL pin to the RT pin. The DCL pin should not be left open. A small decoupling capacitor located close to the DCL pin is recommended.

The oscillator frequency set resistance (R_T) must be determined first before programming the maximum duty cycle. Following the selection of the total R_T resistance, the ratio of the R_T resistors can be designed to set the desired maximum duty cycle. As the UVLO pin voltage increases from 1.25 V, the maximum duty cycle is reduced by the voltage dependent duty cycle limiter previously as described and shown in Figure 18.

8.2 Typical Application

The following schematic shows an example of an LM5026 controlled 100-W active clamp forward power converter. The input voltage range (V_{PWR}) is 36 V to 78 V, and the output voltage is 3.3 V. The output current capability is 30 Amps. Current sense transformer T2 provides information to the CS pin for current mode control and current limit protection. The error amplifiers and reference U3 and U4 provide voltage feedback through optocoupler U2. Synchronous rectifiers Q3-Q6 minimize rectification losses in the secondary. An auxiliary winding on inductor L2 provides power to the LM5026 VCC pin when the output is in regulation. The input voltage UVLO levels are approximately 34 V for increasing V_{PWR}, and ≈32 V for decreasing V_{PWR}. The circuit can be shut down by forcing the ON/OFF input (J2) below 1.25 V. An external synchronizing frequency can be applied to the SYNC input (J11) or like converters can be self-synchronized by connections of (J3). The regulator output is current limited at approximately 32 A.

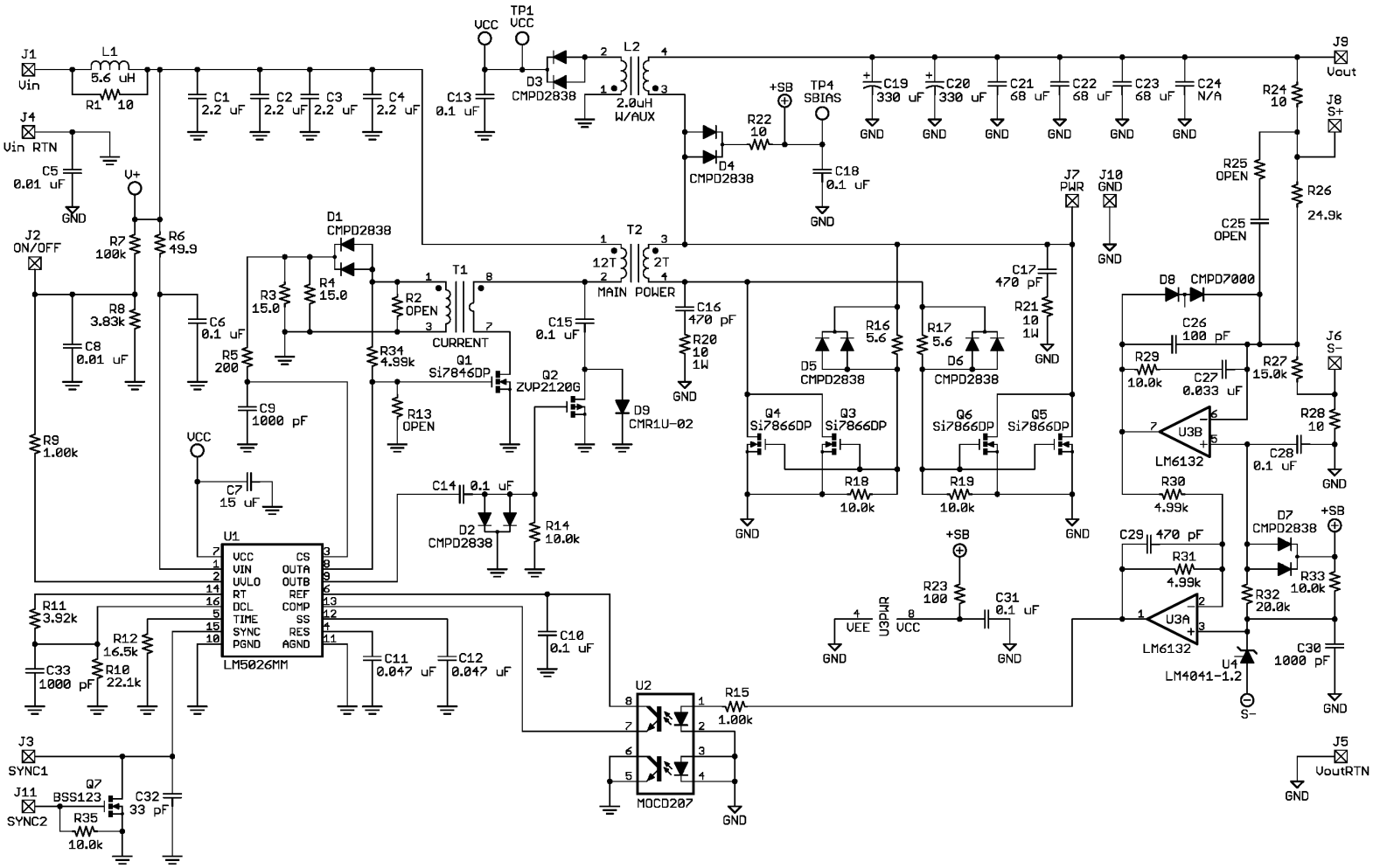


Figure 31. Application Circuit: Input 36 V to 78 V, Output 3.3 V, 30 A

8.2.1 Design Requirements

The design requirements of this application are as follows:

- Input range: 36 V to 78 V
- Output voltage: 3.3 V
- Output current: 0 to 30 A
- Measured efficiency: 90% at 30 A, 92.5% at 15 A
- Frequency of operation: 230 kHz
- Board size: 2.3 × 2.4 × 0.5 inches
- Load Regulation: 1%
- Line Regulation: 0.1%
- Line UVLO, Hiccup Current Limit

8.2.2 Detailed Design Procedure

8.2.2.1 Determine VIN Configuration

First, determine the input voltage range of the application. If the maximum input voltage is less than 100 V, use VIN pin connection in Figure 24. If the maximum input voltage exceeds 100 V, use the configuration shown in Figure 25.

8.2.2.2 Determine UVLO Configuration

As described in *Undervoltage Lockout (UVLO)*, two external resistors program the minimum operational voltage for the power converter. Use Equation 6 and Equation 7 to calculate the resistor values. If remote standby and disable control is needed, use the configuration in Figure 27.

8.2.2.3 Configure Operating Frequency

If internal oscillator is used, use Equation 5 to determine the RT resistor value. If external clock is used, use the configuration in Figure 20.

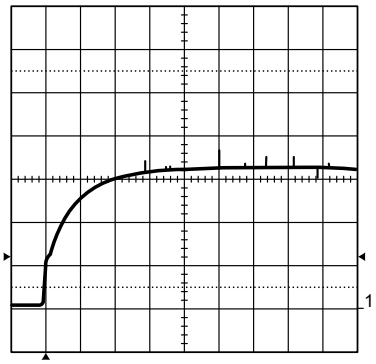
8.2.2.4 Configure Hiccup Mode and Soft Start

The delay time to restart is programmed with the selection of the RES pin capacitor. Soft-start time is programmed by the capacitor on SS pin. Refer to *Hiccup Mode Current Limit Restart (RES)* and Equation 8, Equation 9, and Equation 10 to determine the capacitor values.

8.2.2.5 Determine Deadtime and Maximum Duty Cycle

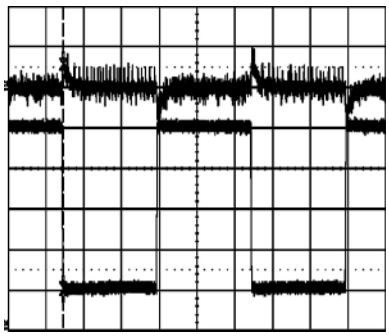
The PWM output phasing the timing is shown in Figure 14. Use Equation 1 and Equation 2 to determine the deadtime programming resistor value. Maximum duty cycle clamp is determined by DCL pin voltage. Use Equation 4 and Figure 17 to determine RT1 and RT2 values.

8.2.3 Application Curves



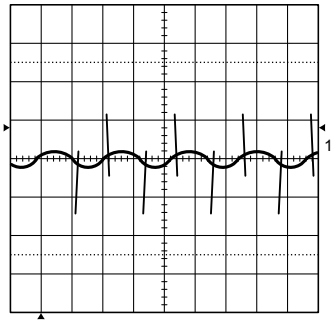
Input Voltage = 48VDC
Output Current = 5 A
Trace 1: Output Voltage V/div = 1 V
Horizontal Resolution = 1 ms/div

Figure 32. Output Voltage



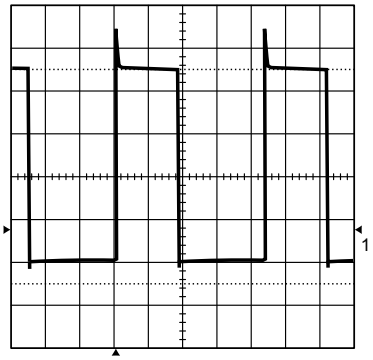
Input Voltage = 48VDC
Output Current = 5 A to 25 A
Trace 1: Output Voltage V/div = 0.5 V
Trace 2: Output Current, A/div = 5 V
Horizontal Resolution = 1 ms/div

Figure 33. Transient Response



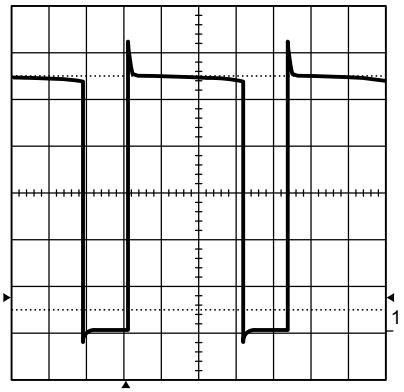
Input Voltage = 48VDC
Output Current = 30 A
Bandwidth Limit = 25 MHz
Trace 1: Output Voltage V/div = 50 mV
Horizontal Resolution = 2 µs/div

Figure 34. Typical Output Ripple



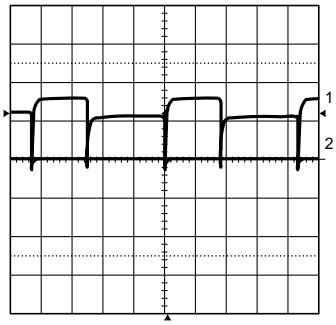
Input Voltage = 38VDC
Output Current = 25 A
Trace 1: Q1 Drain Voltage V/div = 20 V
Horizontal Resolution = 1 µs/div

Figure 35. Drain Voltage of Q1



Input Voltage = 78VDC
Output Current = 25 A
Trace 1: Q1 Drain Voltage V/div = 20 V
Horizontal Resolution = 1 µs/div

Figure 36. Drain Voltage of Q1



Input Voltage = 48VDC
Output Current = 5 A
Synchronous Rectifier, Q3 Gate V/div = 5 V Trance 1
Synchronous Rectifier, Q3 Gate V/div = 5 V Trance 2
Synchronous Rectifier, Q5 Gate V/div = 5 V
Horizontal Resolution = 1 µs/div

Figure 37. Gate Voltages

9 Power Supply Recommendations

VCC pin is the power supply for the device. There should be a 0.1-µF to 100-µF capacitor directly from VCC to ground. REF pin should be bypassed to ground as close as possible to the device using a 0.1-µF capacitor.

10 Layout

10.1 Layout Guidelines

The LM5026 current-sense and PWM comparators are very fast, and respond to short duration noise pulses. The components at the CS, COMP, SS, DCL, UVLO, TIME, SYNC and the RT pins should be as physically close as possible to the IC, thereby minimizing noise pick-up on the PCB tracks.

Layout considerations are critical for the current-sense filter. If a current-sense transformer is used, both leads of the transformer secondary should be routed to the sense filter components and to the IC pins. The ground side of each transformer should be connected through a dedicated PCB track to the AGND pin, rather than through the ground plane.

If the current-sense circuit employs a sense resistor in the drive transistor source, low inductance resistor should be used. In this case, all the noise-sensitive, low-current ground tracks should be connected in common near the IC, and then a single connection made to the power ground (sense resistor ground point). The gate drive outputs of the LM5026 should have short direct paths to the power MOSFETs in order to minimize inductance in the PCB traces.

The two ground pins (AGND, PGND) must be connected together with a short direct connection to avoid jitter due to relative ground bounce.

If the internal dissipation of the LM5026 produces high junction temperatures during normal operation, the use of multiple vias under the IC to a ground place can help conduct heat away from the IC. Judicious positioning of the PCB within the end product, along with use of any available air flow (forced or natural convection) can help reduce the junction temperatures.

10.2 Layout Example

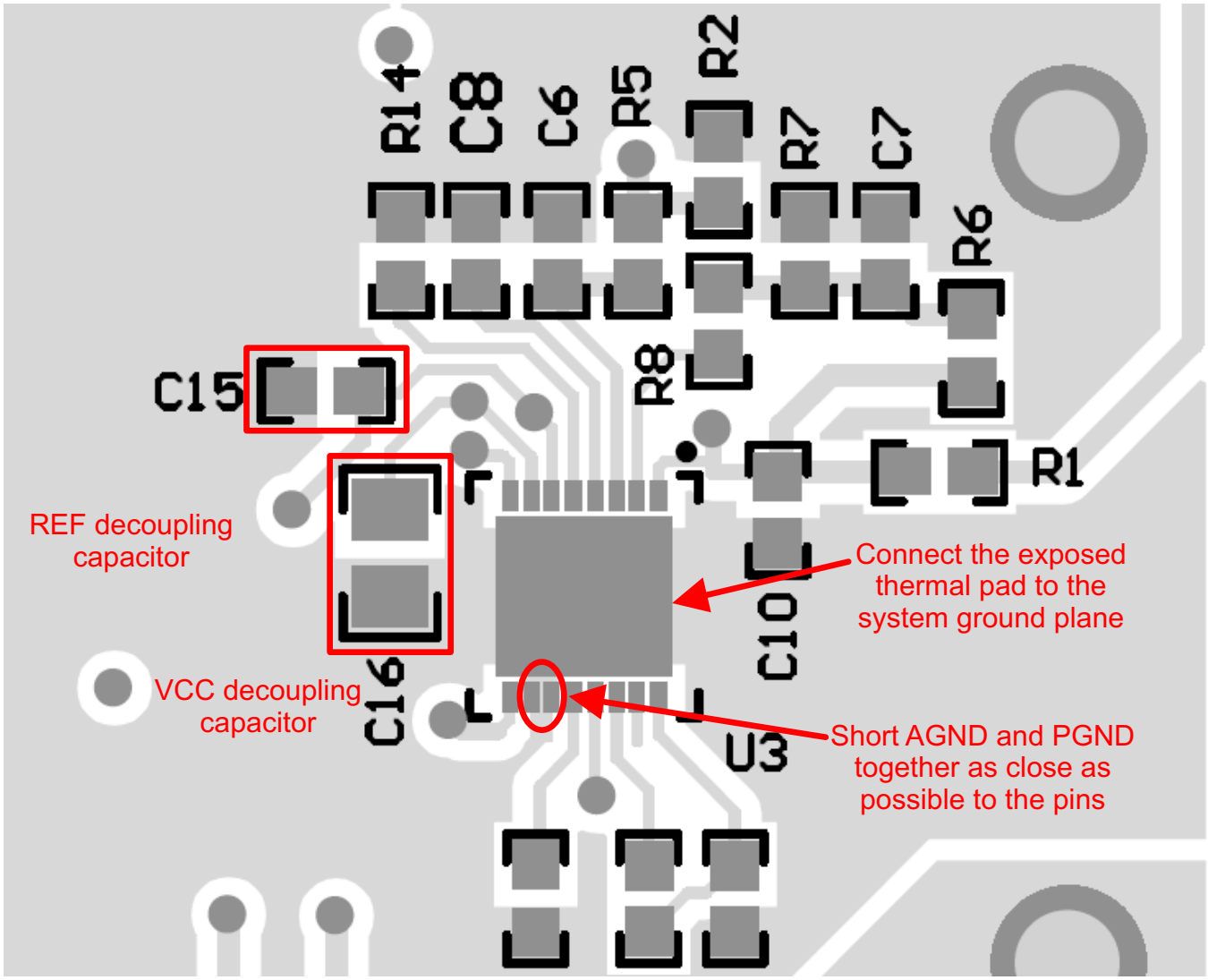


Figure 38. Layout Example

11 Device and Documentation Support

11.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM5026MT	NRND	TSSOP	PW	16	92	Non-RoHS & Green	Call TI	Level-1-260C-UNLIM	-40 to 125	LM5026 MT	
LM5026MT/NOPB	ACTIVE	TSSOP	PW	16	92	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	LM5026 MT	Samples
LM5026MTX/NOPB	ACTIVE	TSSOP	PW	16	2500	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	LM5026 MT	Samples
LM5026SD/NOPB	ACTIVE	WSON	NHQ	16	1000	RoHS & Green	SN	Level-1-260C-UNLIM		5026SD	Samples
LM5026SDX/NOPB	ACTIVE	WSON	NHQ	16	4500	RoHS & Green	SN	Level-1-260C-UNLIM		5026SD	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

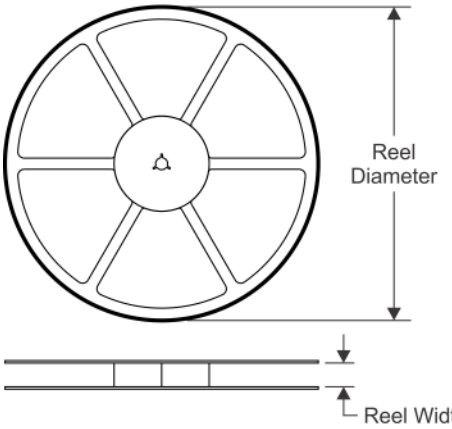
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

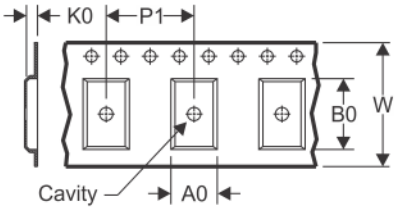
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

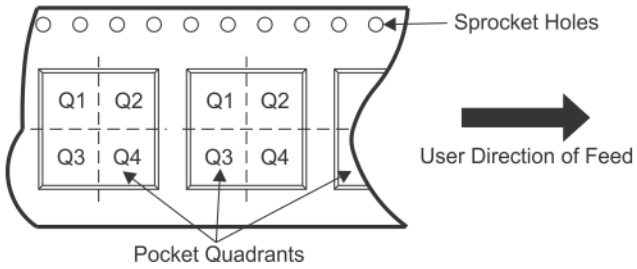


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

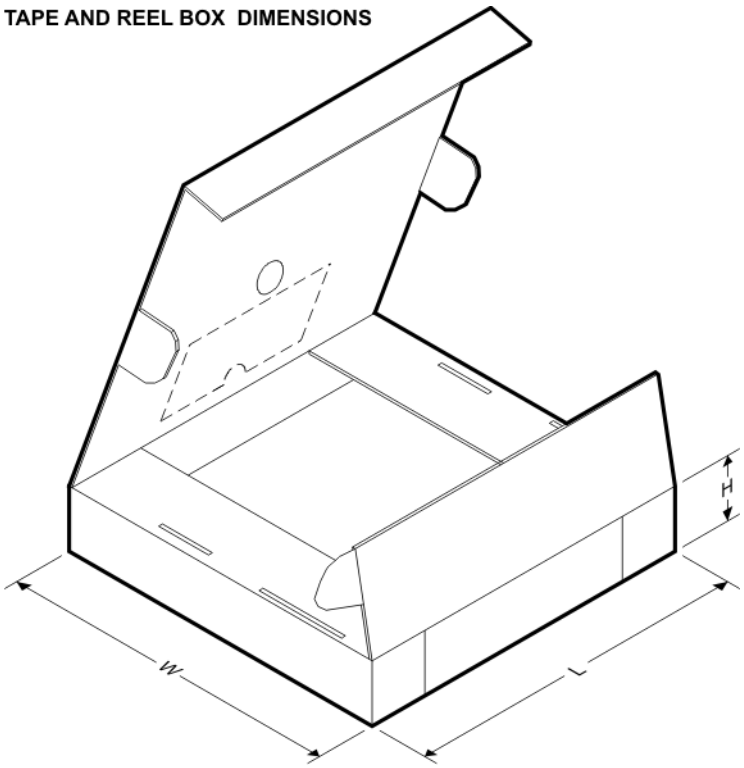
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM5026MTX/NOPB	TSSOP	PW	16	2500	330.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1
LM5026SD/NOPB	WSON	NHQ	16	1000	178.0	12.4	5.3	5.3	1.3	8.0	12.0	Q1
LM5026SDX/NOPB	WSON	NHQ	16	4500	330.0	12.4	5.3	5.3	1.3	8.0	12.0	Q1

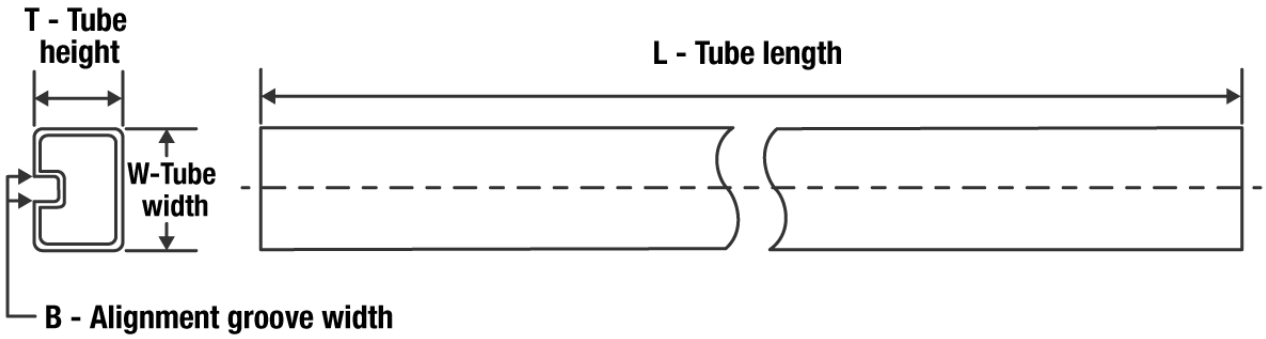
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM5026MTX/NOPB	TSSOP	PW	16	2500	367.0	367.0	35.0
LM5026SD/NOPB	WSON	NHQ	16	1000	208.0	191.0	35.0
LM5026SDX/NOPB	WSON	NHQ	16	4500	367.0	367.0	35.0

TUBE

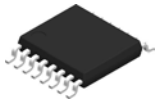


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LM5026MT	PW	TSSOP	16	92	495	8	2514.6	4.06
LM5026MT	PW	TSSOP	16	92	495	8	2514.6	4.06
LM5026MT/NOPB	PW	TSSOP	16	92	530	10.2	3600	3.5
LM5026MT/NOPB	PW	TSSOP	16	92	495	8	2514.6	4.06

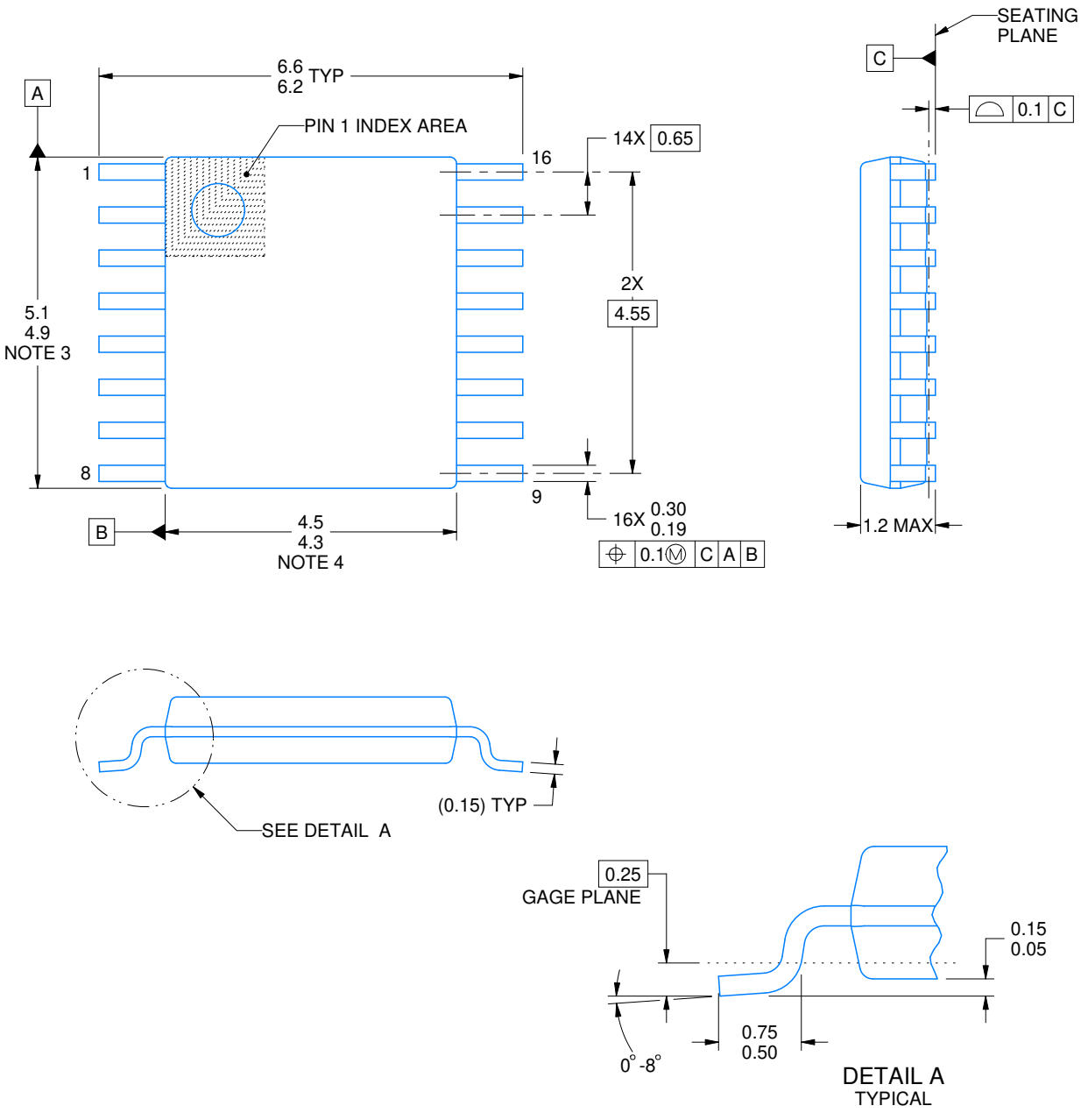
PACKAGE OUTLINE

PW0016A



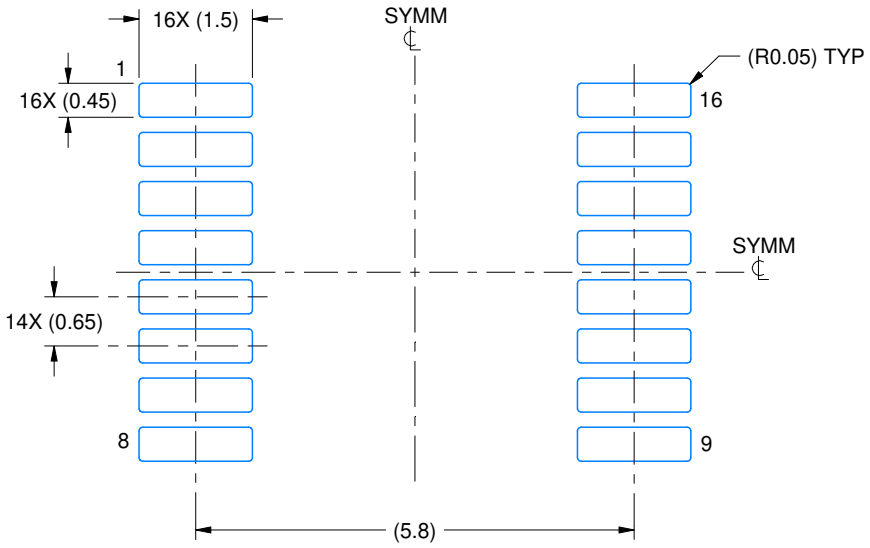
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

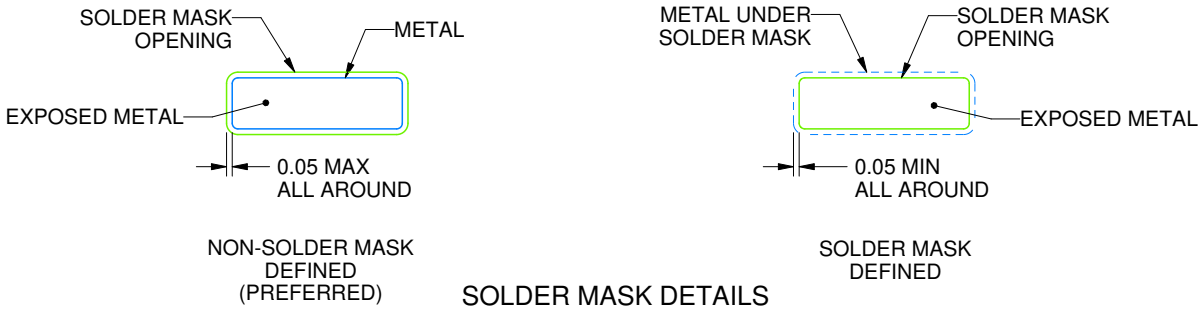


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

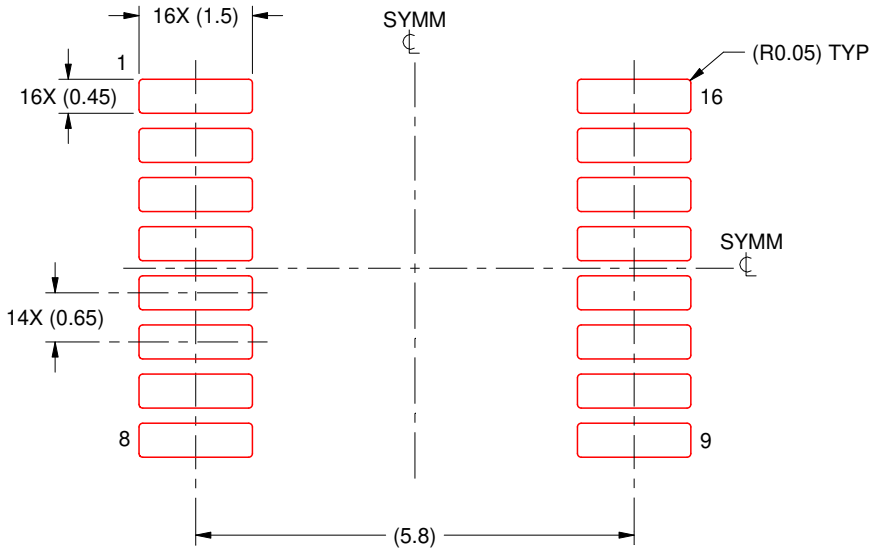


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



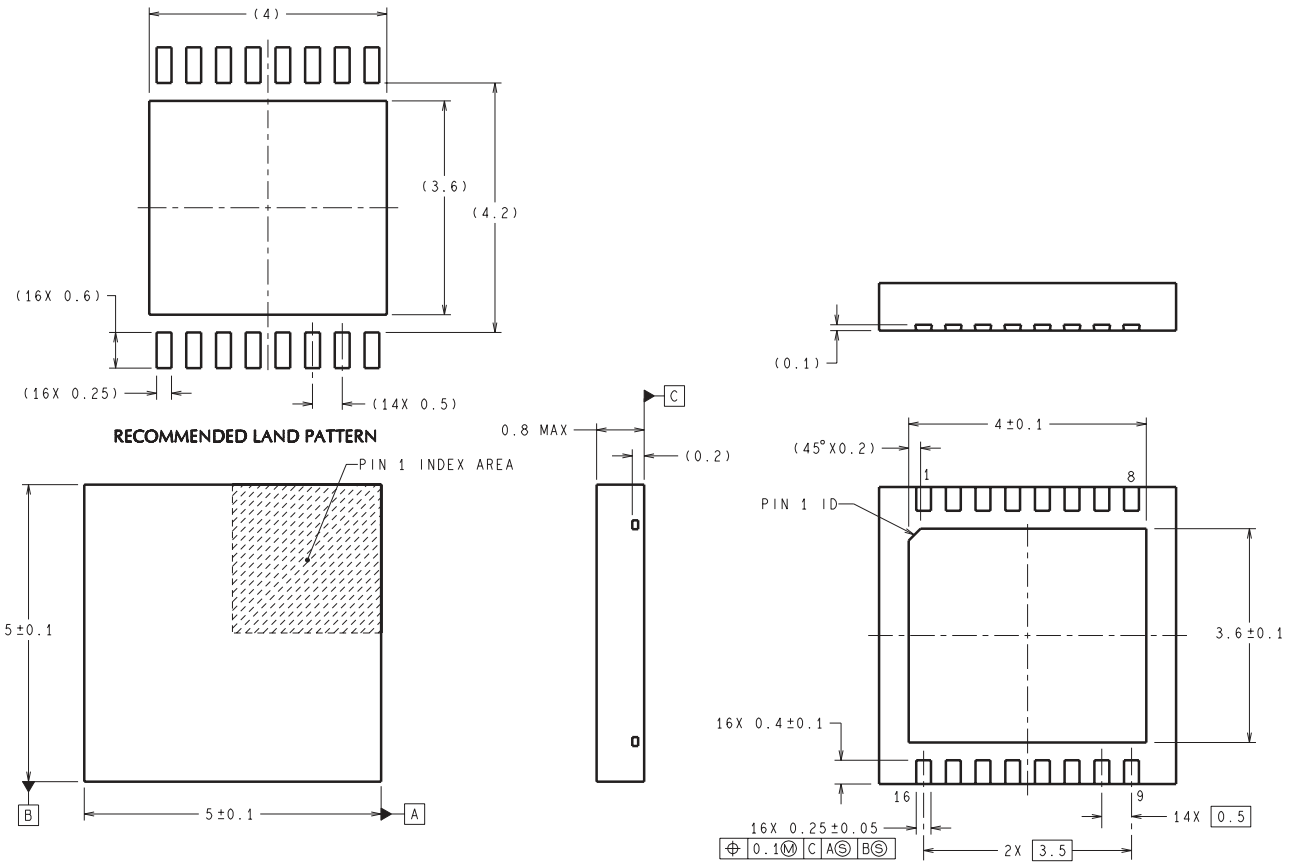
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

NHQ0016A



DIMENSIONS ARE IN MILLIMETERS

SDA16A (Rev A)

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