30V, 0.007 Ohm, 35A, N-Channel UltraFET® Trench Power MOSFET

UltraFET® Trench from Fairchild is a new advanced MOSFET technology that achieves the lowest possible on-resistance per silicon area while maintaining fast switching and low gate charge. The reduced conduction and switching losses extend battery life in notebook PCs, cellular telephones and other portable information appliances and improve the overall efficiency of high frequency DC-DC converters used to power the latest microprocessors.

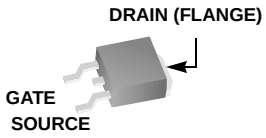
UltraFET® Trench

Features

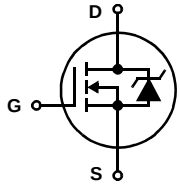
- $r_{DS(ON)}$ = 0.006Ω Typical, V_{GS} = 10V
- Q_g Total 85nC Typical, V_{GS} = 10V
- Q_{gd} 16nC Typical
- C_{ISS} 5600pF Typical

Packaging

ISL9N2357D3ST
JEDEC TO-252AA



Symbol



Ordering Information

PART NUMBER	PACKAGE	BRAND
ISL9N2357D3ST	TO-252AA	N2357D

NOTE: When ordering, use the entire part number.
e.g., ISL9N2357D3ST.

Absolute Maximum Ratings T_C = 25°C, Unless Otherwise Specified

SYMBOL	PARAMETER	ISL9N2357D3ST	UNITS
V_{DSS}	Drain to Source Voltage (Note 1)	30	V
V_{DGR}	Drain to Gate Voltage (R_{GS} = 20kΩ) (Note 1)	30	V
V_{GS}	Gate to Source Voltage	±20	V
	Drain Current		
I_D	Continuous (T_C = 25°C, V_{GS} = 10V) (Figure 2)	35	A
I_D	Continuous (T_C = 100°C, V_{GS} = 10V)	35	A
I_{DM}	Pulsed Drain Current	Figure 4	A
P_D	Power Dissipation	100	W
	Derate Above 25°C	0.67	W/°C
T_J, T_{STG}	Operating and Storage Temperature	-55 to 175	°C
	Maximum Temperature for Soldering		
T_L	Leads at 0.063in (1.6mm) from Case for 10s	300	°C
T_{pkg}	Package Body for 10s, See Techbrief TB334	260	°C
THERMAL SPECIFICATIONS			
$R_{\theta JC}$	Thermal Resistance Junction to Case, TO-252	1.5	°C/W
$R_{\theta JA}$	Thermal Resistance Junction to Ambient TO-252	100	°C/W

NOTE:

1. T_J = 25°C to 150°C.

CAUTION: *Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
OFF STATE SPECIFICATIONS							
Drain to Source Breakdown Voltage	BV_{DSS}	I_D = 250µA, V_{GS} = 0V (Figure 9)		30	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 25V, V_{GS} = 0V		-	-	1	µA
		V_{DS} = 25V, V_{GS} = 0V, $T_C = 150^oC$		-	-	250	µA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±20V		-	-	±100	nA
ON STATE SPECIFICATIONS							
Gate to Source Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250µA (Figure 8)		2	-	4	V
Drain to Source ON Resistance	$r_{DS(ON)}$	I_D = 35A, V_{GS} = 10V (Figure 7)		-	0.006	0.007	Ω
SWITCHING SPECIFICATIONS (V_{GS} = 10V)							
Turn-On Time	t_{ON}	V_{DD} = 15V, I_D = 20A V_{GS} = 10V, R_{GS} = 9.1Ω (Figures 14, 15)		-	-	144	ns
Turn-On Delay Time	$t_{d(ON)}$			-	27	-	ns
Rise Time	t_r			-	69	-	ns
Turn-Off Delay Time	$t_{d(OFF)}$			-	84	-	ns
Fall Time	t_f			-	53	-	ns
Turn-Off Time	t_{OFF}			-	-	207	ns
GATE CHARGE SPECIFICATIONS							
Total Gate Charge at 20V	$Q_{g(TOT)}$	V_{GS} = 0V to 20V	V_{DD} = 15V, I_D = 20A, $I_{g(REF)}$ = 1.0mA (Figures 11, 12, 13)	-	172	258	nC
Total Gate Charge at 10V	$Q_{g(10)}$	V_{GS} = 0V to 10V		-	85	130	nC
Threshold Gate Charge	$Q_{g(TH)}$	V_{GS} = 0V to 2V		-	11	17	nC
Gate to Source Gate Charge	Q_{gs}			-	23	-	nC
Gate to Drain “Miller” Charge	Q_{gd}			-	16	-	nC
CAPACITANCE SPECIFICATIONS							
Input Capacitance	C_{ISS}	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz (Figure 10)		-	5600	-	pF
Output Capacitance	C_{OSS}			-	526	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	355	-	pF

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	V_{SD}	I_{SD} = 20A	-	-	1.25	V
		I_{SD} = 10A	-	-	1.0	V
Reverse Recovery Time	t_{rr}	I_{SD} = 20A, dI_{SD}/dt = 100A/µs	-	-	34	ns
Reverse Recovered Charge	Q_{RR}	I_{SD} = 20A, dI_{SD}/dt = 100A/µs	-	-	29	nC

Typical Performance Curves

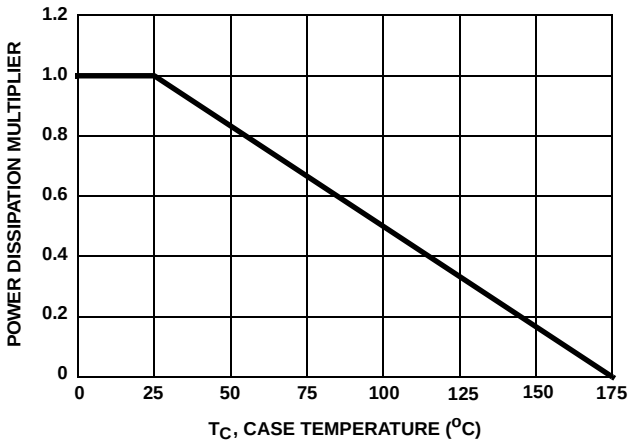


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

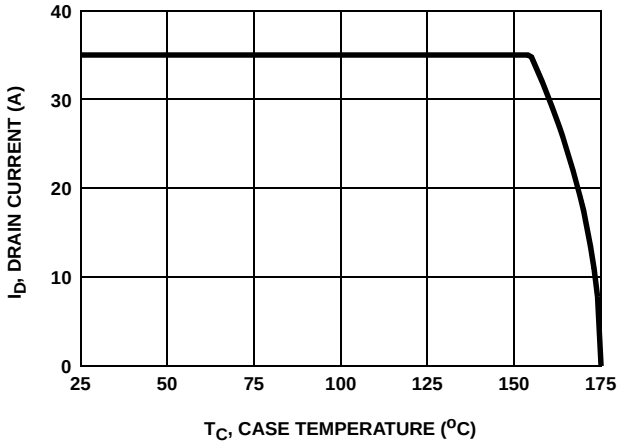


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

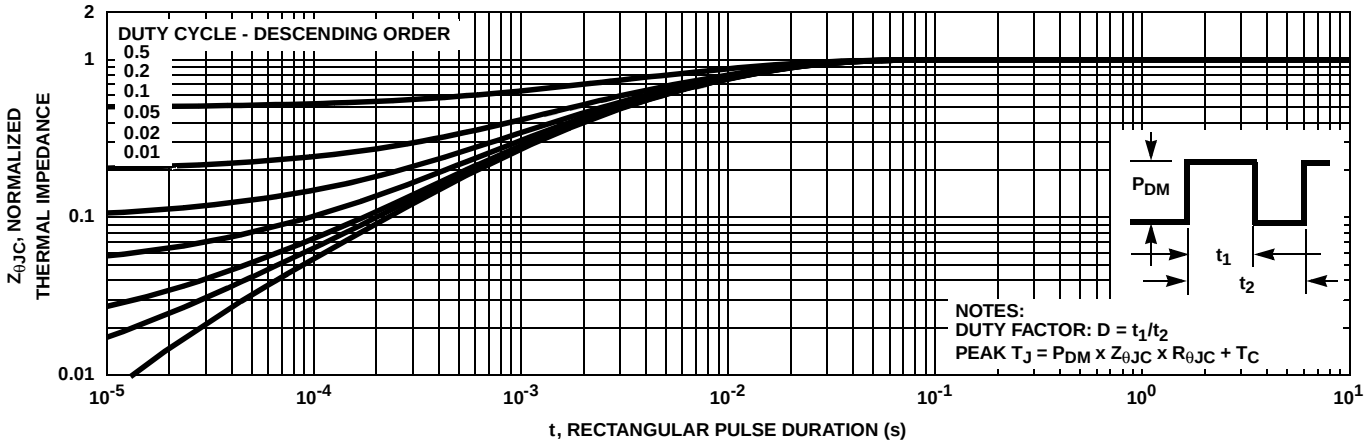


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

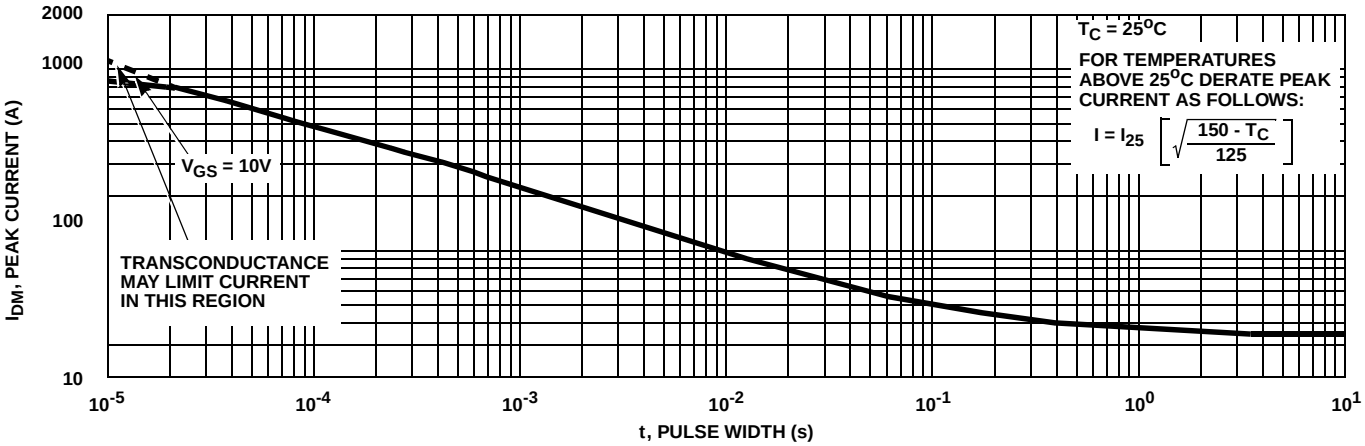


FIGURE 4. PEAK CURRENT CAPABILITY

Typical Performance Curves (Continued)

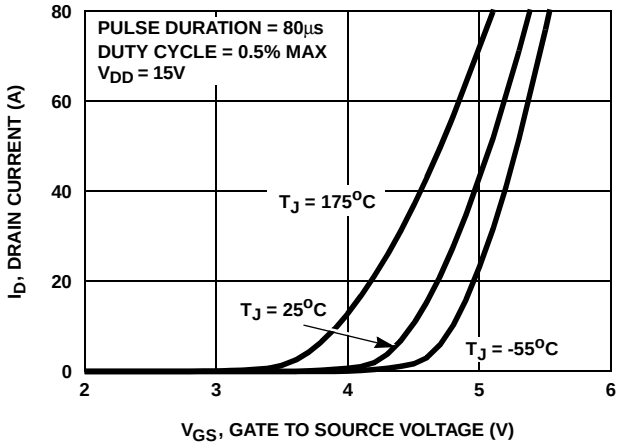


FIGURE 5. TRANSFER CHARACTERISTICS

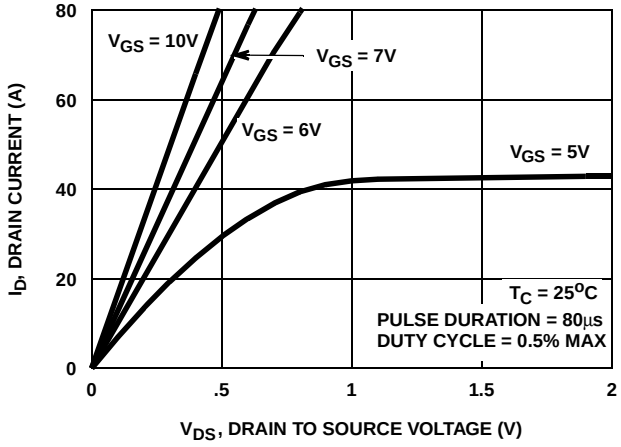


FIGURE 6. SATURATION CHARACTERISTICS

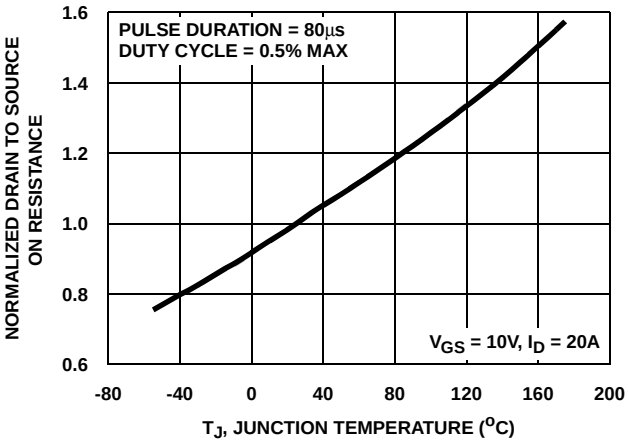


FIGURE 7. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

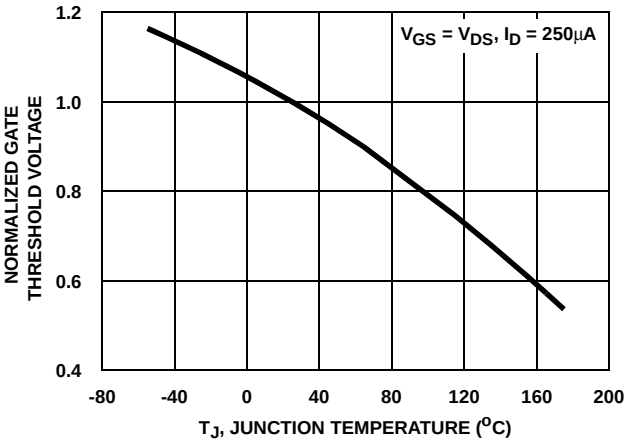


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

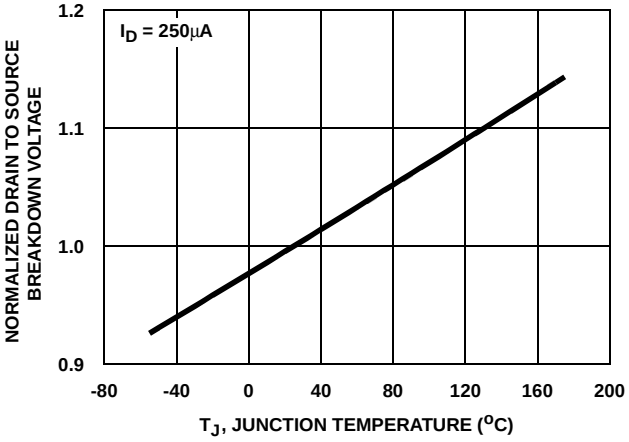


FIGURE 9. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

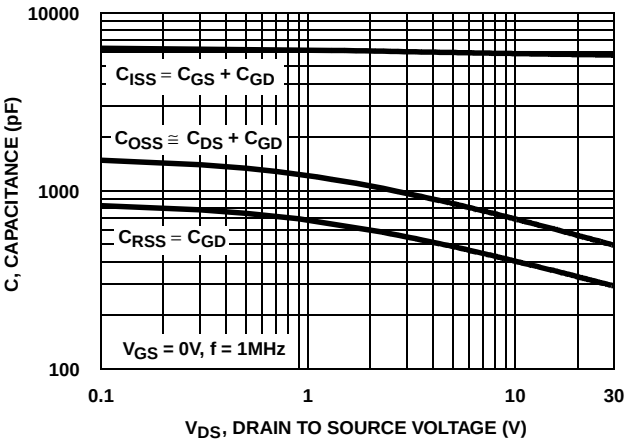
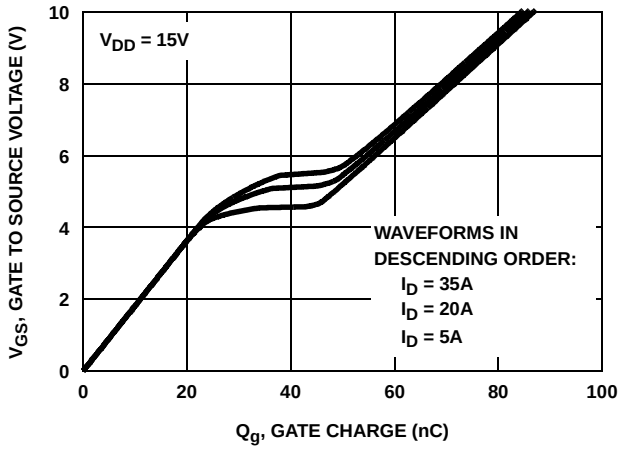


FIGURE 10. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE

Typical Performance Curves (Continued)



NOTE: Refer to Fairchild Application Notes AN7254 and AN7260.

FIGURE 11. GATE CHARGE WAVEFORMS FOR CONSTANT GATE CURRENT

Test Circuits and Waveforms

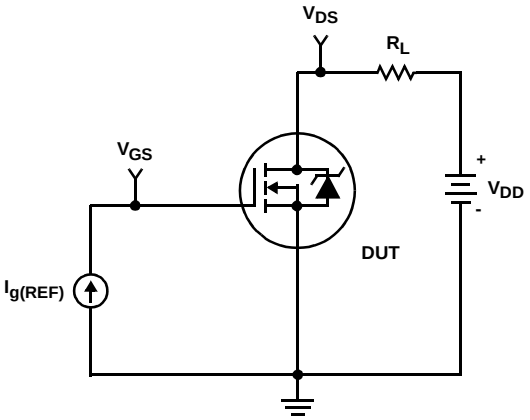


FIGURE 12. GATE CHARGE TEST CIRCUIT

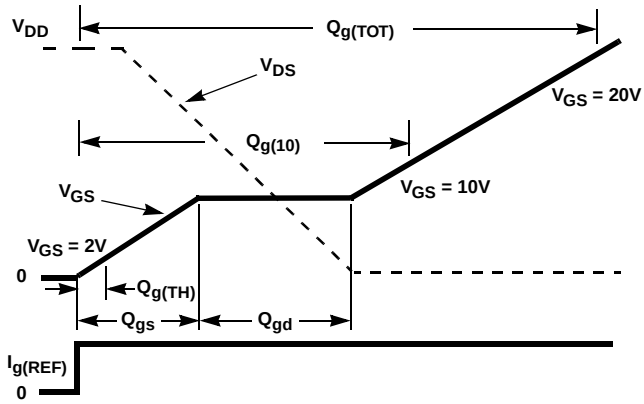


FIGURE 13. GATE CHARGE WAVEFORMS

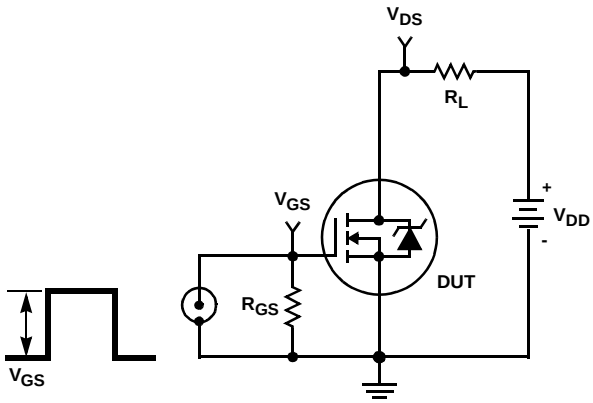


FIGURE 14. SWITCHING TIME TEST CIRCUIT

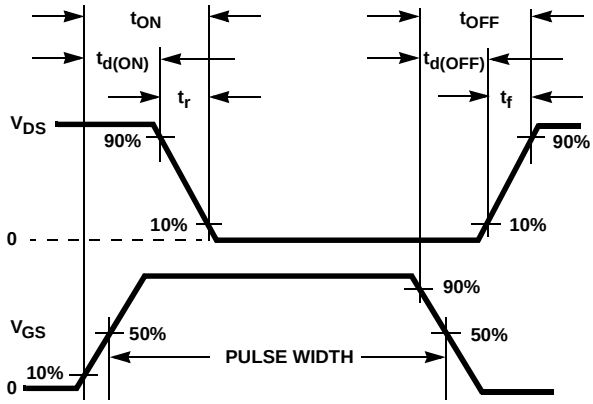


FIGURE 15. SWITCHING TIME WAVEFORM

PSPICE Electrical Model

.SUBCKT ISL9N2357 2 1 3 ; rev Aug 2000

CA 12 8 2.5e-9
CB 15 14 2.1e-9
CIN 6 8 5.2e-9

DBODY 7 5 DBODYMOD
DBREAK 5 11 DBREAKMOD
DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 33.39
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 6 10 6 8 1
EVTHRES 6 21 19 8 1
EVTEMP 20 6 18 22 1

IT 8 17 1

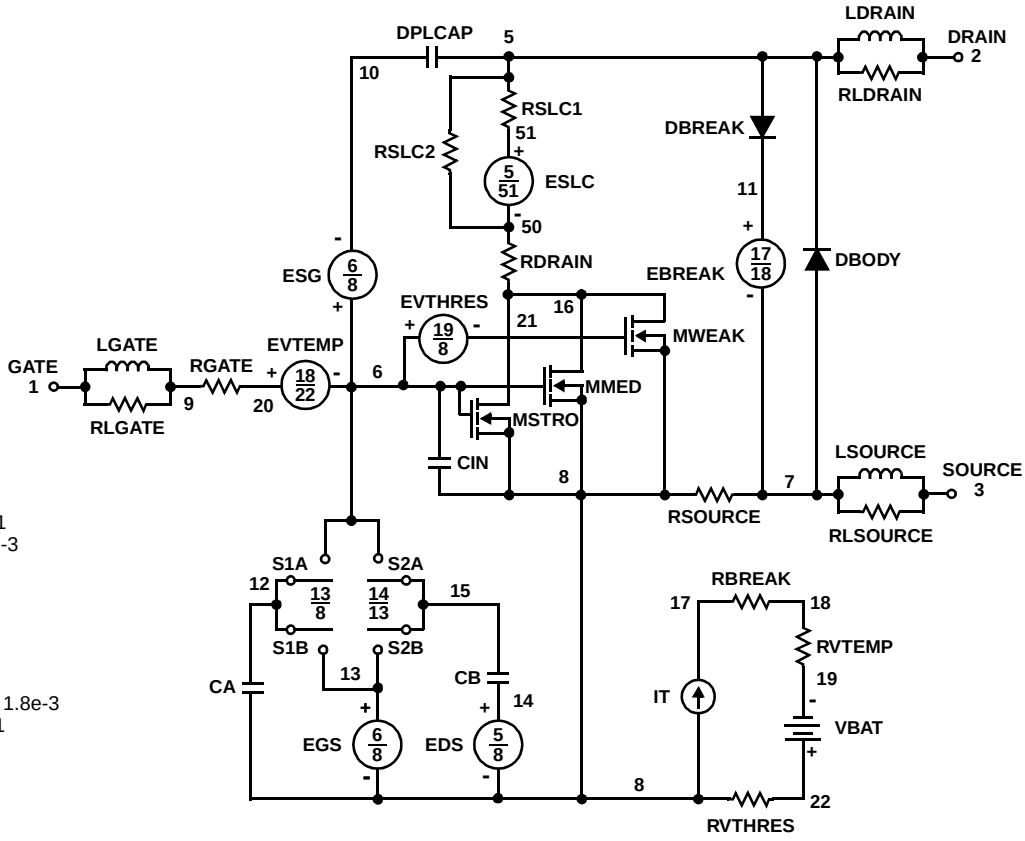
LDRAIN 2 5 1.0e-9
LGATE 1 9 4.3e-9
LSOURCE 3 7 1.6e-9

MMED 16 6 8 8 MMEDMOD
MSTRO 16 6 8 8 MSTROMOD
MWEAK 16 21 8 8 MWEAKMOD

RBREAK 17 18 RBREAKMOD 1
RDRAIN 50 16 RDRAINMOD 2.8e-3
RGATE 9 20 1.68
RLDRAIN 2 5 10
RLGATE 1 9 43
RLSOURCE 3 7 16
RSLC1 5 51 RSLCMOD 1e-6
RSLC2 5 50 1e3
RSOURCE 8 7 RSOURCEMOD 1.8e-3
RVTHRES 22 8 RVTHRESMOD 1
RVTEMP 18 19 RVTEMPMOD 1

S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

VBAT 22 19 DC 1



ESLC 51 50 VALUE={(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)/(1e-6*550),3))}

.MODEL DBODYMOD D (IS = 1.01e-12 RS = 3.5e-3 ikf = 15 TRS1 = 1.01e-3 TRS2 = 1.21e-6 CJO = 6.8e-10 TT = 6.7e-9 M = 0.35)
.MODEL DBREAKMOD D (RS = 0.068 TRS1 = 1.12e-3 TRS2 = 1.25e-6)
.MODEL DPLCAPMOD D (CJO = 8.5e-10 IS = 1e-30 N = 10 M = 0.31)
.MODEL MMEDMOD NMOS (VTO = 3.5 KP = 6.0 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 1.68)
.MODEL MSTROMOD NMOS (VTO = 4.1 KP = 110 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)
.MODEL MWEAKMOD NMOS (VTO = 3.0 KP = 0.03 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 16.8 RS = 0.1)
.MODEL RBREAKMOD RES (TC1 = 1.01e-3 TC2 = 1.07e-7)
.MODEL RDRAINMOD RES (TC1 = 4.5e-3 TC2 = 8.0e-6)
.MODEL RSLCMOD RES (TC1 = 1.02e-4 TC2 = -1.13e-6)
.MODEL RSOURCEMOD RES (TC1 = 1.0e-3 TC2 = 1e-6)
.MODEL RVTHRESMOD RES (TC1 = -3.0e-3 TC2 = -1.5e-5)
.MODEL RVTEMPMOD RES (TC1 = -4.0e-3 TC2 = 1.25e-6)

.MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -6.0 VOFF= -1.5)
.MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -1.5 VOFF= -6.0)
.MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -0.7 VOFF= 0)
.MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 0 VOFF= -0.7)

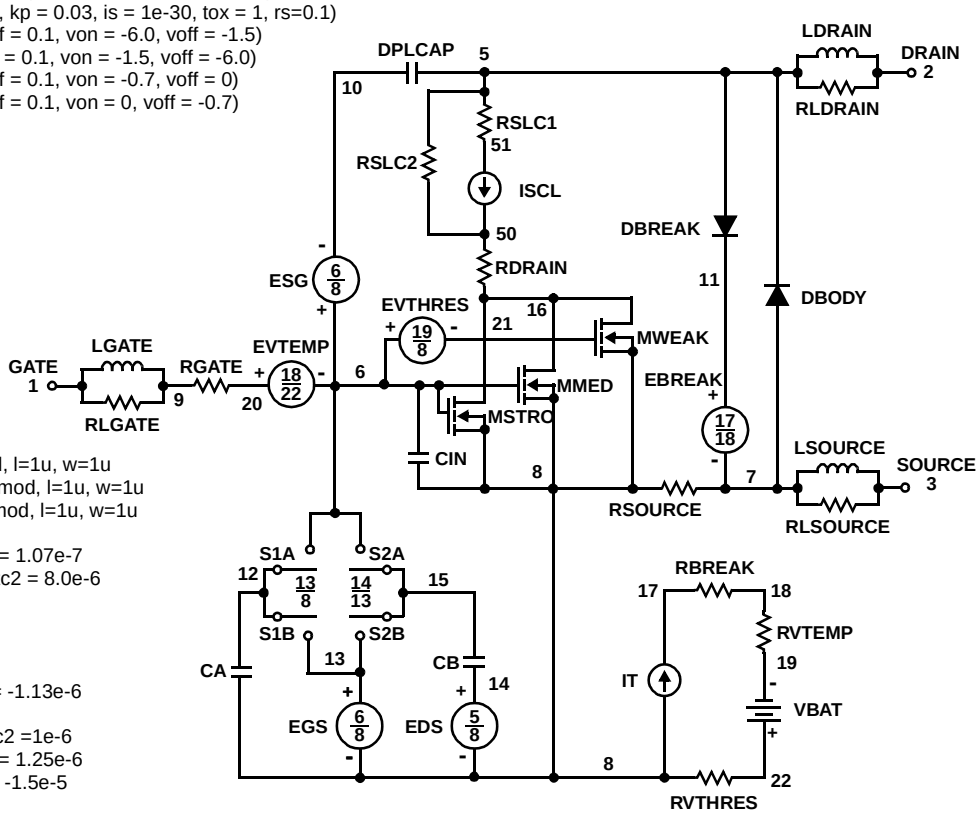
.ENDS

NOTE: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.

SABER Electrical Model

REV Aug 2000

```
template ISL9N2357 n2,n1,n3
electrical n2,n1,n3
{
var i iscl
dp..model dbodymod =  (isl = 1.01e-12, rs = 3.5e-3, ikf=15, trs1 = 1.01e-3, trs2 = 1.21e-6, cjo = 6.8e-10, tt = 6.7e-9, m = 0.35)
dp..model dbreakmod = (rs = 0.068, trs1 = 1.12e-3, trs2 = 1.25e-6)
dp..model dplcapmod =  (cjo = 8.5e-10, isl = 10e-30, nl=10, m = 0..31)
m..model mmedmod = (type=_n, vto = 3.5, kp = 6.0, is = 1e-30, tox = 1)
m..model mstrongmod = (type=_n, vto = 4.1, kp = 110, is = 1e-30, tox = 1)
m..model mweakmod = (type=_n, vto = 3.0, kp = 0.03, is = 1e-30, tox = 1, rs=0.1)
sw_vcsp..model s1amod =  (ron = 1e-5, roff = 0.1, von = -6.0, voff = -1.5)
sw_vcsp..model s1bmod =  (ron =1e-5, roff = 0.1, von = -1.5, voff = -6.0)
sw_vcsp..model s2amod =  (ron = 1e-5, roff = 0.1, von = -0.7, voff = 0)
sw_vcsp..model s2bmod =  (ron = 1e-5, roff = 0.1, von = 0, voff = -0.7)

c.ca n12 n8 = 2.5e-9
c.cb n15 n14 = 2.1e-9
c.cin n6 n8 = 5.5e-9

dp.dbody n7 n5 = model=dbodymod
dp.dbreak n5 n11 = model=dbreakmod
dp.dplcap n10 n5 = model=dplcapmod

i.it n8 n17 = 1

l.ldrain n2 n5 = 1.0e-9
l.lgate n1 n9 = 4.3e-9
l.lsource n3 n7 = 1.6e-9

m.mmed n16 n6 n8 n8 = model=mmedmod, l=1u, w=1u
m.mstrong n16 n6 n8 n8 = model=mstrongmod, l=1u, w=1u
m.mweak n16 n21 n8 n8 = model=mweakmod, l=1u, w=1u

res.rbreak n17 n18  = 1, tc1 = 1.01e-3, tc2 = 1.07e-7
res.rdrain n50 n16  = 2.8e-3, tc1 = 4.5e-3, tc2 = 8.0e-6
res.rgate n9 n20 = 1.68
res.rldrain n2 n5 = 10
res.rlgate n1 n9 = 43
res.rlsource n3 n7 = 16
res.rslc1 n5 n51= 1e-6, tc1 = 1.02e-4, tc2 = -1.13e-6
res.rslc2 n5 n50 = 1e3
res.rsource n8 n7  = 1.8e-3, tc1 = 1.0e-3, tc2 =1e-6
res.rvtemp n18 n19  = 1, tc1 = -4.0e-3, tc2 = 1.25e-6
res.rvthres n22 n8  = 1, tc1 = -3.0e-3, tc2 = -1.5e-5

spe.ebreak n11 n7 n17 n18 = 33.39
spe.eds n14 n8 n5 n8 = 1
spe.egs n13 n8 n6 n8 = 1
spe.esg n6 n10 n6 n8 = 1
spe.evtemp n20 n6 n18 n22 = 1
spe.evthres n6 n21 n19 n8 = 1

sw_vcsp.s1a n6 n12 n13 n8 = model=s1amod
sw_vcsp.s1b n13 n12 n13 n8 = model=s1bmod
sw_vcsp.s2a n6 n15 n14 n13 = model=s2amod
sw_vcsp.s2b n13 n15 n14 n13 = model=s2bmod

v.vbat n22 n19 = dc=1

equations {
i (n51->n50) +=iscl
iscl: v(n51,n50) = ((v(n5,n51)/(1e-9+abs(v(n5,n51))))*((abs(v(n5,n51)*1e6/550))** 3))
}
}
```



SPICE Thermal Model

REV 23March 2000

ISL9N2357T

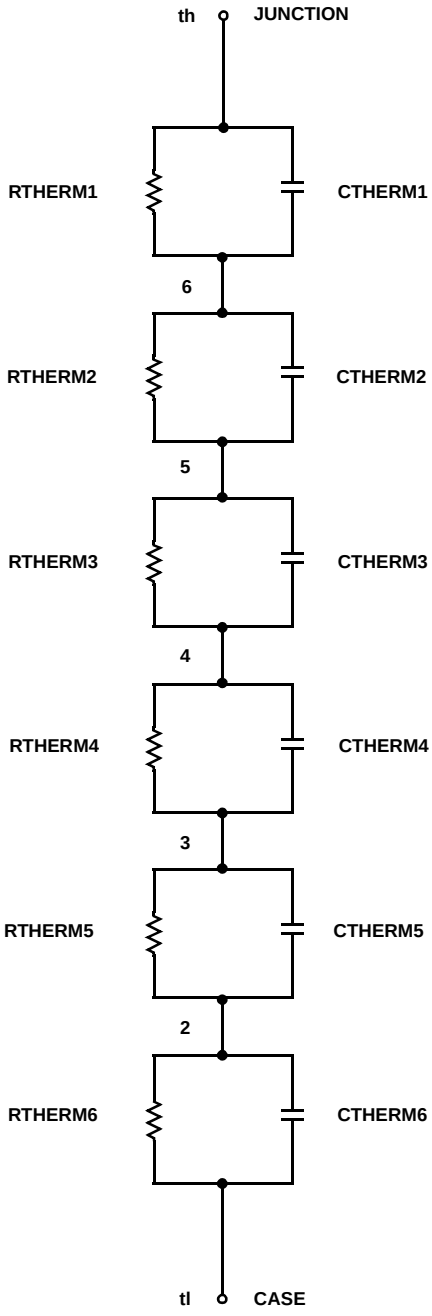
CTHERM1 th 6 3.0e-3
CTHERM2 6 5 4.0e-3
CTHERM3 5 4 4.8e-3
CTHERM4 4 3 5.2e-3
CTHERM5 3 2 8.5e-3
CTHERM6 2 tl 5.0e-2

RTHERM1 th 6 3.5e-3
RTHERM2 6 5 8.5e-3
RTHERM3 5 4 5.7e-2
RTHERM4 4 3 2.5e-1
RTHERM5 3 2 4.3e-1
RTHERM6 2 tl 4.5e-1

SABER Thermal Model

SABER thermal model ISL9N2357T

```
template thermal_model th tl
thermal_c th, tl
{
ctherm.ctherm1 th 6 = 3.0e-3
ctherm.ctherm2 6 5 = 4.0e-3
ctherm.ctherm3 5 4 = 4.8e-3
ctherm.ctherm4 4 3 = 5.2e-3
ctherm.ctherm5 3 2 = 8.5e-3
ctherm.ctherm6 2 tl = 5.0e-2

rtherm.rtherm1 th 6 = 3.5e-3
rtherm.rtherm2 6 5 = 8.5e-3
rtherm.rtherm3 5 4 = 5.7e-2
rtherm.rtherm4 4 3 = 2.5e-1
rtherm.rtherm5 3 2 = 4.3e-1
rtherm.rtherm6 2 tl = 4.5e-1
}
```



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CoolFET™	FRFET™	OPTOPLANAR™	SPM™	VCX™
CROSSVOLT™	GlobalOptoisolator™	PACMAN™	STAR*POWER™	
DenseTrench™	GTO™	POP™	Stealth™	
DOME™	HiSeC™	Power247™	SuperSOT™-3	
EcoSPARK™	I^2C™	PowerTrench ®	SuperSOT™-6	
E^2CMOS^{TM}	ISOPLANAR™	QFET™	SuperSOT™-8	
$EnSigna^{TM}$	LittleFET™	QS™	SyncFET™	
FACT™	MicroFET™	QT Optoelectronics™	TinyLogic™	
FACT Quiet Series™	MicroPak™	Quiet Series™	TruTranslation™	

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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.