NCP1580

Low Voltage Synchronous Buck Controller

The NCP1580 is a voltage mode PWM controller designed to operate from a 5.0 V or 12 V supply and produce an output voltage as low as 0.8 V. This 8−pin device provides an optimal level of integration to reduce size and cost of the power supply. The NCP1580 has a fixed 350 kHz oscillator and soft−start function. The NCP1580 provides a 1.5 A floating gate driver design to drive N−Channel MOSFETs in a synchronous configuration. Adaptive non−overlap circuitry reduces switching losses by preventing simultaneous conduction of both outputs. Protection features include thermal shutdown and undervoltage lockout (UVLO). The NCP1580 is available in an 8−pin SOIC package.

Features

- Input Voltage Range from 4.5 V to 13.2 V
- 350 kHz Internal Oscillator
- Boost Pin Operates to 26.5 V
- Voltage Mode PWM Control
- 0.8 V ± 1.5% Internal Reference Voltage
- Adjustable Output Voltage
- Internal Soft−Start
- Internal 1.5 A Gate Drivers
- Adaptive Non−Overlap Circuit
- 90% Max Duty Cycle
- Input UVLO
- Overtemperature Protection
- Fully Specified over −40°C to 85°C
- Pb−Free Package is Available

Applications

- Graphics Cards
- Desktop Computers
- Servers/Networking
- DSP and FPGA Power Supply
- DC−DC Regulator Modules

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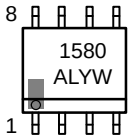
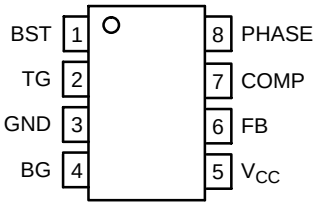
MARKING DIAGRAM

SOIC−8
D SUFFIX
CASE 751



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
NCP1580DR2	SOIC−8	2500/Tape & Reel
NCP1580DR2G	SOIC−8 (Pb−Free)	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

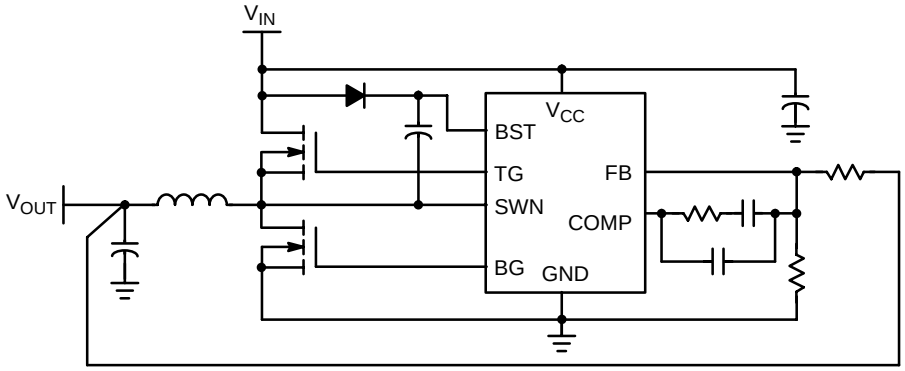


Figure 1. Typical Application Diagram

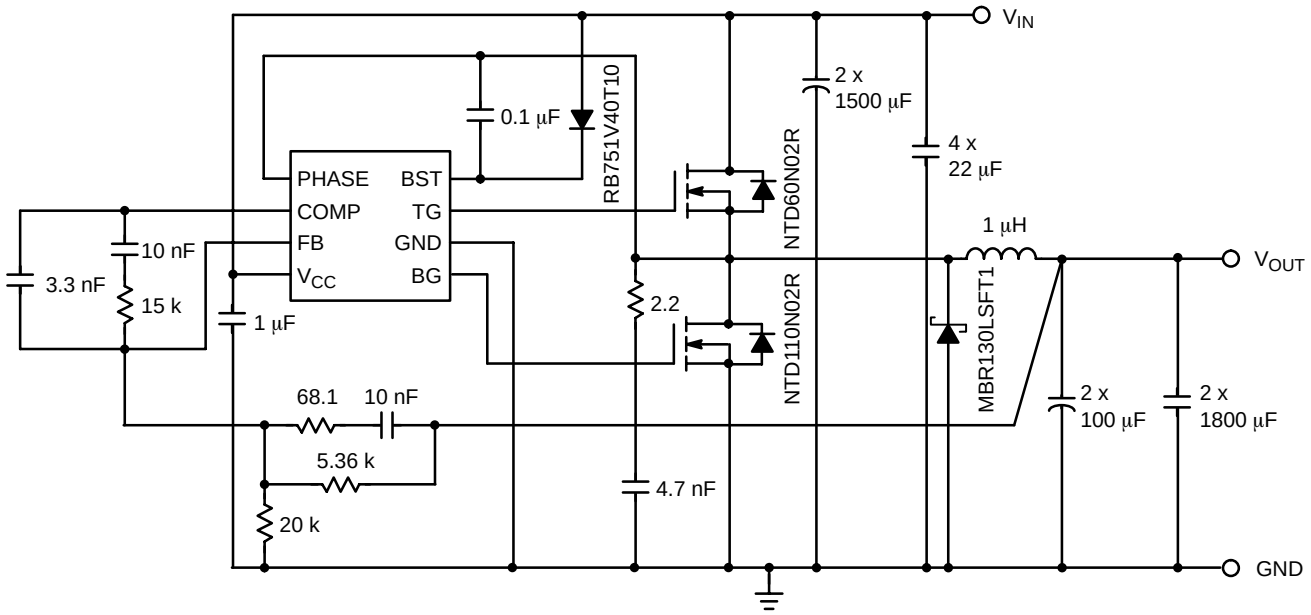


Figure 2. Application Diagram; 12 V Input, 1.0 V at 20 A Output

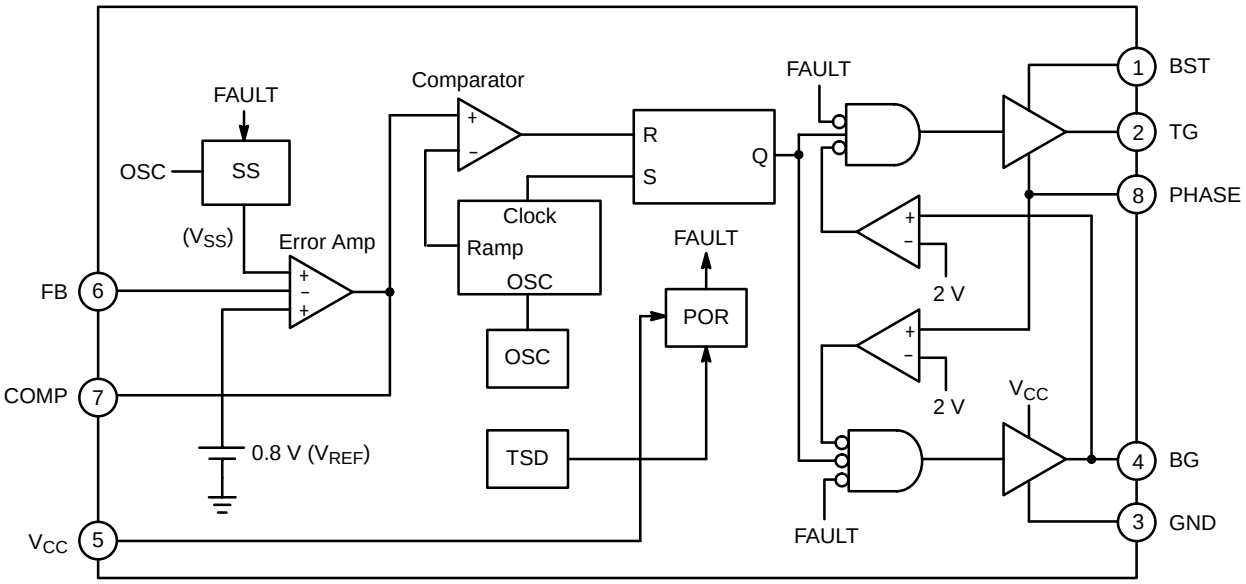


Figure 3. Detailed Block Diagram

PIN FUNCTION DESCRIPTION

Pin No.	Symbol	Description
1	BST	Supply rail for the floating top gate driver. To form a boost circuit, use an external diode to bring the desired input voltage to this pin (cathode connected to BST pin). Connect a capacitor (C_{BST}) between this pin and the PHASE pin. Typical values for C_{BST} range from 0.1 μF to 1 μF. Ensure that C_{BST} is placed near the IC.
2	TG	Top gate MOSFET driver pin. Connect this pin to the gate of the top N−Channel MOSFET.
3	GND	IC ground reference. All control circuits are referenced to this pin.
4	BG	Bottom gate MOSFET driver pin. Connect this pin to the gate of the bottom N−Channel MOSFET.
5	V_{CC}	Supply rail for the internal circuitry. Operating supply range is 4.5 V to 13.2 V. Decouple with a 1 μF capacitor to GND. Ensure that this decoupling capacitor is placed near the IC.
6	FB	This pin is the inverting input to the error amplifier. Use this pin in conjunction with the COMP pin to compensate the voltage−control feedback loop. Connect this pin to the output resistor divider (if used) or directly to Vout.
7	COMP	Compensation Pin. This is the output of the error amplifier (EA) and the non−inverting input of the PWM comparator. Use this pin in conjunction with the FB pin to compensate the voltage−control feedback loop. This pin should not be shorted to ground to disable switching.
8	PHASE	Switch node pin. This is the reference for the floating top gate driver. Connect this pin to the source of the top MOSFET. A Schottky diode between this pin and ground is recommended to reduce negative transient voltages which is common in a power supply system.

ABSOLUTE MAXIMUM RATINGS

Pin Name	Symbol	V_{MAX}	V_{MIN}
Main Supply Voltage Input	V_{CC}	15 V	−0.3 V
Bootstrap Supply Voltage Input	BST	30 V wrt/GND 15 V wrt/PHASE	−0.3 V
Switching Node (Bootstrap Supply Return)	PHASE	30 V	−0.7 V, t > 50 ns −2.0 V, t < 50 ns
High−Side Driver Output (Top Gate)	TG	30 V wrt/GND 15 V wrt/PHASE	−0.3 V wrt/PHASE
Low−Side Driver Output (Bottom Gate)	BG	15 V	−0.3 V
Feedback	FB	5.5 V	−0.3 V
COMP	COMP	5.5 V	−0.3 V

MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Thermal Resistance, Junction−to−Case		$R_{\theta JC}$	45	°C/W
Operating Junction Temperature Range		T_J	−40 to 150	°C
Operating Ambient Temperature Range		T_A	−40 to 85	°C
Storage Temperature Range		T_{stg}	−55 to +150	°C
ESD Susceptibility	Human Body Model Charge Device Model		2.0 200	kV V
Moisture Sensitivity Level		MSL	1	−

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

ELECTRICAL CHARACTERISTICS (−40°C < T_A < 85°C, −40°C < T_J < 125°C (Note 1), 4.5 V < V_{CC} < 13.2 V, 4.5 V < BST < 26.5 V, C_{TG} = C_{BG} = 1.0 nF, for min/max values unless otherwise noted.)

Characteristic	Conditions	Min	Typ	Max	Unit
Input Voltage Range	−	4.5	−	13.2	V
Boost Voltage Range	−	4.5	−	26.5	V
Supply Current					
Quiescent Supply Current	V_{FB} = 1.0 V, No Switching V_{CC} = 13.2 V	−	1.0	1.75	mA
Boost Quiescent Current	V_{FB} = 1.0 V, No Switching	−	140	−	μA
Undervoltage Lockout					
UVLO Threshold	V_{CC} Rising Edge	3.85	4.2	−	V
UVLO Hysteresis	−	−	0.5	−	V
Switching Regulator					
VFB Feedback Voltage, Control Loop in Regulation	T_A = 0 to 70°C T_A = −40 to 85°C	0.788 0.784	0.800 −	0.812 0.816	V
Oscillator Frequency	−	288	350	412	kHz
Ramp−Amplitude Voltage	−	−	1.1	−	V
Minimum Duty Cycle	−	−	0	−	%
Maximum Duty Cycle	−	85	90	95	%
Minimum Pulse Width	Static Operating (Note 2)	50	100	150	nsec
Error Amplifier					
DC Gain	(Note 2)	70	80	−	dB
Gain−Bandwidth Product	(Note 2)	8.0	10	−	MHz
Slew Rate	COMP_GND = 100 pF (Note 2)	2.0	4.0	−	V/μS
FB Bias Current	VFB = 1 V (Note 2)	−	0.1	1.0	μA
Gate Drivers					
TG Rise Time	Load = 1.0 nF V_{CC} = 8.0 V	−	6.0	15	ns
TG Fall Time		−	15	30	ns
BG Rise Time		−	6.0	15	ns
BG Fall Time		−	6.0	15	ns
TG Sink Current	V_{CC} = 12 V V_{TG} = V_{BG} = 2.0 V (Note 2)	−	1.0	−	A
TG Source Current		−	1.5	−	A
BG Sink Current		−	1.5	−	A
BG Source Current		−	1.5	−	A
PHASE falling to BG rising delay	V_{CC} = 12 V PHASE < 2.0 V BG > 2.0 V	−	30	90	ns
BG falling to TG rising delay	V_{CC} = 12 V BG < 2.0 V TG > 2.0 V	−	30	40	ns
Internal Soft−Start					
Time	−	1.0	2.0	3.0	ms
Thermal Shutdown					
Overtemperature Trip Point	(Note 2)	−	160	−	°C

1. Specifications to −40°C are guaranteed via correlation using standard statistical quality control (SQC), not tested in production.
2. Guaranteed by design, not tested in production.

TYPICAL CHARACTERISTIC CURVES

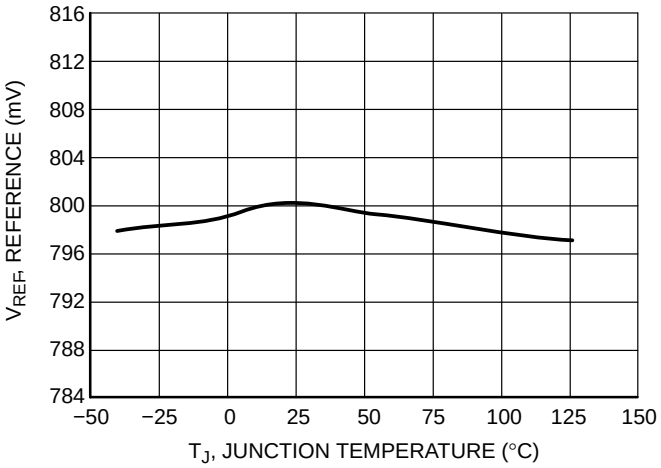


Figure 4. Reference Voltage (V_{REF}) vs. Temperature

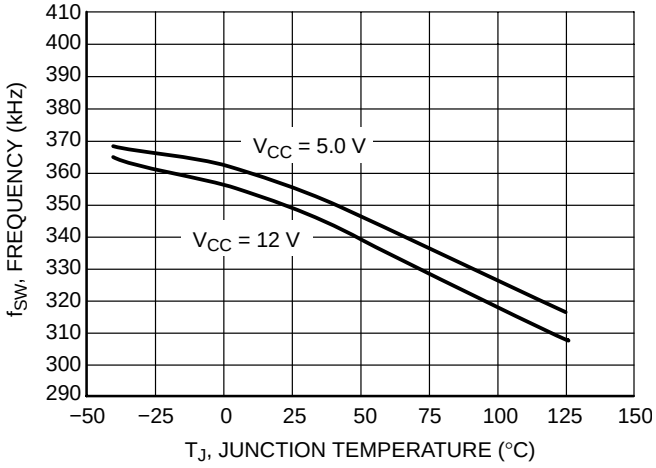


Figure 5. Oscillator Frequency (f_{SW}) vs. Temperature

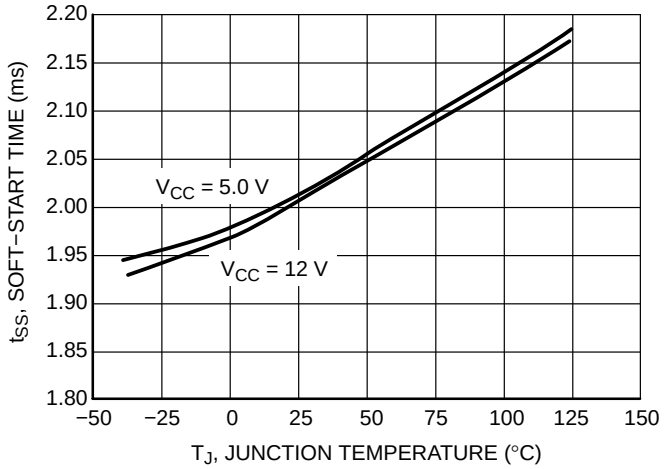


Figure 6. Soft−Start Time (t_{SS}) vs. Temperature

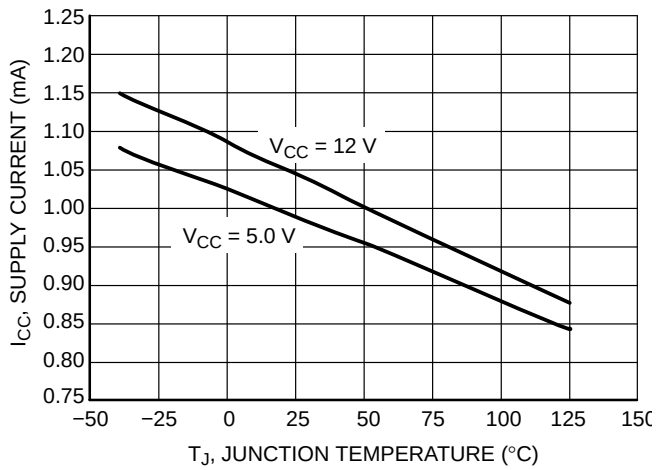


Figure 7. Quiescent Current (I_{CC}) vs. Temperature (No Switching)

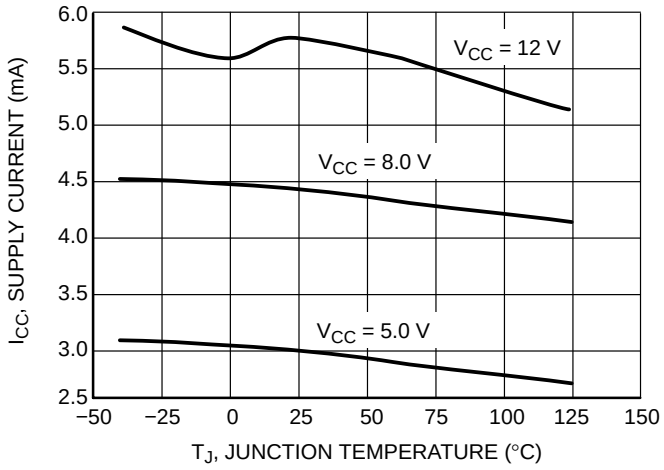


Figure 8. Quiescent Current (I_{CC}) vs. Temperature (Switching)

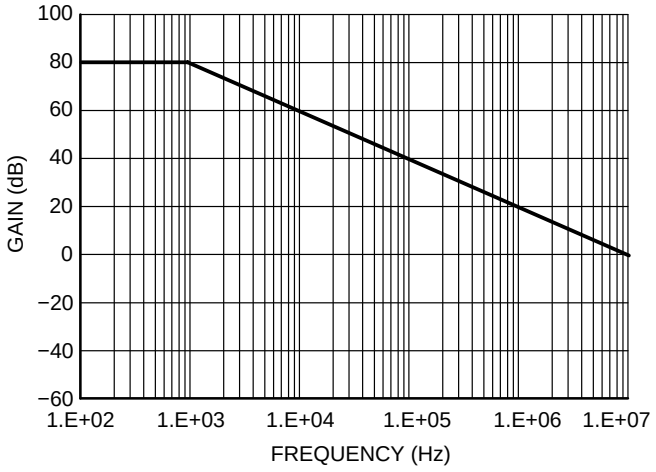


Figure 9. Error Amplifier

DETAILED OPERATING DESCRIPTION

General

The NCP1580 is an 8−pin PWM controller intended for DC−DC conversion from 5.0 V and 12 V buses. The NCP1580 has a 1.5 A internal floating gate driver circuit designed to drive N−Channel MOSFETs in a synchronous−rectifier buck topology. The internal floating gate driver simplifies design, improves performance, and minimizes board area. The output voltage of the converter can be precisely regulated down to 800 mV ± 1.5% when the V_{FB} pin is tied to V_{OUT}. The switching frequency, which is internally set to 350 kHz, and soft−start are completely integrated. The voltage error amplifier features a 10 MHz unity gain bandwidth and 4 V/μsec slew rate for fast transient response.

Duty Cycle and Maximum Pulse Width Limits

In steady state DC operation, the duty cycle will stabilize at an operating point defined by the ratio of the input to the output voltage. The NCP1580 can achieve a 90% duty cycle. There is a built in off−time which ensures that the bootstrap supply is charged every cycle. The NCP1580, which is capable of a 100 nsec minimum pulse width (typ), can allow a 12 V to 1.0 V conversion at 350 kHz.

Input Voltage Range (V_{CC} and BST)

The input voltage range for both V_{CC} and BST is 4.5 V to 13.2 V with respect to GND and PHASE, respectively. Although BST is rated at 13.2 V with respect to PHASE, it can also tolerate 26.5 V with respect to GND.

Normal Shutdown Behavior

Normal shutdown occurs when the IC stops switching because the input supply reaches UVLO threshold. In this case, switching stops, the internal SS is discharged, and all GATE pins go low. The switch node enters a high impedance state and the output capacitors discharge through the load with no ringing on the output voltage.

Internal Soft−Start

The NCP1580 features an internal soft−start function, which reduces inrush current and overshoot of the output voltage. Figure 10 shows a typical soft−start sequence. Soft−start is achieved by ramping up the internal soft−start voltage (V_{SS}) which is applied to the input of the error amplifier. This ramp is generated by applying 0.5 μA to a 100 pf capacitor for 1 μsec on every fourth clock pulse. This sequence begins once V_{CC} surpasses its UVLO threshold (see Figure 11). The typical soft−start time is 2 msec. The internal soft−start voltage is held low when the part is in UVLO.

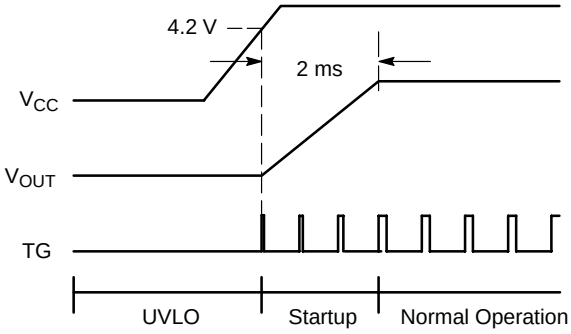


Figure 10. Normal Startup

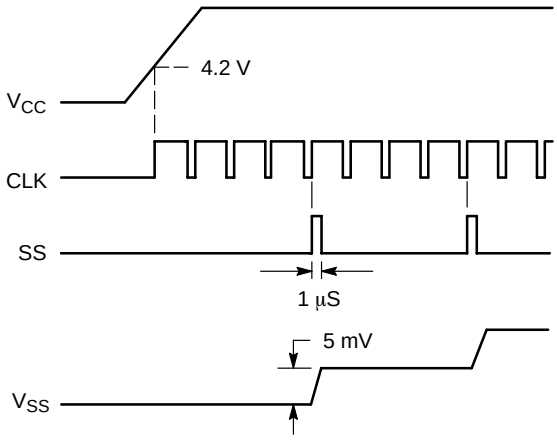


Figure 11. Achieving Internal Soft−Start

UVLO

Undervoltage Lockout (UVLO) is provided to ensure that unexpected behavior does not occur when V_{CC} is too low to support the internal rails and power the converter. For the NCP1580, the UVLO is set to ensure that the IC will start up when V_{CC} reaches 4.2 V and shutdown when V_{CC} drops below 3.7 V. This permits operation when converting from a 5.0 V input voltage.

Thermal Shutdown

The NCP1580 also provides Thermal Shutdown (TSD) for added protection. The TSD circuit monitors the die temperature and turns off the top and bottom gate drivers if an over temperature condition is detected. The internal soft−start capacitor is also discharged. This is a latched state and requires a power cycle to reset.

Drivers

The NCP1580 includes 1.5 A gate drivers to switch external N−Channel MOSFETs. This allows the NCP1580 to address high−power as well as low−power conversion requirements. The gate drivers also include adaptive non−overlap circuitry. The non−overlap circuitry increases efficiency, which minimizes power dissipation, by minimizing the body diode conduction time.

A detailed block diagram of the non−overlap and gate drive circuitry used in the chip is shown in Figure 12.

Careful selection and layout of external components is required, to realize the full benefit of the onboard drivers. The capacitors between V_{CC} and GND and between BST and SWN must be placed as close as possible to the IC. The current paths for the TG and BG connections must be optimized. A ground plane should be placed on the closest layer for return currents to GND in order to reduce loop area and inductance in the gate drive circuit.

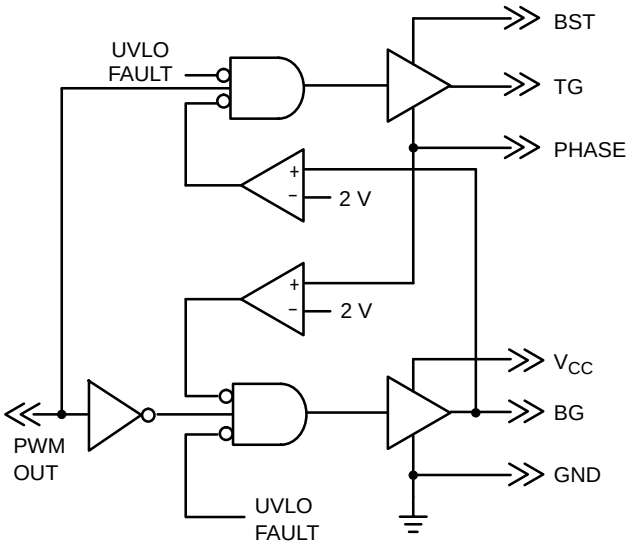


Figure 12. Block Diagram

APPLICATION SECTION

Input Capacitor Selection

The input capacitor has to sustain the ripple current produced during the on time of the upper MOSFET, so it must have a low ESR to minimize the losses. The RMS value of this ripple is:

$$Iin_{RMS} = I_{OUT}\sqrt{D \times (1 - D)},$$

where D is the duty cycle, I_{inRMS} is the input RMS current, and I_{OUT} is the load current. The equation reaches its maximum value with D = 0.5. Losses in the input capacitors can be calculated with the following equation:

$$P_{CIN} = ESR_{CIN} \times Iin_{RMS}^2,$$

where P_{CIN} is the power loss in the input capacitors and ESR_{CIN} is the effective series resistance of the input capacitance. Due to large dI/dt through the input capacitors, electrolytic or ceramics should be used. If a tantalum must be used, it must be surge protected. Otherwise, capacitor failure could occur.

Calculating Input Startup Current

To calculate the input startup current, the following equation can be used.

$$I_{inrush} = \frac{C_{OUT} \times V_{OUT}}{t_{SS}},$$

where I_{inrush} is the input current during startup, C_{OUT} is the total output capacitance, V_{OUT} is the desired output voltage, and t_{SS} is the internal soft−start interval.

If the inrush current is higher than the steady state input current during max load, then the input fuse should be rated accordingly, if one is used.

Output Capacitor Selection

The output capacitor is a basic component for the fast response of the power supply. In fact, during load transient, for the first few microseconds it supplies the current to the load. The controller immediately recognizes the load transient and sets the duty cycle to maximum, but the current slope is limited by the inductor value.

During a load step transient the output voltage initially drops due to the current variation inside the capacitor and the ESR. (neglecting the effect of the effective series inductance (ESL)):

$$\Delta V_{OUT-ESR} = \Delta I_{OUT} \times ESR_{COUT},$$

where $V_{OUT-ESR}$ is the voltage deviation of V_{OUT} due to the effects of ESR and the ESR_{COUT} is the total effective series resistance of the output capacitors.

A minimum capacitor value is required to sustain the current during the load transient without discharging it. The voltage drop due to output capacitor discharge is given by the following equation:

$$\Delta V_{OUT\ -\ DISCHARGE} = \frac{\Delta I_{OUT}^2 \times L_{OUT}}{2 \times C_{OUT} \times (V_{IN} \times D - V_{OUT})},$$

where $V_{OUT-DISCHARGE}$ is the voltage deviation of V_{OUT} due to the effects of discharge, L_{OUT} is the output inductor value and V_{IN} is the input voltage.

It should be noted that $\Delta V_{OUT-DISCHARGE}$ and $\Delta V_{OUT-ESR}$ are out of phase with each other, and the larger of these two voltages will determine the maximum deviation of the output voltage (neglecting the effect of the ESL).

Inductor Selection

Both mechanical and electrical considerations influence the selection of an output inductor. From a mechanical perspective, smaller inductor values generally correspond to smaller physical size. Since the inductor is often one of the largest components in the regulation system, a minimum inductor value is particularly important in space−constrained applications. From an electrical perspective, the maximum current slew rate through the output inductor for a buck regulator is given by:

$$SlewRate_{LOUT} = \frac{V_{IN} - V_{OUT}}{L_{OUT}}$$

This equation implies that larger inductor values limit the regulator's ability to slew current through the output inductor in response to output load transients. Consequently, output capacitors must supply the load current until the inductor current reaches the output load current level. This results in larger values of output capacitance to maintain tight output voltage regulation. In contrast, smaller values of inductance increase the regulator's maximum achievable slew rate and decrease the necessary capacitance, at the expense of higher ripple current. The peak−to−peak ripple current is given by the following equation:

$$Ipk{-}pk_{LOUT} = \frac{V_{OUT}(1 - D)}{L_{OUT} \times 350\ kHZ},$$

where $Ipk{-}pk_{LOUT}$ is the peak to peak current of the output. From this equation it is clear that the ripple current increases as L_{OUT} decreases, emphasizing the trade−off between dynamic response and ripple current.

Feedback and Compensation

The NCP1580 allows the output of the DC−DC converter to be adjusted from 0.8 V to 5.0 V via an external resistor divider network. The controller will try to maintain 0.8 V at the feedback pin. Thus, if a resistor divider circuit was placed across the feedback pin to V_{OUT}, the controller will regulate the output voltage proportional to the resistor divider network in order to maintain 0.8 V at the FB pin.

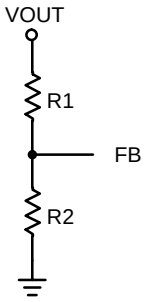


Figure 13.

The relationship between the resistor divider network in Figure 13 and the output voltage is shown in the following equation:

$$R_2 = R_1 \times \left(\frac{V_{REF}}{V_{OUT} - V_{REF}}\right).$$

Resistor R1 is selected based on a design trade off between efficiency and output voltage accuracy. For high values of R1 there is less current consumption in the feedback network, However the trade off is output voltage accuracy due to the bias current in the error amplifier. The output voltage error of this bias current can be estimated using the following equation (neglecting resistor tolerance):

$$\text{Error\%} = \frac{0.1\ \mu A \times R_1}{V_{REF}} \times 100\%$$

Once R1 has been determined, R2 can be calculated.

The NCP1580 utilizes voltage mode control. This is to say, the control loop regulates V_{OUT} by monitoring V_{OUT} and controlling the output current. However, since the control loop is controlling the output current to regulate the output voltage, there are some stability concerns since the inductor current is 90 degrees out of phase with the voltage. It is inherent with all voltage−mode control loops to have a compensation network.

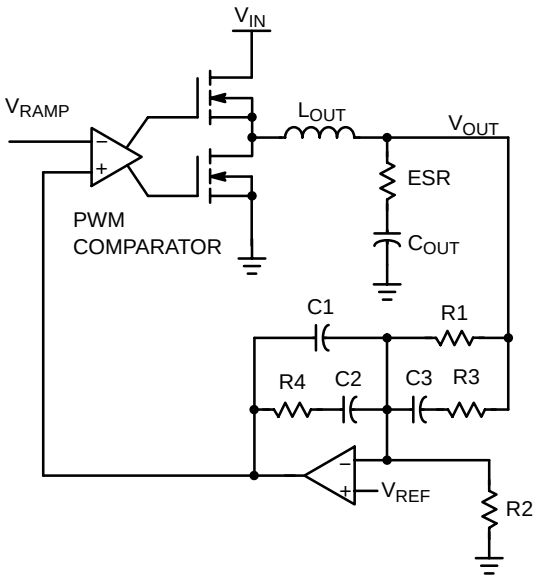


Figure 14. Simplified Diagram of Control Loop

The compensation network consists of the internal error amplifier and the impedance networks Z_{IN} (R1, R3 and C3) and Z_{FB} (R4, C1 and C2). The compensation network has to provide a closed loop transfer function with the highest 0 dB crossing frequency to have fast response (but always lower than $f_{SW}/8$) and the highest gain in DC conditions to minimize the load regulation. A stable control loop has a gain crossing with −20 dB/decade slope and a phase margin greater than 45°. Include worst−case component variations when determining phase margin. To place the poles and zeroes of the compensation networks, the following equations may be used:

Modulator frequencies:

$$\omega_{LC} = \frac{1}{\sqrt{L_{OUT} \times C_{OUT}}} \quad \omega_{ESR} = \frac{1}{\sqrt{ESR \times C_{OUT}}}$$

Compensation network frequency:

$$\omega_{P1} = \frac{1}{R4 \times \left(\frac{C1 \times C2}{C1 + C2}\right)} \quad \omega_{P2} = \frac{1}{R3 \times C3}$$

$$\omega_{Z1} = \frac{1}{R4 \times C2} \quad \omega_{Z2} = \frac{1}{(R1 + R3) \times C3}$$

Place ω_{Z1}, and ω_{Z2} around the output filter resonance ω_{LC}; Place ω_{P1} at the output capacitor ESR zero ω_{ESR}; Place ω_{P2} at one half of the switching frequency;

The modulator transfer function is the small−signal transfer function of V_{OUT}/V_{COMP}. This function has a double pole at frequency ω_{LC} and a zero at ω_{ESR}. The DC Gain of the modulator is simply the input voltage V_{IN} divided by the peak−to−peak oscillator voltage ΔV_{OSC}.

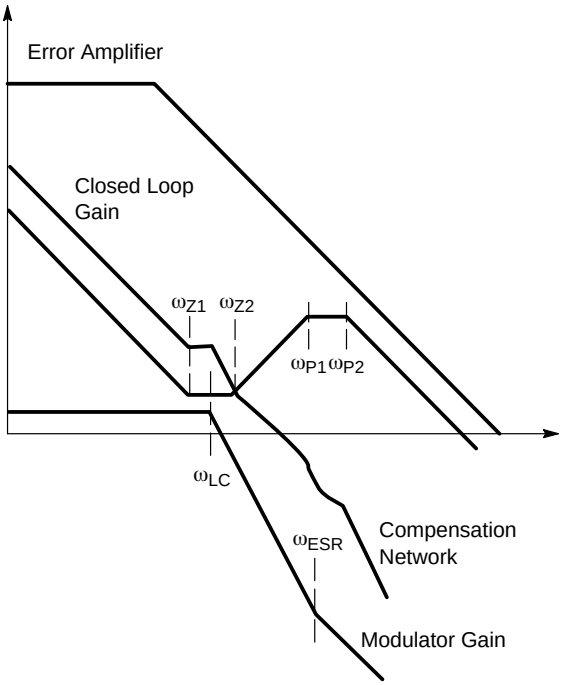


Figure 15.

Visit http://www.onsemi.com/pub/Collateral/COMPCALC for self extracting compensation program for design assistance.

Thermal Considerations

The power dissipation of the NCP1580 varies with the MOSFETs used, V_{CC}, and the boost voltage (V_{BST}). The average MOSFET gate current typically dominates the control IC power dissipation. The IC power dissipation is determined by the formula:

$$P_{IC} = (I_{CC} \times V_{CC}) + P_{TG} + P_{BG}.$$

Where:

P_{IC} = Control IC power dissipation,
I_{CC} = IC measured supply current,
V_{CC} = IC supply voltage,
P_{TG} = Top gate driver losses,
P_{BG} = Bottom gate driver losses.

The upper (switching) MOSFET gate driver losses are:

$$P_{TG} = Q_{TG} \times f_{SW} \times V_{BST}.$$

Where:

Q_{TG} = Total upper MOSFET gate charge at VBST,
f_{SW} = The switching frequency,
V_{BST} = The BST pin voltage.

The lower (synchronous) MOSFET gate driver losses are:

$$P_{BG} = Q_{BG} \times f_{SW} \times V_{CC}.$$

Where:

Q_{BG} = total lower MOSFET gate charge at V_{CC}.

The junction temperature of the control IC can then be calculated as:

$$T_J = T_A + P_{IC} \times \theta_{JA}.$$

Where:

T_J = The junction temperature of the IC,
T_A = The ambient temperature,
θ_{JA} = The junction−to−ambient thermal resistance of the IC package.

The package thermal resistance ($R_{\theta JC}$) can be obtained from the specifications section of this data sheet and a calculation can be made to determine the IC junction temperature. In addition, a thermal resistance (Junction−to−Ambient/Safe Operating Area) curve has been included below to further aid design. However, it should be noted that the physical layout of the board, the proximity of other heat sources such as MOSFETs and inductors, and the amount of metal connected to the IC, impact the temperature of the device. Use these calculations as a guide, but measurements should be taken in the actual application.

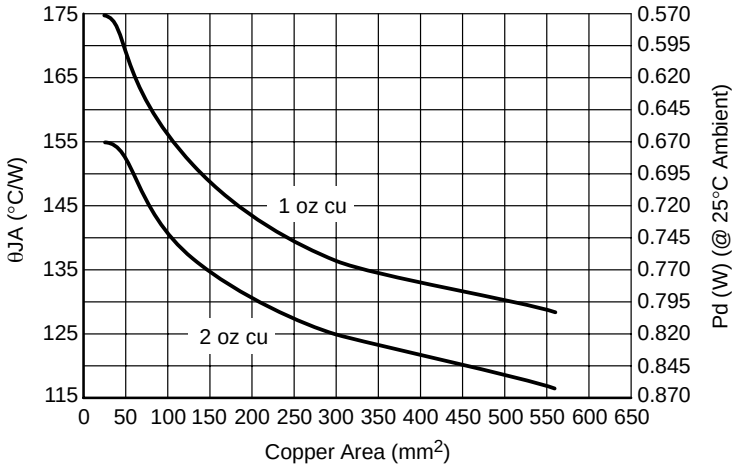


Figure 16. Thermal Resistance (Junction−to−Ambient/Safe Operating Area)

Layout Considerations

As in any high frequency switching converter, layout is very important. Switching current from one power device to another can generate voltage transients across the impedances of the interconnecting bond wires and circuit traces. These interconnecting impedances should be minimized by using wide, short printed circuit traces. The critical components should be located as close together as possible using ground plane construction or single point grounding. Figure 17 shows the critical power components of the converter. To minimize the voltage overshoot the interconnecting wires indicated by heavy lines should be part of ground or power plane in a printed circuit board. The components shown in Figure 17 should be located as close together as possible. Please note that the capacitors C_{IN} and C_{OUT} each represent numerous physical capacitors. It is desirable to locate the NCP1580 within 1 inch of the MOSFETs, Q1 and Q2. The circuit traces for the MOSFETs' gate and source connections from the NCP1580 must be sized to handle up to 2.0 A peak current.

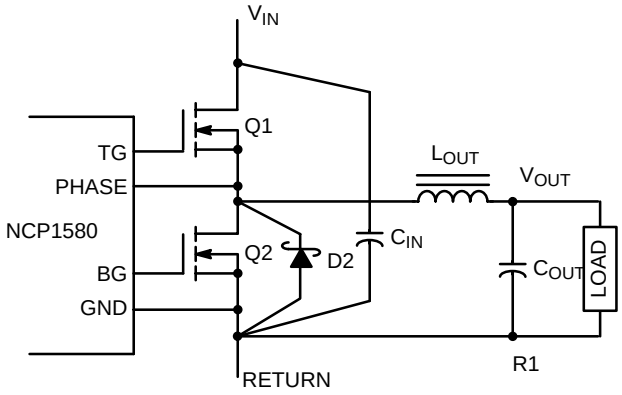


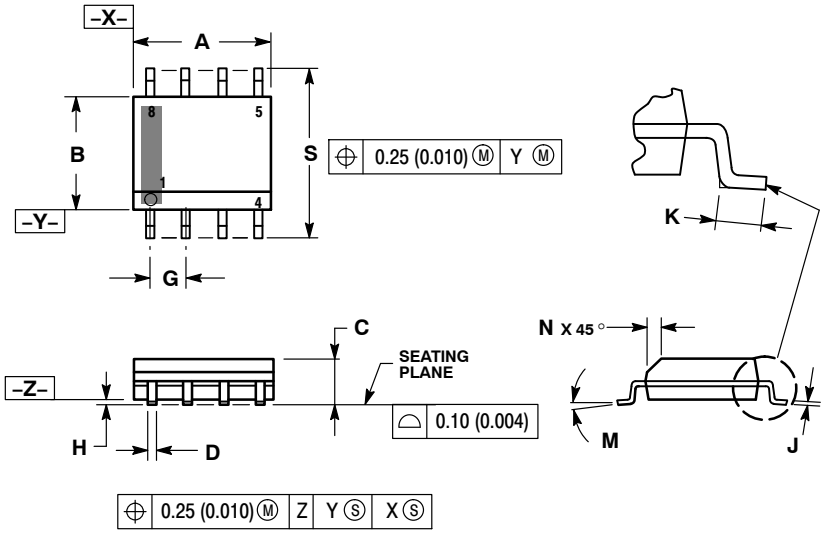
Figure 17.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

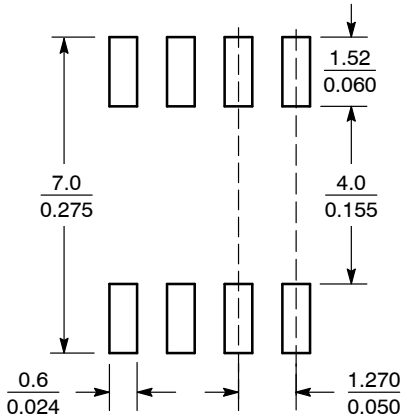
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

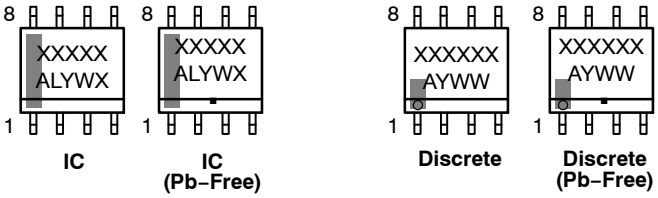
SOLDERING FOOTPRINT*



SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



IC | **IC (Pb−Free)** | **Discrete** | **Discrete (Pb−Free)**

XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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DESCRIPTION:	**SOIC−8 NB**		**PAGE 1 OF 2**

SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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