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# S1R72V17
# CPU Connection Guide

SEIKO EPSON CORPORATION

Rev. 1.0

## Scope

This document applies to the S1R72V17 USB2.0 host/device controller LSI.

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# 1. Introduction

## 1.1 Overview

This document contains information required for actual use of the S1R72V17 by the customer, focusing on the details necessary to connect the S1R72V17 to the control CPU.

This document describes typical connection methods. No guarantees are made regarding the suitability of these methods. The connection methods must be modified to suit specific customer system configurations.

The contents of this document are subject to change without notice.

## 1.2 Related Documents

- S1R72V17 Technical Manual (Hardware Specifications)

# 2. Connection Example with Standard CPU

This section illustrates a typical connection with a standard CPU.

1) 16-bit bus, Strobe mode connection example

Set CPU_Config register (0x075h address) BusMode bit to "0" and Bus8x16 bit to "0."

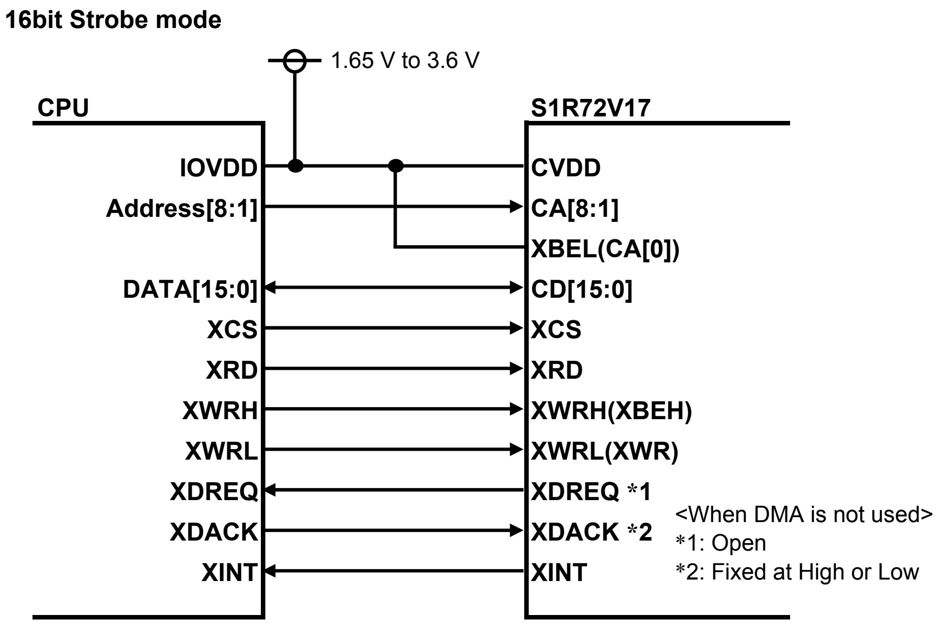


**Fig. 2-1 16-bit bus, Strobe mode connection example**

2) 16-bit bus, BE mode connection example

Set CPU_Config register (0x075h address) BusMode bit to "1" and Bus8x16 bit to "0."

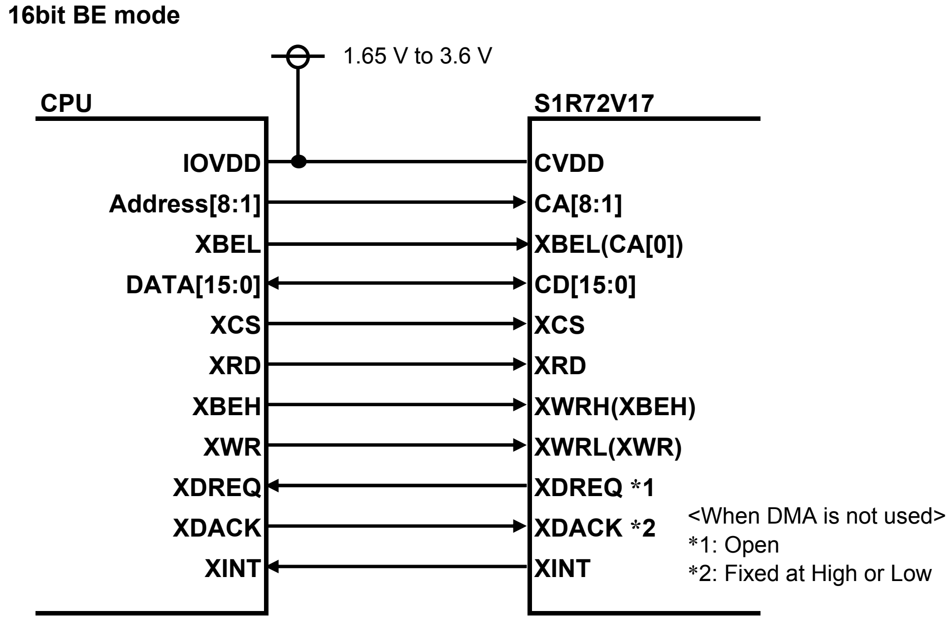


**Fig. 2-2 16-bit bus, BE mode connection example**

3) 8-bit bus mode connection example

Set CPU_Config register (0x075h address) BusMode bit to "0" and Bus8x16 bit to "1."

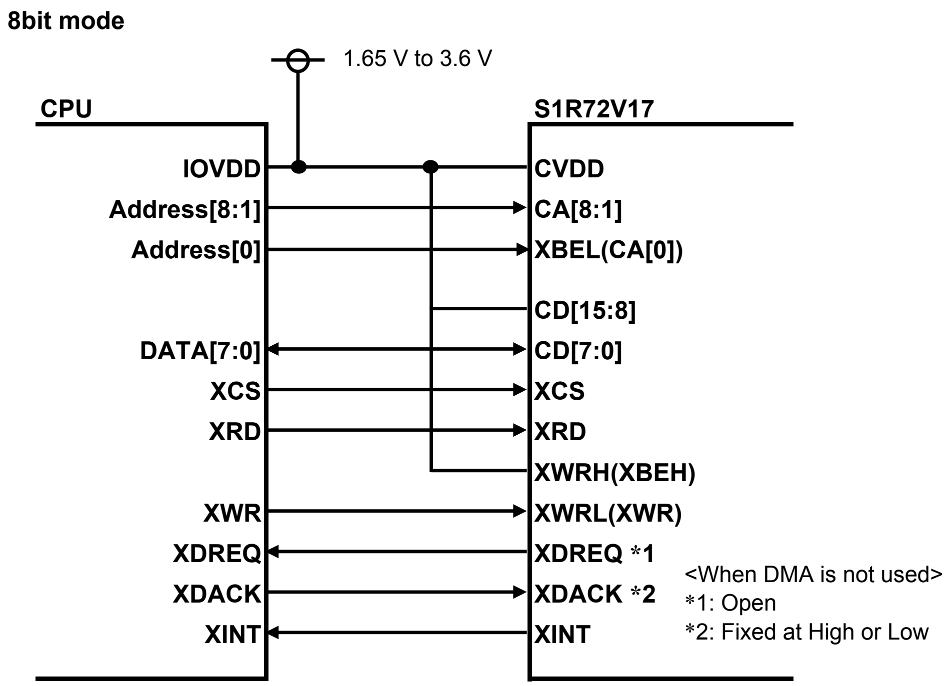


**Fig. 2-3 8-bit bus mode connection example**

# 3. Endian Settings for 16-bit Bus Width Connection

This section describes endian settings when connecting to a CPU with a 16-bit bus width.

The discussion of the S1R72V17 registers divides them into the following three types. For register details, refer to the *S1R72V17 Technical Manual*.

1) Word register: Registers with _H/_L/_HH/_HL/_LH/_LL at the end of the register name
2) Byte register: Registers not corresponding to Word or FIFO registers
3) FIFO register: RAM_Rd_00 to _1F/RAM_WrDoor_0,1/FIFO_Rd_0,1/FIFO_Wr_0,1/ FIFO_ByteRd registers

## 3.1 Connection to Big-endian CPU

Access is normally in the mode with "0" set in the CPU_Config register (0x075h address) CPU_Endian bit.

1) Access to Word register

The S1R72V17 connects the D[15:8] bus to the first byte of the Word register and the D[7:0] bus to the last byte of the Word register.

The example below illustrates the writing and reading of 0x1234h data to/from the Word register.

Writing: The data (12h) in the CPU memory even-number address is saved to the first byte of the S1R72V17 Word register.

Reading: The first byte data (12h) of the S1R72V17 Word register is saved to the even-number address in CPU memory.

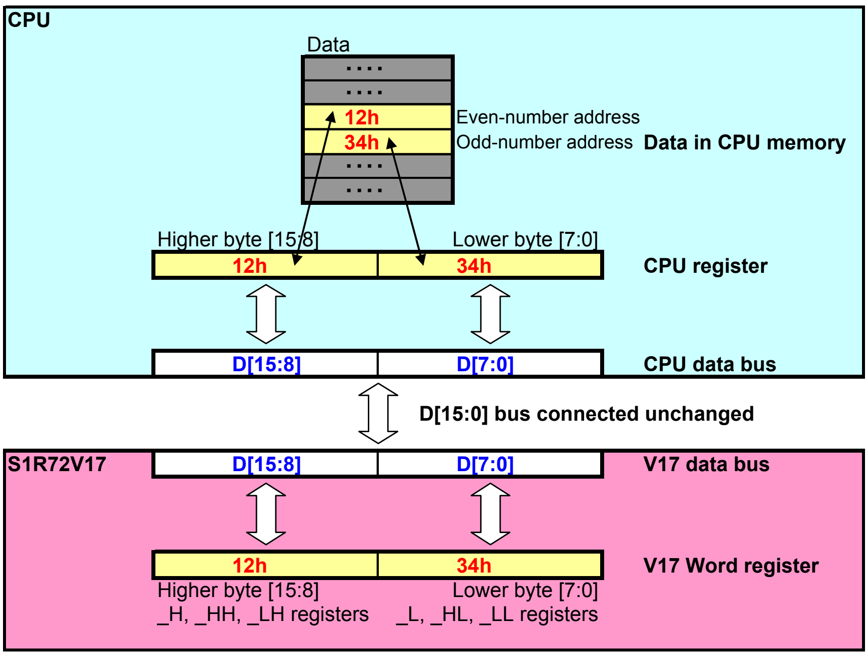


**Fig. 3-1 Access to Word registers (big-endian CPU)**

2) Access to Byte register

The S1R72V17 connects the D[15:8] bus to the even-number address register and the D[7:0] bus to the odd-number address register when the CPU_Endian bit is set to “0.”

The example below illustrates the writing and reading of F1h to/from the Byte register even-number address register and of F2h to/from the Byte register odd-number address register.

Writing: The data (F1h) in the CPU memory even-number address is saved to the S1R72V17 even-number address register.

Reading: The S1R72V17 even-number address register data (F1h) is saved to the even-number address in CPU memory.

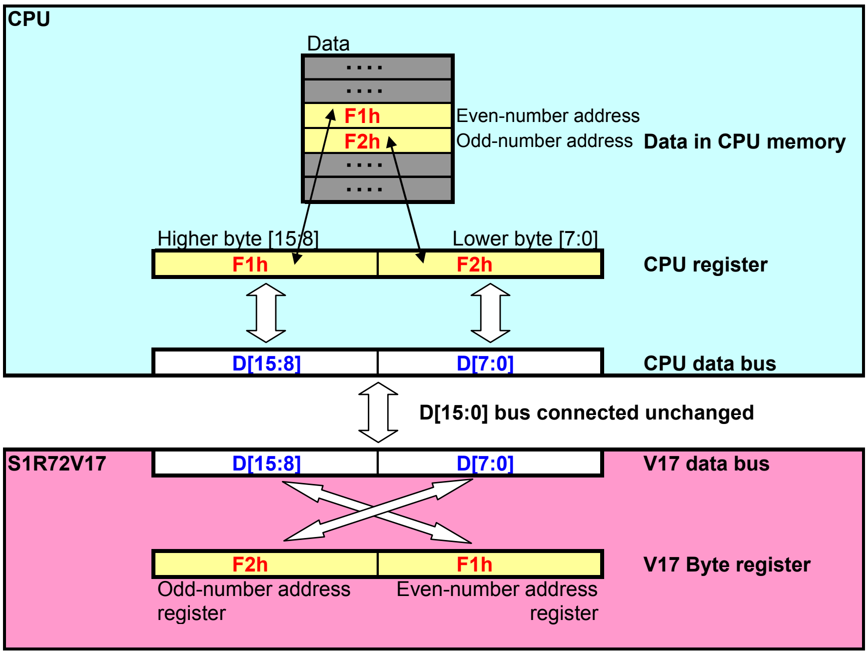


**Fig. 3-2 Access to Byte registers (big-endian CPU)**

3) Access to FIFO register

The S1R72V17 connects the D[15:8] bus to the even-number address register and the D[7:0] bus to the odd-number address register when the CPU_Endian bit is set to "0."

The example below illustrates transmission from the USB bus in the sequence C1h/C2h and receiving in the sequence C1h/C2h.

Writing: The data (C1h) in the CPU memory even-number address is sent from the USB bus as the first data.

Reading: The first data received from the USB bus (C1h) is saved to the even-number address in CPU memory.

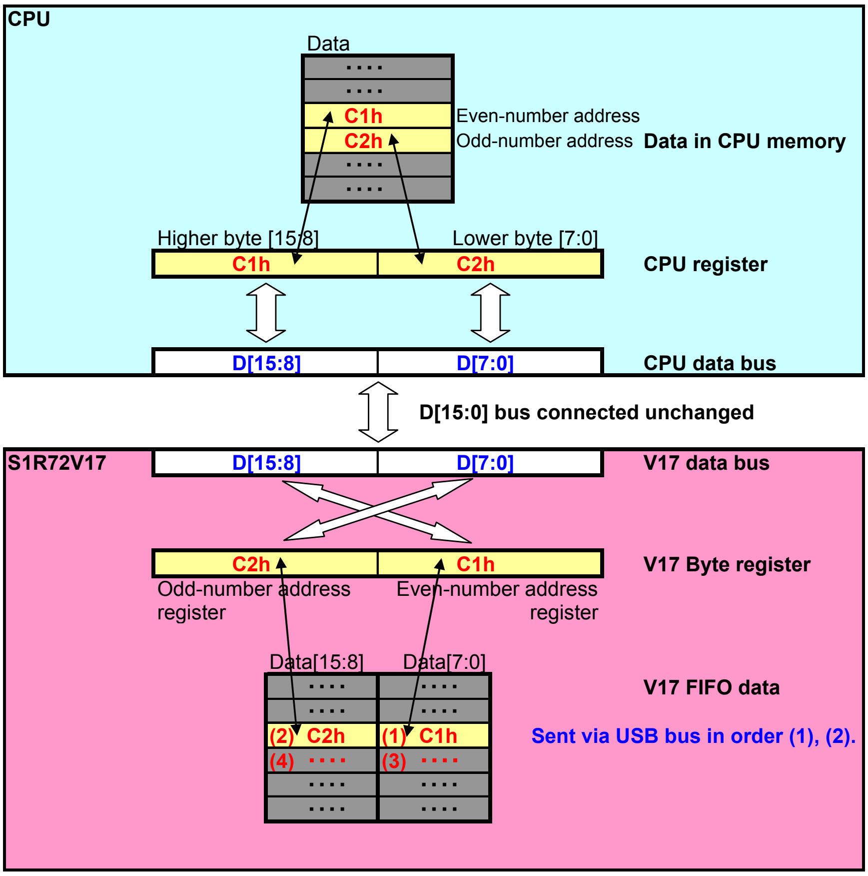


**Fig. 3-3 Access to FIFO registers (big-endian CPU)**

## 3.2 Connection to Little-endian CPU

Access is normally in the mode with “1” set in the CPU_Config register (0x075h address) CPU_Endian bit.

1) Access to Word register

The S1R72V17 connects the D[15:8] bus to the first byte of the Word register and the D[7:0] bus to the last byte of the Word register.

The example below illustrates the writing and reading of 0x1234h data to/from the Word register.

Writing: The data (34h) in the CPU memory even-number address is saved to the last byte of the S1R72V17 Word register.

Reading: The last byte data (34h) of the S1R72V17 Word register is saved to the even-number address in CPU memory.

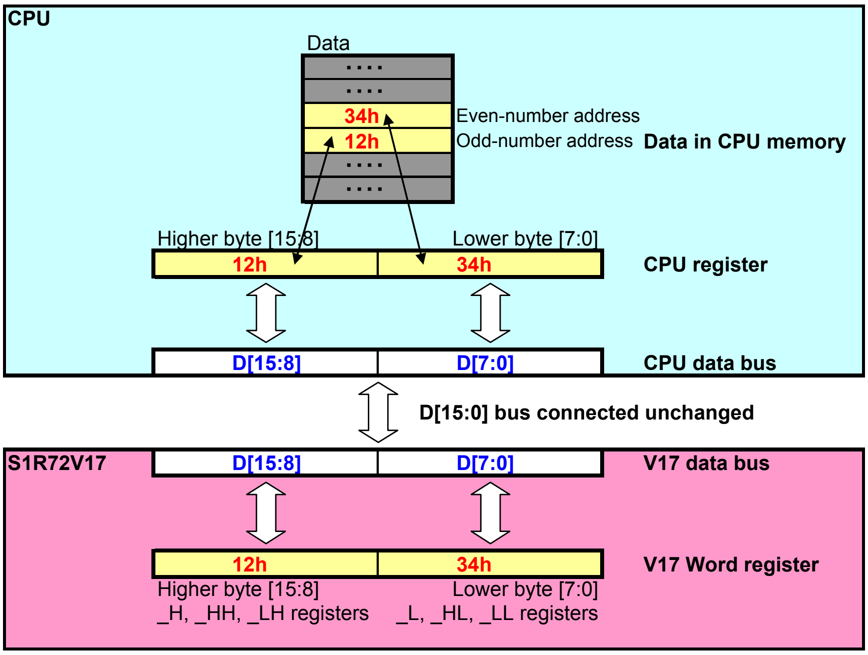


**Fig. 3-4 Access to Word registers (little-endian CPU)**

2) Access to Byte register

The S1R72V17 connects the D[7:0] bus to the even-number address register and the D[15:8] bus to the odd-number address register when the CPU_Endian bit is set to "1."

The example below illustrates the writing and reading of F1h to/from the Byte register even-number address register and of F2h to/from the Byte register odd-number address register.

Writing: The data (F1h) in the CPU memory even-number address is saved to the S1R72V17 even-number address register.

Reading: The S1R72V17 even-number address register data (F1h) is saved to the even-number address in CPU memory.

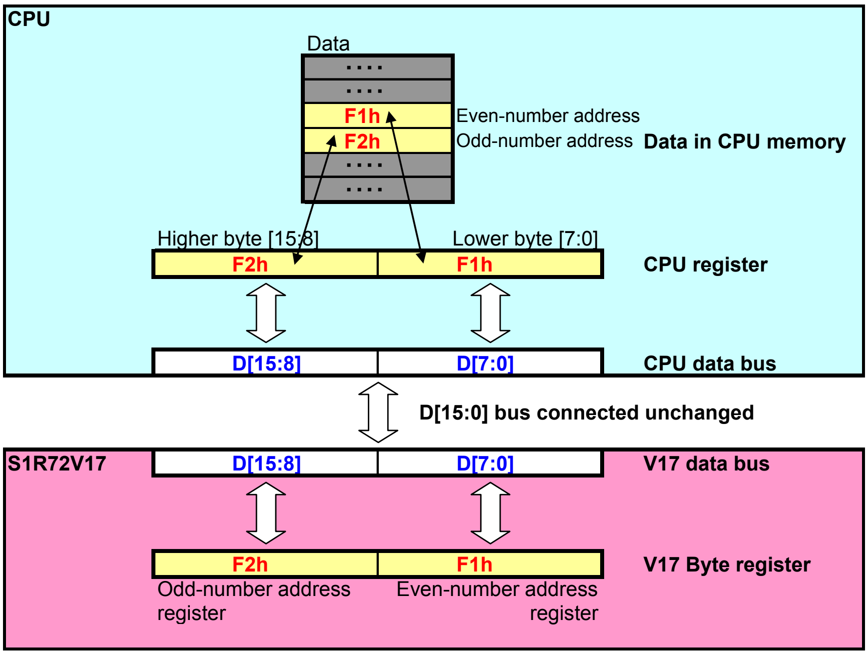


**Fig. 3-5 Access to Byte registers (little-endian CPU)**

3) Access to FIFO register

The S1R72V17 connects the D[7:0] bus to the even-number address register and the D[15:8] bus to the odd-number address register when the CPU_Endian bit is set to "1."

The example below illustrates transmission from the USB bus in the sequence C1h/C2h and receiving in the sequence C1h/C2h.

Writing: The data (C1h) in the CPU memory even-number address is sent from the USB bus as the first data.

Reading: The first data received from the USB bus (C1h) is saved to the even-number address in CPU memory.

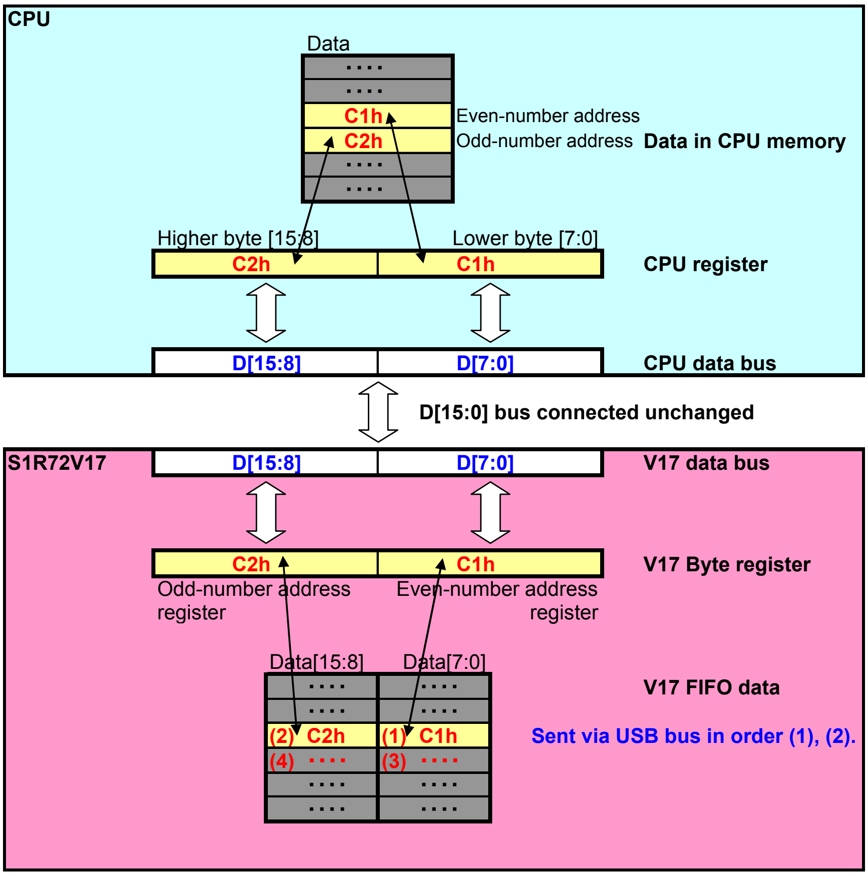


Fig. 3-6 Access to FIFO registers (little-endian CPU)

# 4. CPUIF Verification Procedure

The procedure shown here checks whether the S1R72V17 is correctly connected to the CPU. Follow the procedure given below, using ICE on the CPU used to control this LSI.

**<Connection test start (HW reset cancel)>**

| | |
| --- | --- |
| **1) Recovery processing from CPU_Cut state** | Dummy read PM_Control register (0x012 address) |
| **2) Endian setting initialization** | Dummy read CPU_ChgEndian register (0x077h address) |
| **3) CPU operating mode setting** | Set CPU_Endian, BusMode, Bus8x16 to the CPU_Config register<br>Little-endian CPU: 0x74h address<br>Big-endian CPU: 0x75h address |
| **4) Endian setting enabling** | Dummy read CPU_ChgEndian register (0x077h address) |
| **5) Asynchronous register access test (Word register)** | Read/write test to/from WakeupTim_H,L registers (0x014h address) |
| **6) Clock input setting** | Write clock setting value to ClkSelect register (0x73h address) |
| **7) Clock input setting protect** | Write 0x00 to ModeProtect register (0x071 address) |
| **8) MTM reset** | Write 0x00 to ChipReset register (0x011 address) |
| **9) Oscillation start time setting** | Write oscillation start time to WakeupTim_H,L registers (0x014 address) |
| **10) Internal clock feed setting** | Write 0x40 to PM_Control register (0x012 address) |
| **11) Internal clock setting confirmation** | Read MainIntStat register (0x000 address) to check that FinishedPM bit (bit 0) is set to "1." |
| **12) Synchronous register access test (Word register)** | Read/write test to/from AREA0StartAdrs_L,H registers (0x080 address) |
| **13) Synchronous register access test (Byte register)** | Read/write test to/from D_EPaIntEnb register (0x0C6 address) and D_EPbIntEnb register (0x0C7 address) |

**<Connection test end>**

**Fig. 4-1 CPU-IF verification procedure**

**1) Recovery processing from CPU_Cut state**

Dummy read the PM_Control register (0x012h address).

The S1R72V17 switches to CPU_Cut state after resetting has been cancelled. This dummy read operation ends the CPU_Cut state and switches to Sleep. In the Sleep state, reading/writing is possible to/from all asynchronous registers.

**2) Endian setting initialization**

Dummy read the CPU_ChgEndian register (0x077h address).

Setting the ChipReset register (0x011h address) AllReset bit to “1” enables the reset CPU_Config register CPU_Endian setting after this register has been dummy read when the S1R72V17 has been reset.

**3) CPU operating mode setting**

Write the usage mode settings to the CPU_Config register CPU_Endian, BusMode, and Bus8x16 bits.

Little-endian CPU: 0x74h address

Big-endian CPU: 0x75h address

This register address is assigned to the 0x075h address. Since the S1R72V17 operates in the default big-endian state until this setting is changed, the 0x074h address should be accessed to access a little-endian CPU.

**Table 4-1 CPU_Config register settings**

| Bus mode | CPU endian | Setting |
|---|---|---|
| 16-bit Strobe mode | Little Endian | 0x04 |
| | Big Endian | 0x00 |
| 16-bit BE mode | Little Endian | 0x06 |
| | Big Endian | 0x02 |
| 8-bit mode | - | 0x01 |

**4) Endian setting enabling**

Dummy read the CPU_ChgEndian register (0x77h address).

Reading this register enables the CPU_Endian bit set in 3).

**5) Asynchronous register access test (Word register)**

Read/write test to/from the WakeupTim_L,H registers (0x014 address).

This register can be read/written in the Sleep state. All bits are enabled.

Read/write testing this register checks whether the CPU data bus is correctly connected. If this read/write operation is not performed correctly, check the physical connection with the CPU.

**6) Clock input setting**

Write the clock input setting value to the ClkSelect register (0x73h address).

This sets the clock input method and frequency used for the S1R72V17. The settings are shown in Table 4-2.

**Table 4-2 ClkSelect register settings**

| | Clock input method | |
|---|---|---|
| **Clock frequency** | **External oscillator** | **External clock source** |
| 12 MHz | 0x00 | 0x80 |
| 24 MHz | 0x01 | 0x81 |
| 48 MHz | Not available | 0x83 |

**7) Clock input setting protect**

Write 0x00 to the ModeProtect register (0x071 address).

Writing a value other than 0x56 to this register enables write protection for the ClkSelect register.

**8) MTM reset**

Write 0x00 to the ChipReset register (0x011 address).

Clearing the bit7 ResetMTM bit to "0" clears the USB Transceiver Macro reset and enables oscillation of the PLL contained in the S1R72V17.

**9) Oscillation start time setting**

Write the oscillation start time to the WakeupTim_H,L registers (0x014 address).

With external clock source:

Write 0x0010. Note that the external clock source oscillation must have stabilized before this occurs.

With external oscillator:

The standard time is usually within the clock frequency ±10%, but this will vary greatly, depending on the selected oscillator, circuit board, and external components. Write 0x2500 here to check the connection.

**10) Internal clock feed setting**

Write 0x40 to the PM_Control register (0x012 address).

Setting the bit6 GoActive bit to "1" starts the internal clock operation (starts OSC and PLL) and starts the clock feed to the internal circuit.

11) **Internal clock feed confirmation**

Read the MainIntStat register (0x000 address) to confirm that the FinishedPM bit (bit 0) has been set to "1."

If this bit is not set, it is likely that the clock is not fed from the external clock when the external clock source is selected and that the oscillator is not oscillating correctly when the external oscillator is selected.

In this case, the 0x008 address (MainIntEnb register) bit 0 (EnFinishedPM bit) should be set to "1." This asserts the XINT output pin to "Low." Subsequently clearing the bit to "0" negates the XINT output pin to "High." This operation should be used to confirm that an interrupt occurs in the CPU.

Writing "1" to the MainIntStat register (0x000 address) bit 0 (FinishedPM bit) clears this status. Read the MainIntStat register (0x000 address) bit 0 (FinishedPM bit) again to confirm that it has been cleared to "0."

12) **Synchronous register access test (Word register)**

Read/write test to/from the AREA0StartAdrs_L,H registers (0x080 address).

These registers can be read/written in the Active state.

The first 3 bits (bits [15:13]) and the last 2 bits (bits [1:0]) cannot be written to. They will always read "0."

13) **Synchronous register access test (Byte register)**

Read/write test to/from the D_EPaIntEnb register (0x0C6 address) and D_EPbIntEnb registers (0x0C7 address).

These registers can be read/written in the Active state.

The first bit (bit [7]) for the D_EPaIntEnb and D_EPbIntEnb registers cannot be written to and always reads "0."

**<This ends the connection test.>**

# 5. Connection Example with FreeScale iMX21

## 5.1 Connection Example

This section illustrates an example of a connection between the proven CPU-IF on the S1R72V17 and the iMX21.

The connection uses the S1R72V17 16-bit BE mode bus mode.

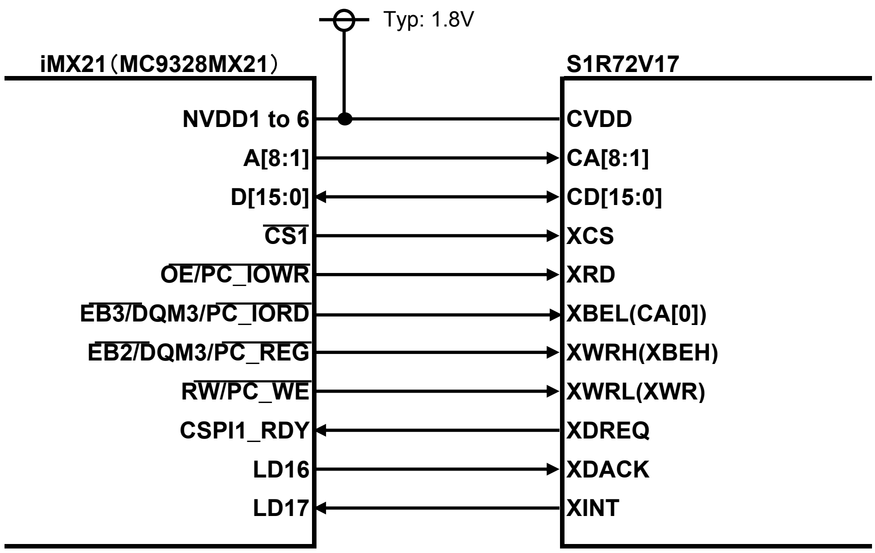


**Fig. 5-1 Connection example with iMX21**

**1) CPU-IF power supply voltage**

In this connection example, the CPU-IF supply voltage is Typ 1.8 V.

iMX21 IO supply voltage (NVDD1 to 6): 1.7 V to 3.3 V

S1R72V17 CPU-IF supply voltage (CVDD): 1.65 V to 3.6 V

**2) iMX21 shared pin settings**

The iMX21 shared pins are set as shown below in this connection example.

**Table 5-1 iMX21 shared pin settings**

| iMX21 pin name | iMX21 pin function |
|---|---|
| NVDD1 to NVDD6 | NVDD1 to NVDD6 |
| A[8:1] | A[8:1] |
| D[15:0] | D[15:0] |
| CS1 | CS1 |
| OE/PC_IOWR | OE |
| EB3/DQM3/PC_IORD | EB3 |
| EB2/DQM2/PC_REG | EB2 |
| RW/PC_WE | RW |
| CSPI1_RDY | EXT_DMAREQ |
| LD16 | EXT_DMAGRANT |
| LD17 | PA23(GPIO used as XINT) |

## 5.2 iMX21 Bus Cycle Setting Example

- **iMX21 clock settings**

  The iMX21 clock settings are set as shown below in this connection example.

  System clock: 264 MHz

  CPU-IF bus clock (HCLK): 88 MHz (system clock 3 divisions)

- **Bus cycle settings**

**CS1U register (0xDF001008 address)** Setting: 0x0402_0700

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SP | WP | DCT | | RWA | | | | PSZ | | PME | SYNC | RWN | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CNC | | WSC | | | | | | EW | WWS | | | EDC | | | |

**CS1L register (0xDF00100C address)** Setting: 0x4200_0D01

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| OEA | | | | OEN | | | | WEA | | | | WEN | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CSA | | | | EBC | DSZ | | | CSN | | | | PSR | CRE | WRAP | CSEN |

**Setting descriptions**

| Register | Setting | Description |
|---|---|---|
| RWA | 4'b0100 | RW output assert timing (2HCLK) |
| SYNC | 1'b0 | Synchronous transfer mode (disabled) |
| RWN | 4'b0010 | RW output negate timing (1HCLK) |
| WSC | 6'b000111 | Access cycle (8HCLK) |
| WWS | 3'b000 | Wait cycle for write (0HCLK) |
| OEA | 4'b0100 | OE output assert timing (2HCLK) |
| OEN | 4'b0010 | OE output negate timing (1HCLK) |
| WEA | 4'b0000 | EBx output assert timing (0HCLK) |
| WEN | 4'b0000 | EBx output negate timing (0HCLK) |
| CSA | 4'b0000 | CS1 output assert timing (0HCLK) |
| EBC | 1'b1 | EB3, 2 output mode for read (disabled) |
| DSZ | 3'b101 | Data bus size (using 16 bits [15:0]) |
| CSN | 4'b0000 | CS1 output assert timing (0HCLK) |
| CSEN | 1'b1 | CS1 enable (enabled) |

**Fig. 5-2 Bus cycle setting registers**

- **Bus cycle waveform**

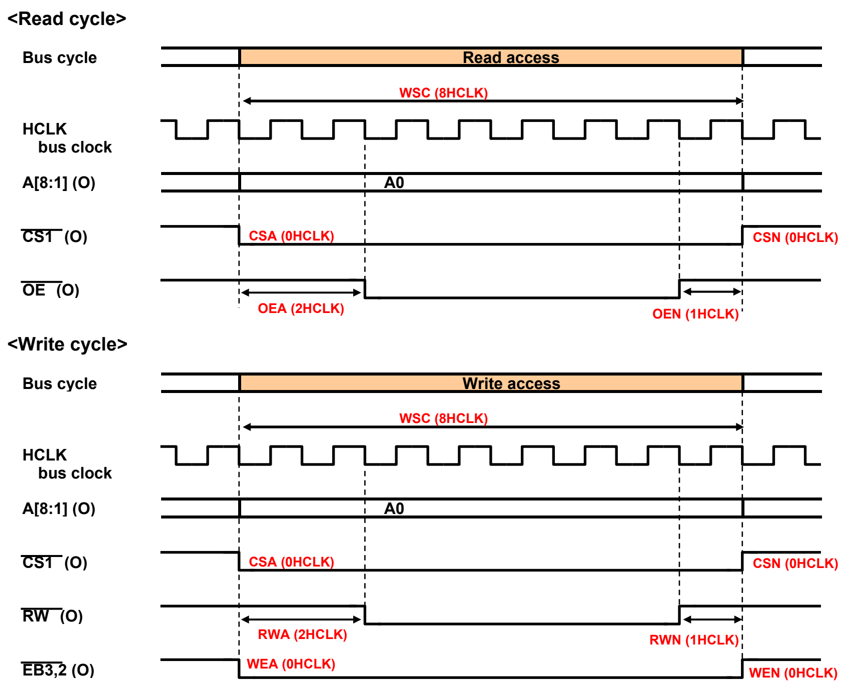


**Fig. 5-3 iMX21 bus cycle waveform**

## 5.3 Checking S1R72V17 AC Spec and iMX21 Bus Cycle

The table below compares S1R72V17 AC specification values to iMX21 bus cycle settings.

For more information on S1R72V17 AC specification, refer to "CPU/DMA IF Access Timing" (8.4.3.1 Basic Cycle) in the *S1R72V17 Technical Manual*.

**Table 5-2 AC Specification Comparison**

| S1R72V17 CPU/DMA IF access timing | | | | iMX21 setting | | |
|---|---|---|---|---|---|---|
| **Code** | **Item** | **min** | **max** | **Cycles** | **unit** | **iMX21 setting register** |
| tcas | Address setup time | 6 | - | 2 | HCLK | RWA, OEA |
| tcah | Address hold time (from strobe negation) | 6 | - | 1 | HCLK | RWN, OEN |
| tsah | Address hold time (from strobe assertion) | 55 | - | 6 | HCLK | WSC-(RWA, OEA) |
| tccs | XCS setup time | 6 | - | 2 | HCLK | RWA, OEA |
| tcch | XCS hold time | 6 | - | 1 | HCLK | RWN, OEN |
| trcy | Read cycle | 80 | - | 8 | HCLK | WSC |
| tras | Read strobe assert time | 40 | - | 5 | HCLK | WSC-(OEA+OEN) |
| trng | Read strobe negate time | 25 | - | 3 | HCLK | OEA+OEN |
| trbd | Read data output start time | 1 | - | — | | |
| trdf | Read data confirmation time | - | 35 | 5 | HCLK | WSC-(OEA+OEN) |
| trdh | Read data hold time | 3 | - | — | | |
| trbh | Read data output delay time | - | 9 | — | | |
| twcy | Write cycle | 80 | - | 8 | HCLK | WSC |
| twas | Write strobe assert time | 40 | - | 5 | HCLK | WSC-(RWA+RWN) |
| twng | Write strobe negate time | 25 | - | 3 | HCLK | RWA+RWN |
| twbs | Write byte enable setup time | 6 | - | 2 | HCLK | RWA |
| twbh | Write byte enable hold time | 6 | - | 1 | HCLK | RWN |
| twds | Write data setup time | 0 | - | 1.5 | HCLK | RWA - 0.5HCLK (data output start) |
| twdh | Write data hold time | 0 | - | 1 | HCLK | RWN |
| tdrn | XDREQ negate delay time | - | 35 | — | | |
| tdaa | XDREQ setup time | 6 | - | — | | |
| tdan | XDREQ hold time | 6 | - | — | | |

( $C_L$=30pf ) 1HCLK=11.36ns (88MHz)

## Revision History

| Date | Revision details | | | |
|---|---|---|---|---|
| | Rev. | Page | Type | Details |
| 06/06/2008 | 1.0 | All | New | Newly created |

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