8-Bit Addressable, DMOS Power Driver

Discontinued Product

These parts are no longer in production The device should not be purchased for new design applications. Samples are no longer available.

Date of status change: October 29, 2007

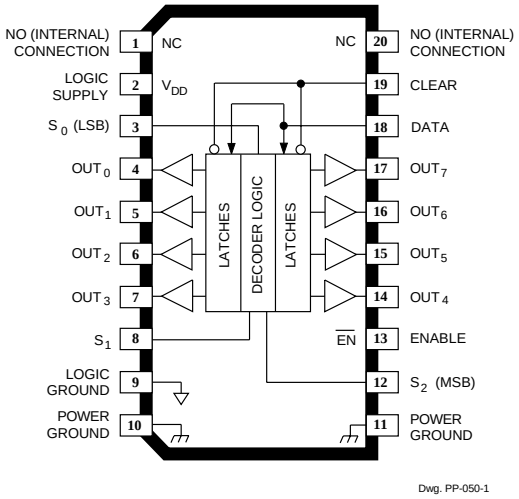
Recommended Substitutions:

NOTE: For detailed information on purchasing options, contact your local Allegro field applications engineer or sales representative.

6B259

Data Sheet
26186.122

8-BIT ADDRESSABLE DMOS POWER DRIVER



Note that the A6B259KA (DIP) and the A6B259KLW (SOIC) are electrically identical and share a common terminal number assignment.

ABSOLUTE MAXIMUM RATINGS at T_A = 25°C

Output Voltage, V_O ..... **50 V**
Output Drain Current,
Continuous, I_O ..... **150 mA***
Peak, I_{OM} ..... **500 mA†**
Single-Pulse Avalanche Energy,
E_{AS} ..... **30 mJ**
Logic Supply Voltage, V_{DD} ..... **7.0 V**
Input Voltage Range,
V_I ..... **-0.3 V to +7.0 V**
Package Power Dissipation,
P_D ..... **See Graph**
Operating Temperature Range,
T_A ..... **-40°C to +125°C**
Storage Temperature Range,
T_S ..... **-55°C to +150°C**

* Each output, all outputs on.

† Pulse duration ≤ 100 µs, duty cycle ≤ 2%.

Caution: These CMOS devices have input static protection (Class 3) but are still susceptible to damage if exposed to extremely high static electrical charges.

The A6B259KA and A6B259KLW combine a 3-to-8 line CMOS decoder and accompanying data latches, control circuitry, and DMOS outputs in a multi-functional power driver capable of storing single-line data in the addressable latches or use as a decoder or demuliplexer. Driver applications include relays, solenoids, and other medium-current or high-voltage peripheral power loads.

The CMOS inputs and latches allow direct interfacing with micro-processor-based systems. Use with TTL may require appropriate pull-up resistors to ensure an input logic high. Four modes of operation are selectable with the CLEAR and ENABLE inputs.

The A6B259KA/KLW DMOS open-drain outputs are capable of sinking up to 500 mA. Similar devices with reduced $r_{DS(on)}$ are available as the A6259KA/KLW.

The A6B259KA is furnished in a 20-pin dual in-line plastic package. The A6B259KLW is furnished in a 20-lead wide-body, small-outline plastic package (SOIC) with gull-wing leads for surface-mount applications. Copper lead frames, reduced supply current requirements, and low on-state resistance allow either device to sink 150 mA from all outputs continuously, to ambient temperatures greater than 85°C.

FEATURES

- 50 V Minimum Output Clamp Voltage
- 150 mA Output Current (all outputs simultaneously)
- 5 Ω Typical $r_{DS(on)}$
- Low Power Consumption
- Replacements for TPIC6B259N and TPIC6B259DW

Always order by complete part number:

Part Number	Package	$R_{\theta JA}$	$R_{\theta JC}$
A6B259KA	20-pin DIP	55°C/W	25°C/W
A6B259KLW	20-lead SOIC	70°C/W	17°C/W

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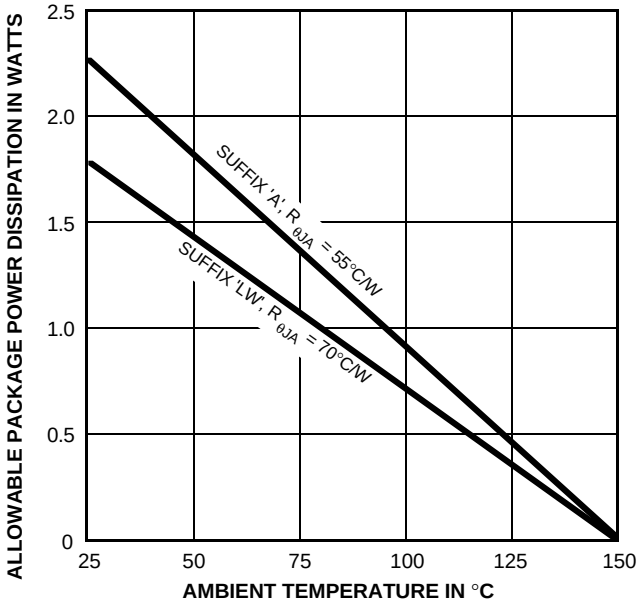
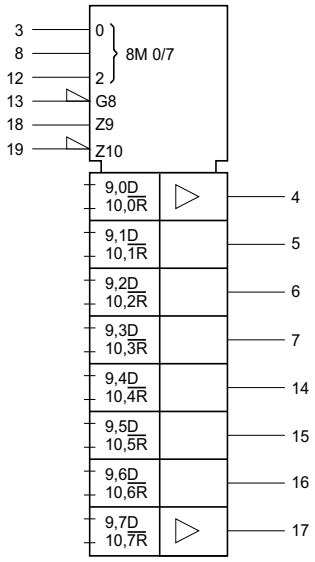
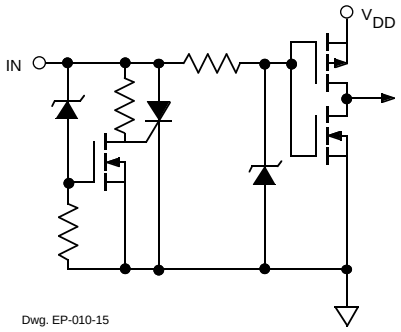


Dwg. GS-004A

LOGIC SYMBOL



Dwg. FP-046



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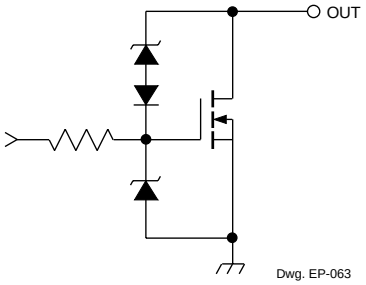
LOGIC INPUTS



Dwg. EP-063

DMOS POWER DRIVER OUTPUT

FUNCTION TABLE

Inputs			Addressed	Other	
CLEAR	ENABLE	DATA	OUTPUT	OUTPUTs	Function
H	L	H	L	R	Addressable Latch
H	L	L	H	R	
H	H	X	R	R	Memory
L	L	H	L	H	8-Line Demultiplexer
L	L	L	H	H	
L	H	X	H	H	Clear

L = Low Logic Level H = High Logic Level X = Irrelevant R = Previous State

LATCH SELECTION TABLE

Select Inputs			Addressed
S_2 (MSB)	S_1	S_0 (LSB)	OUTPUT
L	L	L	0
L	L	H	1
L	H	L	2
L	H	H	3
H	L	L	4
H	L	H	5
H	H	L	6
H	H	H	7

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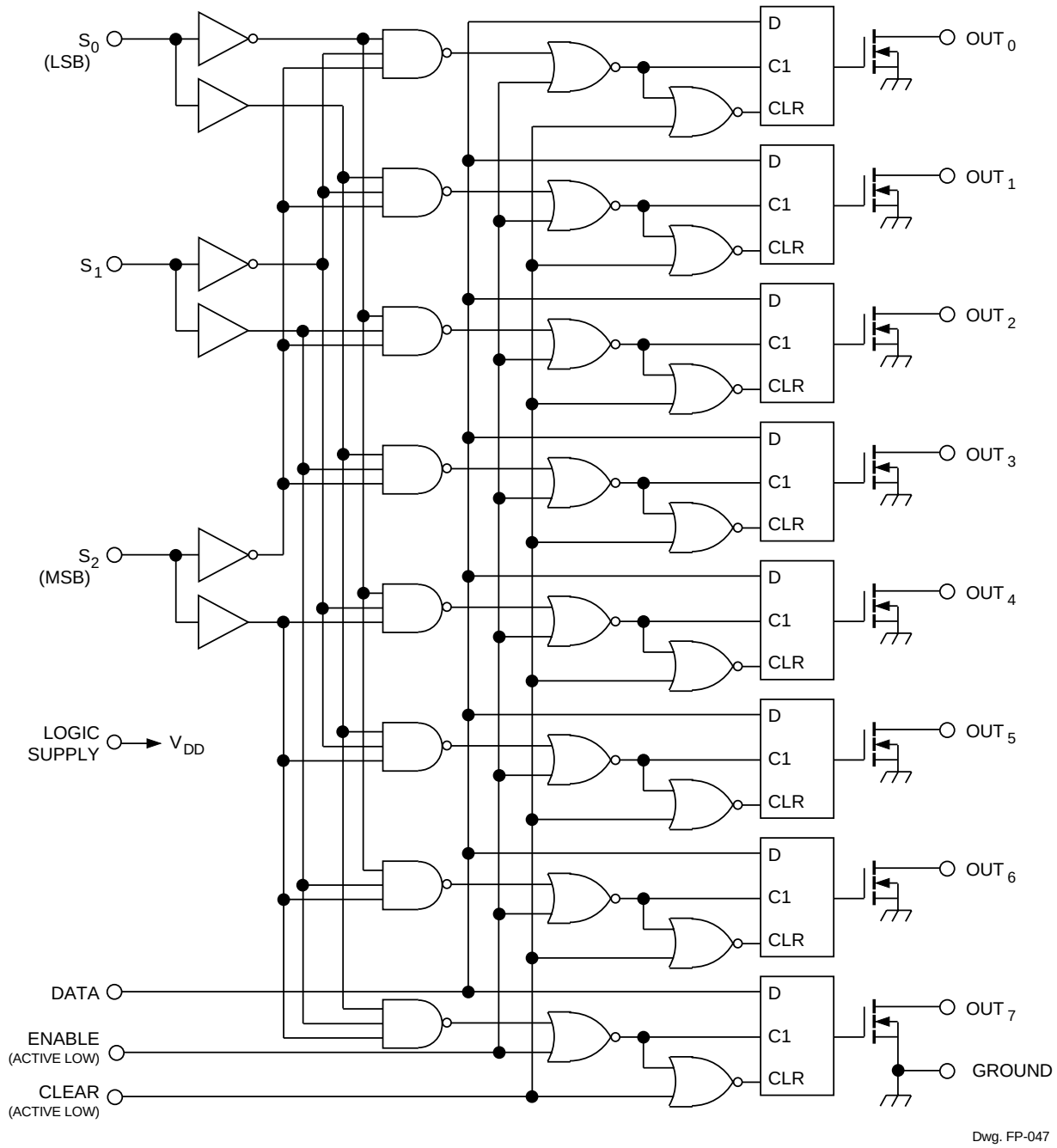
FUNCTIONAL BLOCK DIAGRAM



Grounds (terminals 9, 10, and 11) must be connected externally to a single point.

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RECOMMENDED OPERATING CONDITIONS

over operating temperature range

Logic Supply Voltage Range, V_{DD} ..... 4.5 V to 5.5 V
High-Level Input Voltage, V_{IH} ..... $\geq 0.85V_{DD}$
Low-level input voltage, V_{IL} ..... $\leq 0.15V_{DD}$

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{DD} = 5 V, $t_{ir} = t_{if} \leq 10$ ns (unless otherwise specified).

Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Logic Supply Voltage	V_{DD}	Operating	4.5	5.0	5.5	V
Output Breakdown Voltage	$V_{(BR)DSX}$	I_O = 1 mA	50	—	—	V
Off-State Output Current	I_{DSX}	V_O = 40 V, V_{DD} = 5.5 V	—	0.1	5.0	µA
		V_O = 40 V, V_{DD} = 5.5 V, T_A = 125°C	—	0.15	8.0	µA
Static Drain-Source On-State Resistance	$r_{DS(on)}$	I_O = 100 mA, V_{DD} = 4.5 V	—	4.2	5.7	Ω
		I_O = 100 mA, V_{DD} = 4.5 V, T_A = 125°C	—	6.8	9.5	Ω
		I_O = 350 mA, V_{DD} = 4.5 V (see note)	—	5.5	8.0	Ω
Nominal Output Current	I_{ON}	$V_{DS(on)}$ = 0.5 V, T_A = 85°C	—	90	—	mA
Logic Input Current	I_{IH}	$V_I = V_{DD}$ = 5.5 V	—	—	1.0	µA
	I_{IL}	V_I = 0, V_{DD} = 5.5 V	—	—	-1.0	µA
Prop. Delay Time	t_{PLH}	I_O = 100 mA, C_L = 30 pF	—	150	—	ns
	t_{PHL}	I_O = 100 mA, C_L = 30 pF	—	90	—	ns
Output Rise Time	t_r	I_O = 100 mA, C_L = 30 pF	—	200	—	ns
Output Fall Time	t_f	I_O = 100 mA, C_L = 30 pF	—	200	—	ns
Supply Current	$I_{DD(OFF)}$	V_{DD} = 5.5 V, Outputs off	—	20	100	µA
	$I_{DD(ON)}$	V_{DD} = 5.5 V, Outputs on	—	150	300	µA

Typical Data is at V_{DD} = 5 V and is for design information only.

NOTE — Pulse test, duration ≤100 µs, duty cycle ≤2%.

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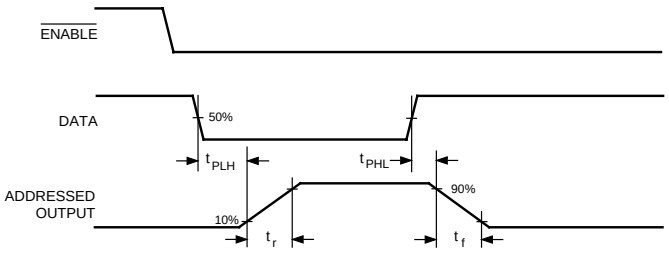
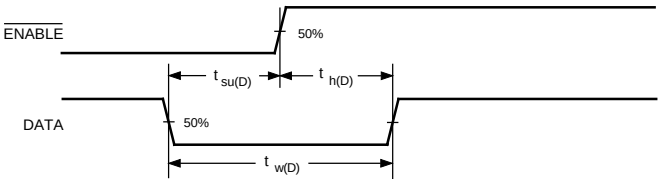
FUNCTIONAL DESCRIPTION and INPUT REQUIREMENTS



Dwg. WP-036

OUTPUT SWITCHING TIME



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DATA INPUT REQUIREMENTS

Data Active Time Before Enable
(Data Set-Up Time), $t_{su(D)}$ ..... **20 ns**
Data Active Time After Enable
(Data Hold Time), $t_{h(D)}$ ..... **20 ns**
Data Pulse Width, $t_{w(D)}$ ..... **40 ns**
Input Logic High, V_{IH} ..... $\geq$ **0.85V_{CC}**
Input Logic Low, V_{IL} ..... $\leq$ **0.15V_{CC}**

Four modes of operation are selectable by controlling the CLEAR and ENABLE inputs as shown above.

In the addressable-latch mode, data at the DATA input is written into the addressed transparent latch. The addressed output inverts the data input with all other outputs remaining in their previous states.

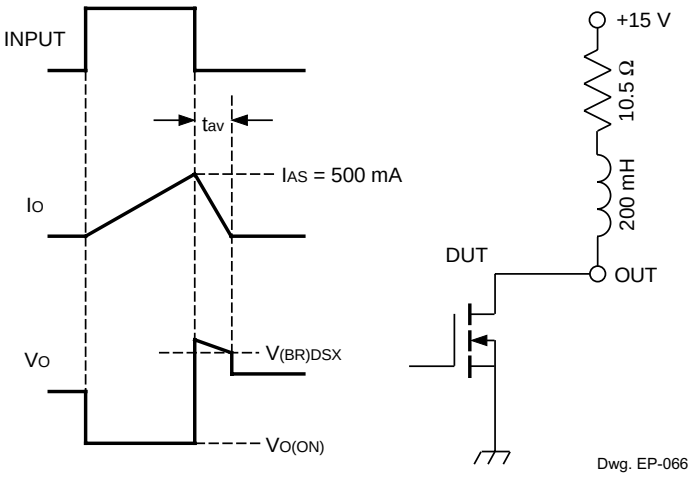
In the memory mode, all outputs remain in their previous states and are unaffected by the DATA or address (S_n) inputs. To prevent entering erroneus data in the latches, ENABLE should be held HIGH while the address lines are changing.

In the demultiplexing/decoding mode, the addressed output inverts the data input and all other outputs are OFF.

In the clear mode, all outputs are OFF and are unaffected by the DATA or address (S_N) inputs.

Given the appropriate inputs, when DATA is LOW for a given address, the output is OFF; when DATA is HIGH, the output is ON and can sink current.

TEST CIRCUITS



$$E_{AS} = I_{AS} \times V_{(BR)DSX} \times t_{AV}/2$$

Single-Pulse Avalanche Energy Test Circuit and Waveforms

TERMINAL DESCRIPTIONS

Terminal No.	Terminal Name	Function
1	NC	No (internal) connection.
2	LOGIC SUPPLY	(V_{DD}) The logic supply voltage (typically 5 V).
3	S_0	Binary-coded output-select input, least-significant bit.
4	OUT_0	Current-sinking, open-drain DMOS output, address 000.
5	OUT_1	Current-sinking, open-drain DMOS output, address 001.
6	OUT_2	Current-sinking, open-drain DMOS output, address 010.
7	OUT_3	Current-sinking, open-drain DMOS output, address 011.
8	S_1	Binary-coded output-select input.
9	LOGIC GROUND	Reference terminal for logic voltage measurements.
10	POWER GROUND	Reference terminal for output voltage measurements (OUT_{0-3}).
11	POWER GROUND	Reference terminal for output voltage measurements (OUT_{4-7}).
12	S_2	Binary-coded output-select input, most-significant bit.
13	ENABLE	Mode control input; see Function Table.
14	OUT_4	Current-sinking, open-drain DMOS output, address 100.
15	OUT_5	Current-sinking, open-drain DMOS output, address 101.
16	OUT_6	Current-sinking, open-drain DMOS output, address 110.
17	OUT_7	Current-sinking, open-drain DMOS output, address 111.
18	DATA	CMOS data input to the addressed output latch. When enabled, the addressed output inverts the data input (DATA = HIGH, OUTPUT = LOW).
19	CLEAR	Mode control input; see Function Table.
20	NC	No (internal) connection.

NOTE — Grounds (terminals 9, 10, and 11) must be connected externally to a single point.

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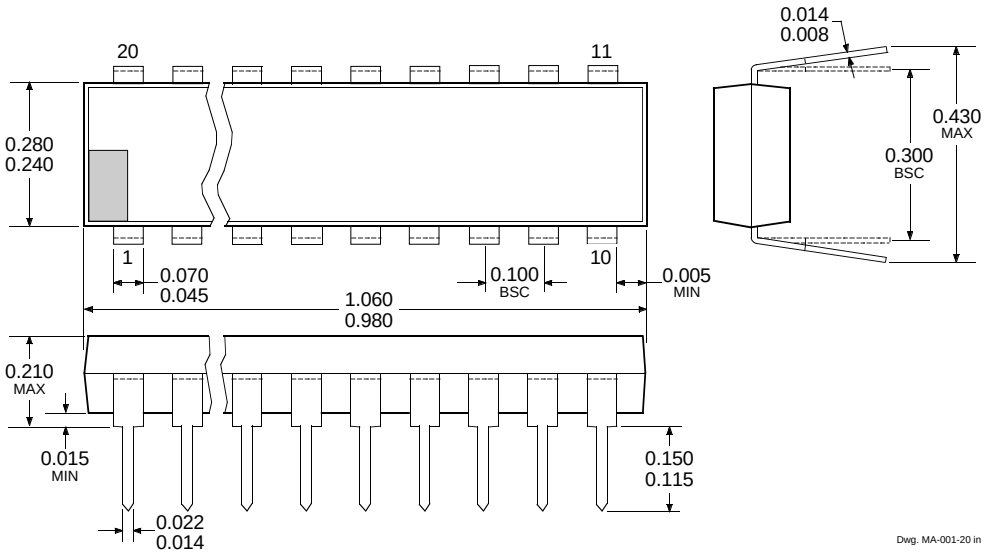
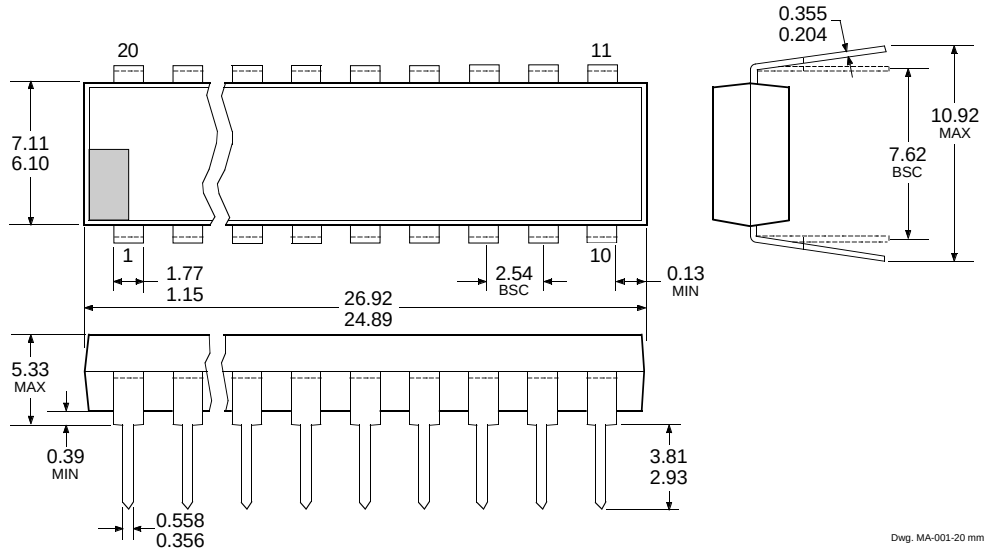
A6B259KA

Dimensions in Inches
(controlling dimensions)



Dimensions in Millimeters
(for reference only)



NOTES: 1. Exact body and lead configuration at vendor's option within limits shown.
2. Lead spacing tolerance is non-cumulative.
3. Lead thickness is measured at seating plane or below.

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A6B259KLW

Dimensions in Inches
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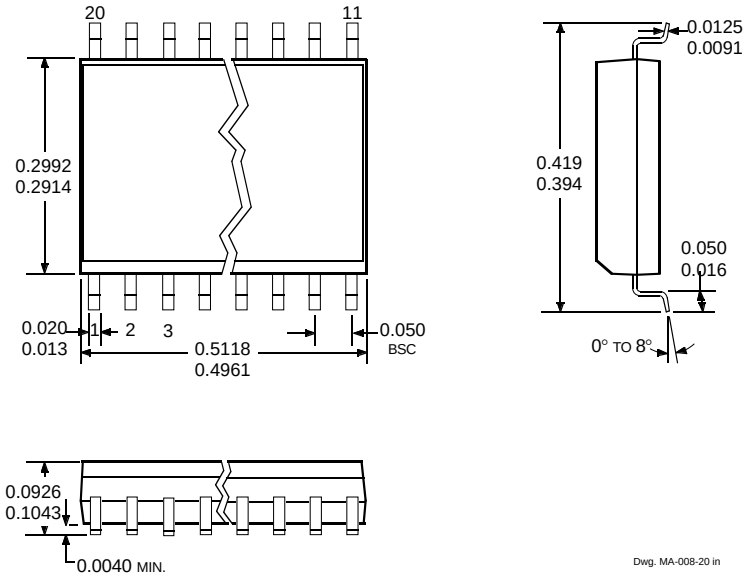
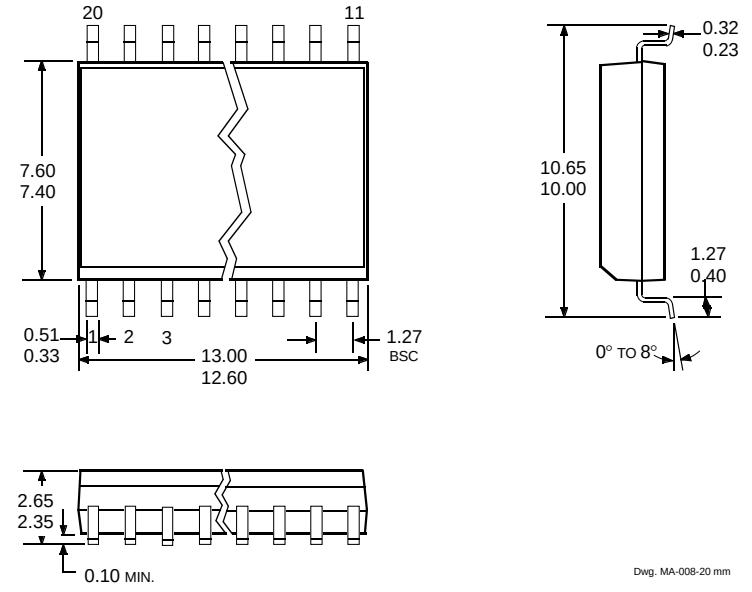


Dwg. MA-008-20 in

Dimensions in Millimeters
(controlling dimensions)



Dwg. MA-008-20 mm

NOTES: 1. Exact body and lead configuration at vendor's option within limits shown.
2. Lead spacing tolerance is non-cumulative.

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