Evaluating the LT3041 20 V, 1 A, Ultra-Low Noise, Ultra-High PSRR Linear Regulator with VIOC Control

FEATURES

- Input voltage range: 3.8 V to 20 V
- Resistor-programmed 3.32 V output voltage
- Maximum output current: 1 A
- BNC connectors for noise and PSRR measurement
- Resistor programmed power-good
- Resistor-programmable current limit, current monitoring, and UV-LO
- VIOC to manage power dissipation and PSRR
- Thermally enhanced, 14-lead, 3 mm × 4 mm, DFN package

EVALUATION KIT CONTENTS

- DC3158A evaluation board

EQUIPMENT NEEDED

- A DC power supply
- Multimeters for voltage and current measurements
- Electronic or resistive loads

DOCUMENTS NEEDED

- LT3041 data sheet

EVALUATION BOARD PHOTOGRAPH

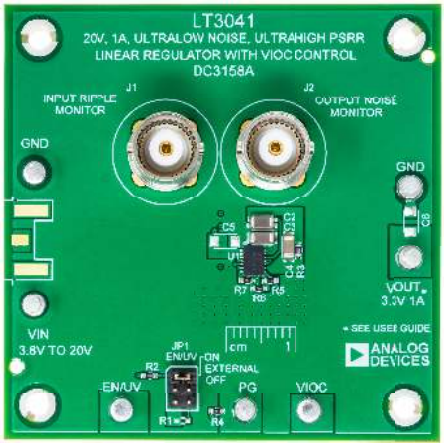

Figure 1. DC3158A Evaluation Board Photograph

GENERAL DESCRIPTION

The DC3158A evaluation board features the LT3041, a 20 V, 1 A, ultra-low noise and ultra-high power-supply rejection ratio (PSRR), low-dropout (LDO) linear regulator that incorporates voltage input-to-output control (VIOC) tracking. VIOC allows control of the upstream switching converter to maintain a constant voltage across the LT3041 and, therefore, minimizes power dissipation and maintains PSRR.

The DC3158A operates over an input voltage range of 3.8 V to 20 V. The LT3041 delivers a maximum output current of 1 A. In addition to featuring ultra-low noise and ultra-high PSRR, the regulator offers programmable power-good functionality and a programmable current limit. Current monitoring is also achieved by sensing the ILIM pin voltage.

Built-in protection includes reverse-battery protection, reverse-current protection, internal current limit with foldback and thermal limit with hysteresis.

For full details on the LT3041, see the LT3041 data sheet, which must be consulted with this user guide when using the DC3158A evaluation board.

The LT3041 of the DC3158A features a 14-lead, 3 mm × 4 mm, plastic DFN package with an exposed pad on the bottom side of the IC. Proper board layout is essential for maximum thermal performance.

Design files are available on the DC3158A evaluation board page.

TABLE OF CONTENTS

REVISION HISTORY

10/2022—Revision 0: Initial Version

PERFORMANCE SUMMARY

Specifications are at T_A = 25°C, unless otherwise noted.

Table 1. Performance Summary

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT VOLTAGE RANGE	V_{IN}	Output current (I_{OUT}) = 150 mA, V_{OUT} = 3.3 V	3.8		20	V
		I_{OUT} = 1 A, V_{OUT} = 3.3 V	3.8		5.8[1]	V
OUTPUT VOLTAGE	V_{OUT}	V_{IN} = 5 V, I_{OUT} = 1 A, R3 = 33.2 kΩ	3.25	3.32	3.39	V
SHUTDOWN INPUT CURRENT	I_{IN}	JP1 = off, R4 = open, V_{IN} = 6 V		18		µA

[1] The maximum power dissipation and, consequently, the maximum input voltage for a 1 A load current is set by the 60°C temperature rise of the LT3041 on the evaluation board. Higher input voltages can be reached if larger copper area or forced-air cooling is applied. In addition, consider the effect of ambient temperature and the maximum junction temperature that may occur. The LT3041 limits output current at higher input-to-output voltage differentials. See the LT3041 data sheet for more information.

QUICK START PROCEDURE

The DC3158A evaluation board is simple to set up to evaluate the performance of the LT3041. Refer to Figure 2 for the proper measurement equipment setup and take the following steps:

1. Connect a load between the VOUT and GND terminals.
2. With power off, connect the input power supply to the VIN and GND terminals.
3. Ensure that the shunt of JP1 is in the **ON** position.
4. With the load turned down, turn the input power supply on, and ensure that the voltage is between 3.8 V and 20 V.
5. Vary V_{IN} from 3.8 V to 20 V and vary the load current from 0 A to 1 A. Note the following when setting V_{IN} and the load current:
   - An input voltage that is too close to the programmed output voltage (too low) may cause dropout operation and a loss of output-voltage regulation.
   - The amount of output current combined with an input voltage that is too high above the output may increase power dissipation to an unacceptable level.
   - The LT3041 limits output current at higher input-to-output voltage differentials (refer to the LT3041 data sheet for more information).
6. Refer to Application Note 83 and Application Note AN159 for measuring the output noise and PSRR. Note that, J1 and J2 are Bayonet Neill–Concelman (BNC) connectors that are used for noise and PSRR measurements.
7. With JP1 in the **ON** position, R1 and R2 can be used to set an accurate undervoltage lockout (UVLO) threshold.
8. Change to a suitable ILIM resistor (R7) to program a current limit and provide output current monitoring at the resistor or pin.
9. Refer to the data sheet for the usage of the VIOC terminal.
10. In addition, change the PGFB divider resistors (R5 and R6) if the SET resistor (R3) is changed. Monitor power good at the PG terminal.

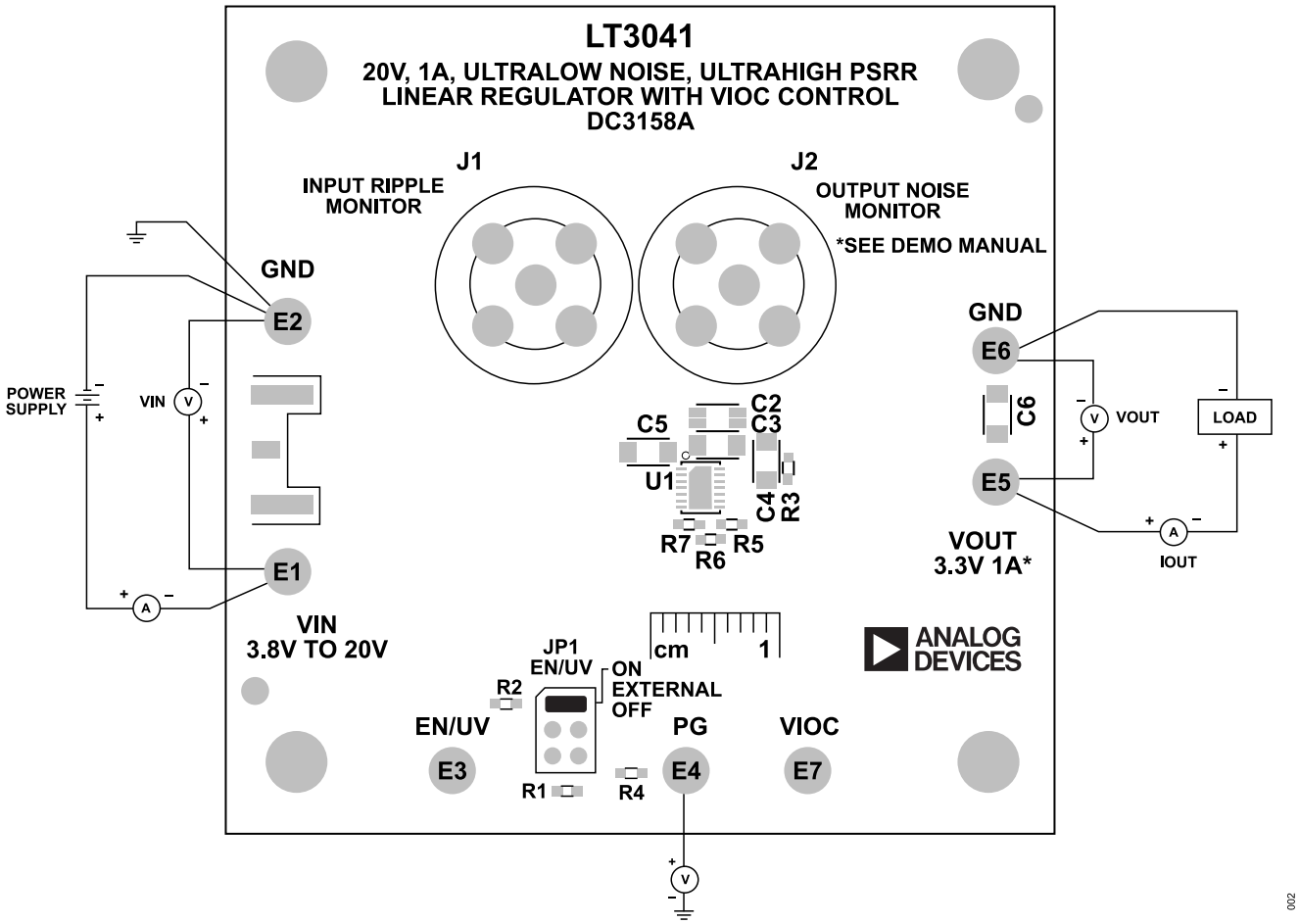

Figure 2. Proper Measurement Equipment Setup for DC3158A

PRINTED CIRCUIT BOARD (PCB) LAYOUT

BEST PSRR PERFORMANCE: PCB LAYOUT FOR INPUT TRACES

For applications using the LT3041 for post-regulating switching converters, placing a capacitor directly at the LT3041 input results in AC current (at the switching frequency) flowing near the LT3041. Without careful attention to PCB layout, this relatively high-frequency switching current generates an electromagnetic field (EMF) that couples to the LT3041 output, degrading its effective PSRR. Highly dependent on the PCB, the switching preregulator, and the input capacitor size, among other factors, the PSRR degradation can easily be 30 dB at 1 MHz. This degradation is present even if the LT3041 is desoldered from the board because it effectively degrades the PSRR of the PCB itself. While negligible for conventional low PSRR LDO regulators, the ultra-high PSRR of the LT3041 requires careful attention to higher-order parasitics to realize the full performance offered by the regulator.

The LT3041 evaluation board alleviates this degradation in PSRR by using a specialized layout technique. The V_{IN} input trace and its corresponding return path (GND) are highlighted in red in Figure 3 and Figure 4. Figure 4 also shows the location of the C1 input capacitor. Normally, when AC voltages are applied to the inputs of the board, AC current flows on the input and return paths, thus generating an electromagnetic field (EMF). This EMF couples to the C2 and C3 output capacitors and the related traces, making the PSRR appear worse than it actually is. With the input trace directly above the return path, the EMFs are in opposite directions, and consequently, cancel each other out. Making sure that these traces exactly overlap each other maximizes the cancellation effect and thus provides the maximum PSRR offered by the regulator.

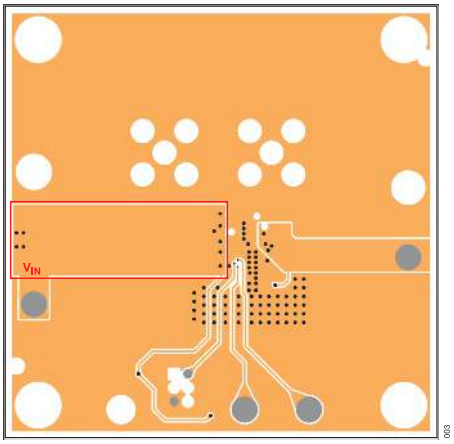

Figure 3. Layer 3 of DC3158A

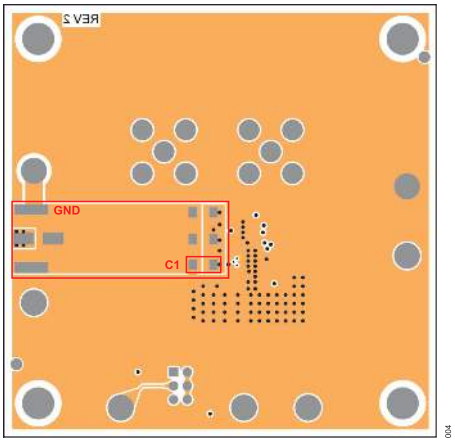

Figure 4. Layer 4 of DC3158A

PRINTED CIRCUIT BOARD (PCB) LAYOUT

BEST AC PERFORMANCE: PCB LAYOUT FOR OUTPUT CAPACITOR C2

For ultra-high PSRR performance, the LT3041 bandwidth is quite high (~750 kHz), making it close to the self-resonance frequency (~1.6 MHz) of the output capacitor. Therefore, it is important to avoid adding extra impedance (effective-series inductance (ESL) and effective-series resistance (ESR)) outside the feedback loop. To achieve this avoidance, minimize the effects of the PCB trace and solder inductance by Kelvin connecting the output sense pin (OUTS) and the SET pin capacitor (C_{SET}) GND directly to the terminals of the output capacitor (C2) using a split capacitor technique, as shown in Figure 5 and Figure 6. With only small AC current flowing through these connections, the impact of the solder joint and/or PCB trace inductance on stability is eliminated. While the LT3041 is robust enough not to oscillate if the recommended layout is not followed, phase and gain margin and stability degrade.

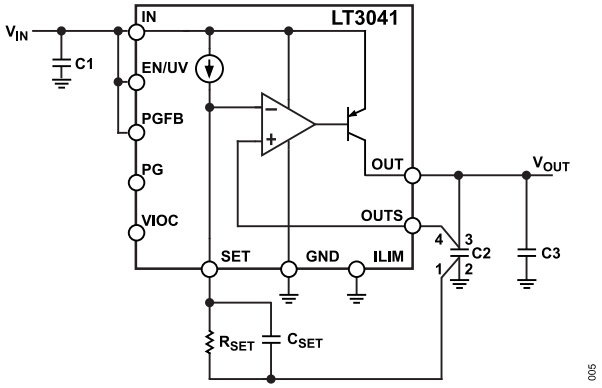

Figure 5. C2 and C_{SET} Connections for Best Performance

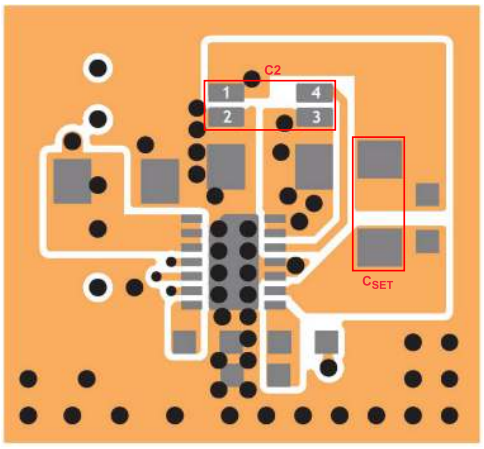

Figure 6. Split Pads for C2 on the Top Layer of DC3158A

EVALUATION BOARD SCHEMATIC

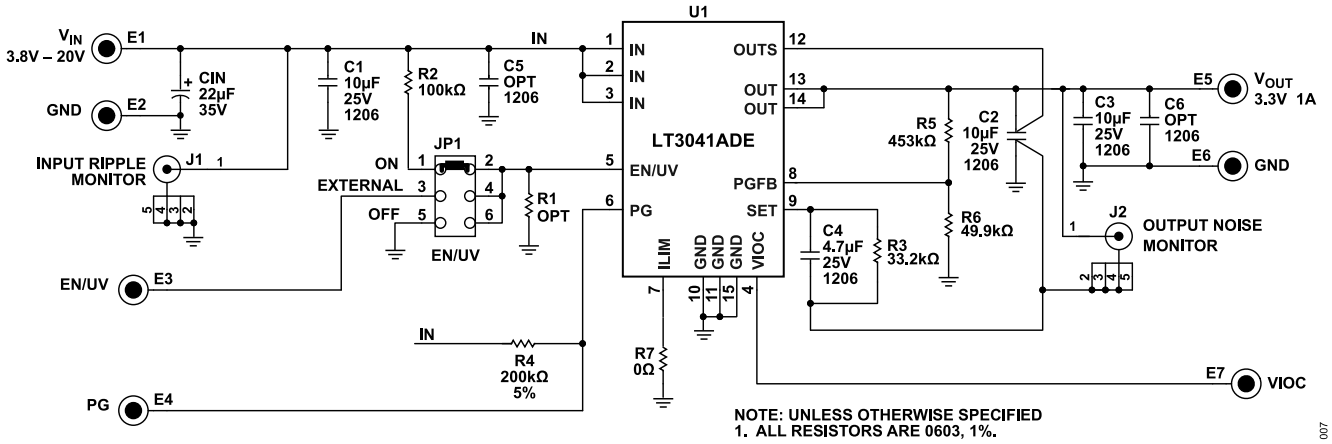

Figure 7. Evaluation Board Schematic

ORDERING INFORMATION

BILL OF MATERIALS

Table 2. Bill of Materials

Item	Quantity	Reference Designator	Part Description	Manufacturer, Part Number
Required Circuit Components				
1	1	C1	10 µF capacitor, X7R, 25 V, 10%, 1206	KEMET, C1206C106K3RACAUTO
2	2	C2, C3	10 µF capacitors, X7S, 25 V, 10%, 1206	Murata, GCM31CC71E106KA03L
3	1	C4	4.7 µF capacitor, X7R, 25 V, 10%, 1206	Murata, GCJ31CR71E475KA12L
4	1	R3	33.2 kΩ resistor, 1%, 1/10 W, 0603	Vishay, CRCW060333K2FKEA
5	1	U1	20 V, 1 A, ultra-low noise, ultra-high PSRR, linear regulator with VIOC control	Analog Devices, Inc., LT3041ADE#PBF-ES
Optional Evaluation Board Components				
1	1	CIN	22 µF capacitor, 35 V, 20%, 5 mm × 5.4 mm	Sun Electronic Industries, 35CE22BSS
2	0	C5, C6	Capacitors, 1206, optional	
3	1	R7	0 Ω, 1/10 W, 0603, AEC-Q200	Vishay, CRCW06030000Z0EA
4	1	R5	453 kΩ resistor, 1%, 1/10 W, 0603	Vishay, CRCW0603453KFKEA
5	1	R6	49.9 kΩ resistor, 1%,1/10 W, 0603	Vishay, CRCW060349K9FKEA
6	1	R2	100 kΩ resistor, 1%, 1/10 W, 0603	Vishay, CRCW0603100KFKEA
7	1	R4	200 kΩ resistor, 5%, 1/10 W, 0603	Vishay, CRCW0603200KJNEA
8	0	R1	Resistor, 0603, optional	
Hardware				
1	7	E1 to E7	Test points, turret, 0.094" PBF	Mill-Max, 2501-2-00-80-00-00-07-0
2	2	J1, J2	Connector, RF, BNC, receptacle, jack, 5-pin, straight, through-hole, 50 Ω	Amphenol RF, 112404
3	1	JP1	Connector, header, male, 2 × 3, 2 mm, vertical, straight, through-hole	Wurth Elektronik, 62000621121
4	1	XJP1	Connector, shunt, female, 2 position, 2 mm	Wurth Elektronik, 60800213421
5	4	MP1 to MP4	Standoff, nylon, snap-on, 6.4 mm	Wurth Elektronik, 702931000

ORDERING INFORMATION

NOTES

ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.