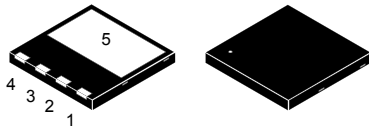
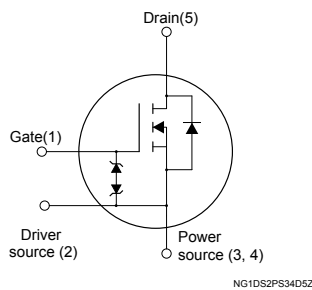


## N-channel 600 V, 0.115 $\Omega$ typ., 22 A MDmesh M2 Power MOSFET in a PowerFLAT 8x8 HV package



PowerFLAT 8x8 HV



### Features

Order code	$V_{DS} @ T_{Jmax}$	$R_{DS(on)max}$	$I_D$
STL33N60M2	650 V	0.135 $\Omega$	22 A

- Extremely low gate charge
- Excellent output capacitance ( $C_{OSS}$ ) profile
- 100% avalanche tested
- Zener-protected

### Applications

- Switching applications
- LLC converters, resonant converters

### Description

This device is an N-channel Power MOSFET developed using MDmesh M2 technology. Thanks to its strip layout and an improved vertical structure, the device exhibits low on-resistance and optimized switching characteristics, rendering it suitable for the most demanding high efficiency converters.



#### Product status link

[STL33N60M2](#)

#### Product summary

<b>Order code</b>	STL33N60M2
<b>Marking</b>	33N60M2
<b>Package</b>	PowerFLAT™ 8x8 HV
<b>Packing</b>	Tape & reel

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{GS}$	Gate-source voltage	$\pm 25$	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	22	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	13.8	A
$I_{DM}^{(2)}$	Drain current (pulsed)	88	A
$P_{TOT}$	Total power dissipation at $T_C = 25\text{ }^\circ\text{C}$	150	W
$I_{AR}$	Avalanche current, repetitive or not-repetitive (pulse width limited by $T_j$ max)	5	A
$E_{AS}$	Single pulse avalanche energy (starting $T_j = 25\text{ }^\circ\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{ V}$ )	450	mJ
$dv/dt^{(3)}$	Peak diode recovery voltage slope	15	V/ns
$dv/dt^{(4)}$	MOSFET $dv/dt$ ruggedness	50	V/ns
$T_{stg}$	Storage temperature range	- 55 to 150	$^\circ\text{C}$
$T_j$	Operating junction temperature range	150	$^\circ\text{C}$

1. The value is limited by package.
2. Pulse width limited by safe operating area.
3.  $I_{SD} \leq 22\text{ A}$ ,  $di/dt \leq 400\text{ A}/\mu\text{s}$ ,  $V_{DS(\text{peak})} < V_{(BR)DSS}$ ,  $V_{DD} = 400\text{ V}$ .
4.  $V_{DS} \leq 480\text{ V}$ .

**Table 2. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj\text{-case}}$	Thermal resistance junction-case	0.83	$^\circ\text{C}/\text{W}$
$R_{thj\text{-pcb}}^{(1)}$	Thermal resistance junction-pcb	45	$^\circ\text{C}/\text{W}$

1. When mounted on FR-4 board of 1 inch<sup>2</sup>, 2oz Cu.

## 2 Electrical characteristics

( $T_C = 25\text{ °C}$  unless otherwise specified)

**Table 3. On /off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$ , $I_D = 1\text{ mA}$	600			V
$I_{DSS}$	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$ , $V_{DS} = 600\text{ V}$			1	$\mu\text{A}$
		$V_{GS} = 0\text{ V}$ , $V_{DS} = 600\text{ V}$ , $T_C = 125\text{ °C}$ <sup>(1)</sup>			100	$\mu\text{A}$
$I_{GSS}$	Gate-body leakage current	$V_{DS} = 0\text{ V}$ , $V_{GS} = \pm 25\text{ V}$			$\pm 10$	$\mu\text{A}$
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static drain-source on- resistance	$V_{GS} = 10\text{ V}$ , $I_D = 11\text{ A}$		0.115	0.135	$\Omega$

1. Defined by design, not subject to production test.

**Table 4. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 100\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0\text{ V}$	-	1781	-	pF
$C_{oss}$	Output capacitance		-	85	-	pF
$C_{rss}$	Reverse transfer capacitance		-	2.5	-	pF
$C_{oss\text{ eq.}}$ <sup>(1)</sup>	Equivalent output capacitance	$V_{DS} = 0$ to $480\text{ V}$ , $V_{GS} = 0\text{ V}$	-	135	-	pF
$R_G$	Intrinsic gate resistance	$f = 1\text{ MHz}$ open drain	-	5.2	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 480\text{ V}$ , $I_D = 26\text{ A}$	-	45.5	-	nC
$Q_{gs}$	Gate-source charge	$V_{GS} = 0$ to $10\text{ V}$	-	9.9	-	nC
$Q_{gd}$	Gate-drain charge	(see Figure 15. Gate charge test circuit)	-	18.5	-	nC

1.  $C_{oss\text{ eq.}}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$ .

**Table 5. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300\text{ V}$ , $I_D = 13\text{ A}$	-	16	-	ns
$t_r$	Rise time	$R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$	-	9.6	-	ns
$t_{d(off)}$	Turn-off delay time	(see Figure 14. Switching times test circuit for resistive load and Figure 19. Switching time waveform)	-	109	-	ns
$t_f$	Fall time		-	9	-	ns

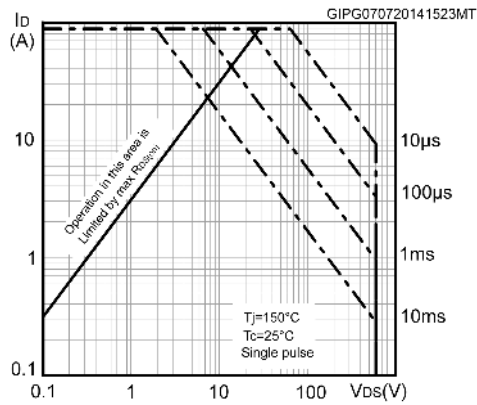
**Table 6. Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		22	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		88	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 22\text{ A}, V_{GS} = 0\text{ V}$	-		1.6	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 26\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$	-	375		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 60\text{ V}$ (see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	5.6		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	30		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 26\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$	-	478		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 60\text{ V}, T_j = 150\text{ }^\circ\text{C}$ (see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	7.7		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	32.5		A

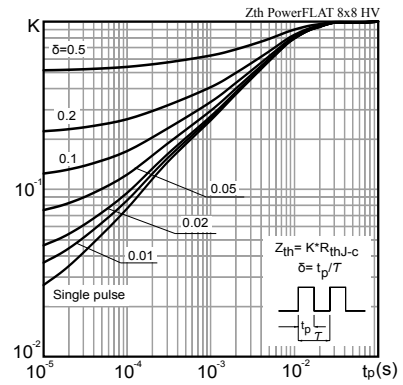
1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%.

## 2.1 Electrical characteristics (curves)

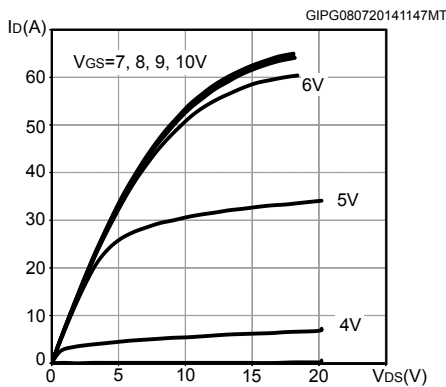
**Figure 1. Safe operating area**



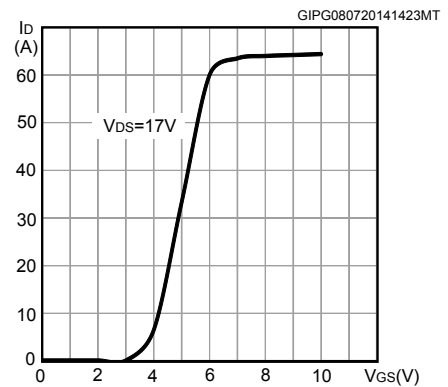
**Figure 2. Thermal impedance**



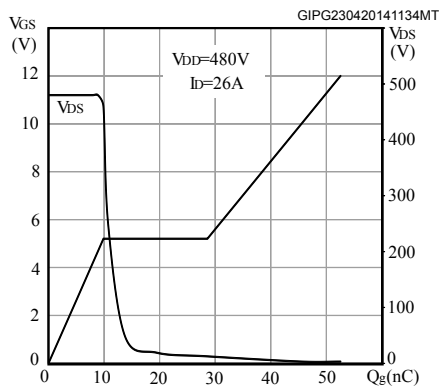
**Figure 3. Output characteristics**



**Figure 4. Transfer characteristics**



**Figure 5. Gate charge vs gate-source voltage**



**Figure 6. Static drain-source on-resistance**

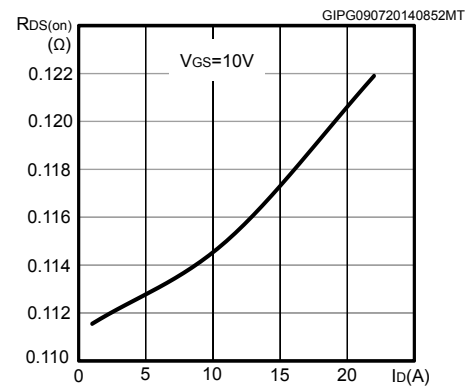


Figure 7. Capacitance variations

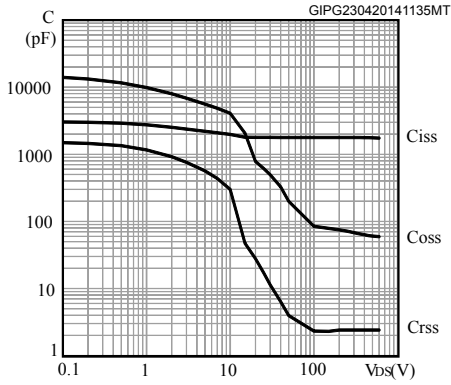


Figure 8. Normalized gate threshold voltage vs temperature

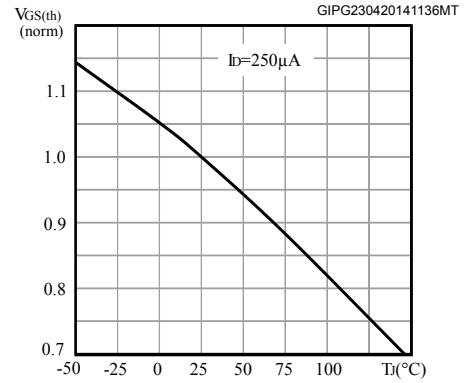


Figure 9. Normalized on-resistance vs temperature

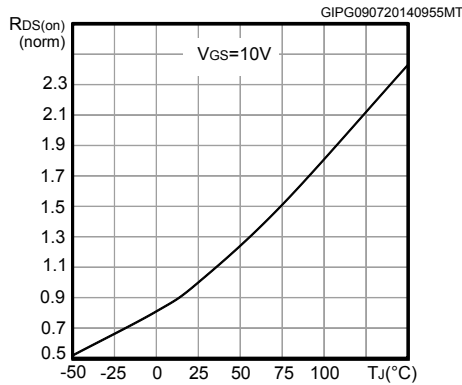


Figure 10. Normalized  $V_{(BR)DSS}$  vs temperature

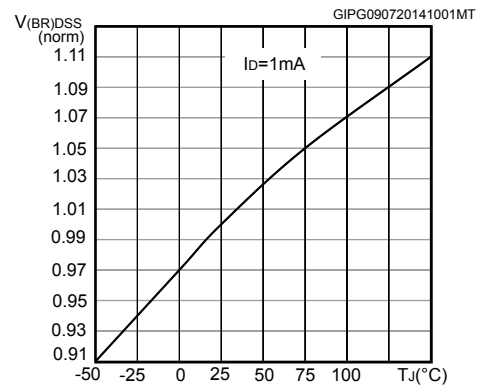


Figure 11. Source-drain diode forward characteristics

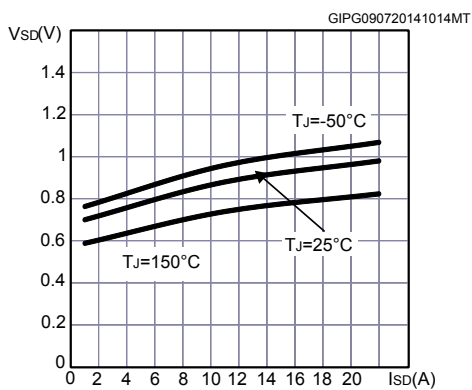
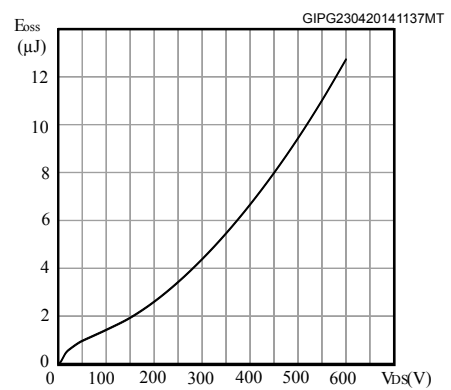
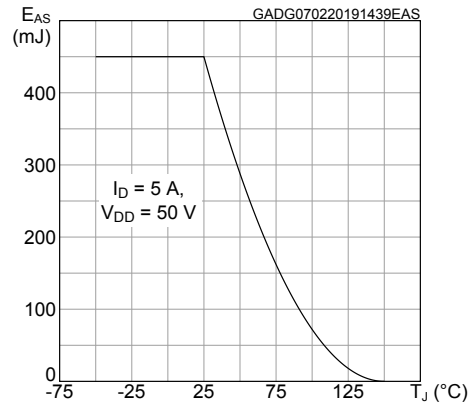


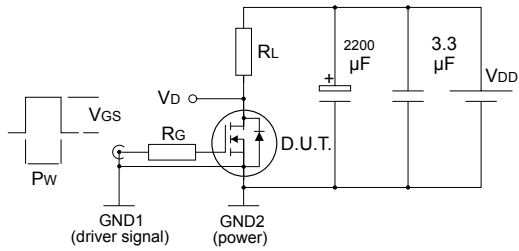
Figure 12. Output capacitance stored energy



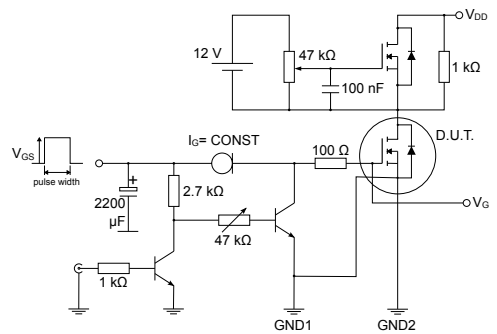
**Figure 13. Maximum avalanche energy vs temperature**



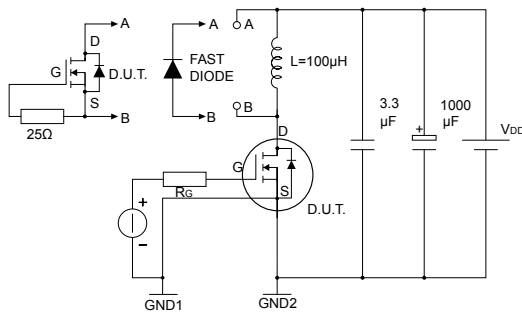
### 3 Test circuits

**Figure 14. Switching times test circuit for resistive load**


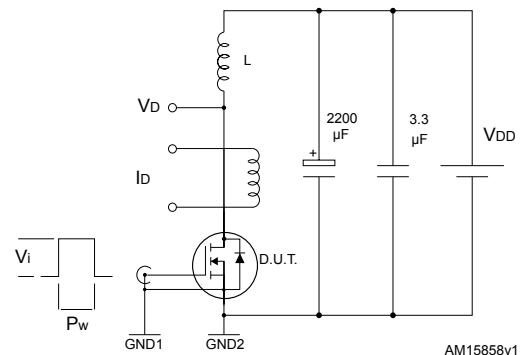
AM15855v1

**Figure 15. Gate charge test circuit**


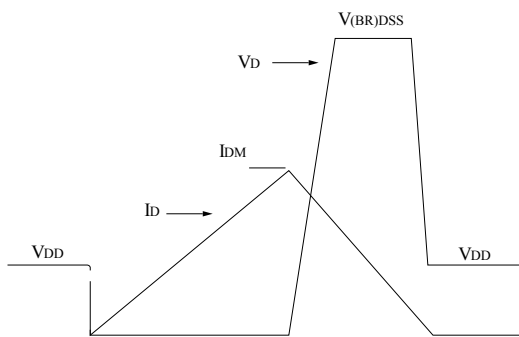
AM01469v2

**Figure 16. Test circuit for inductive load switching and diode recovery times**


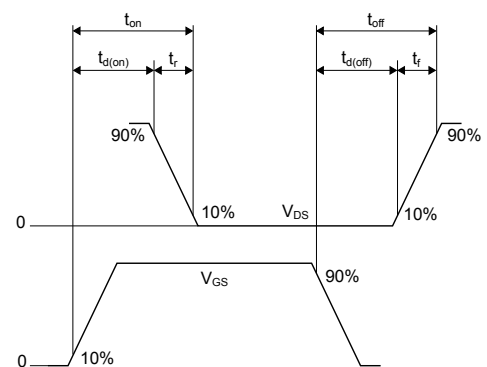
AM15857v1

**Figure 17. Unclamped inductive load test circuit**


AM15858v1

**Figure 18. Unclamped inductive waveform**


AM01472v1

**Figure 19. Switching time waveform**


AM01473v1

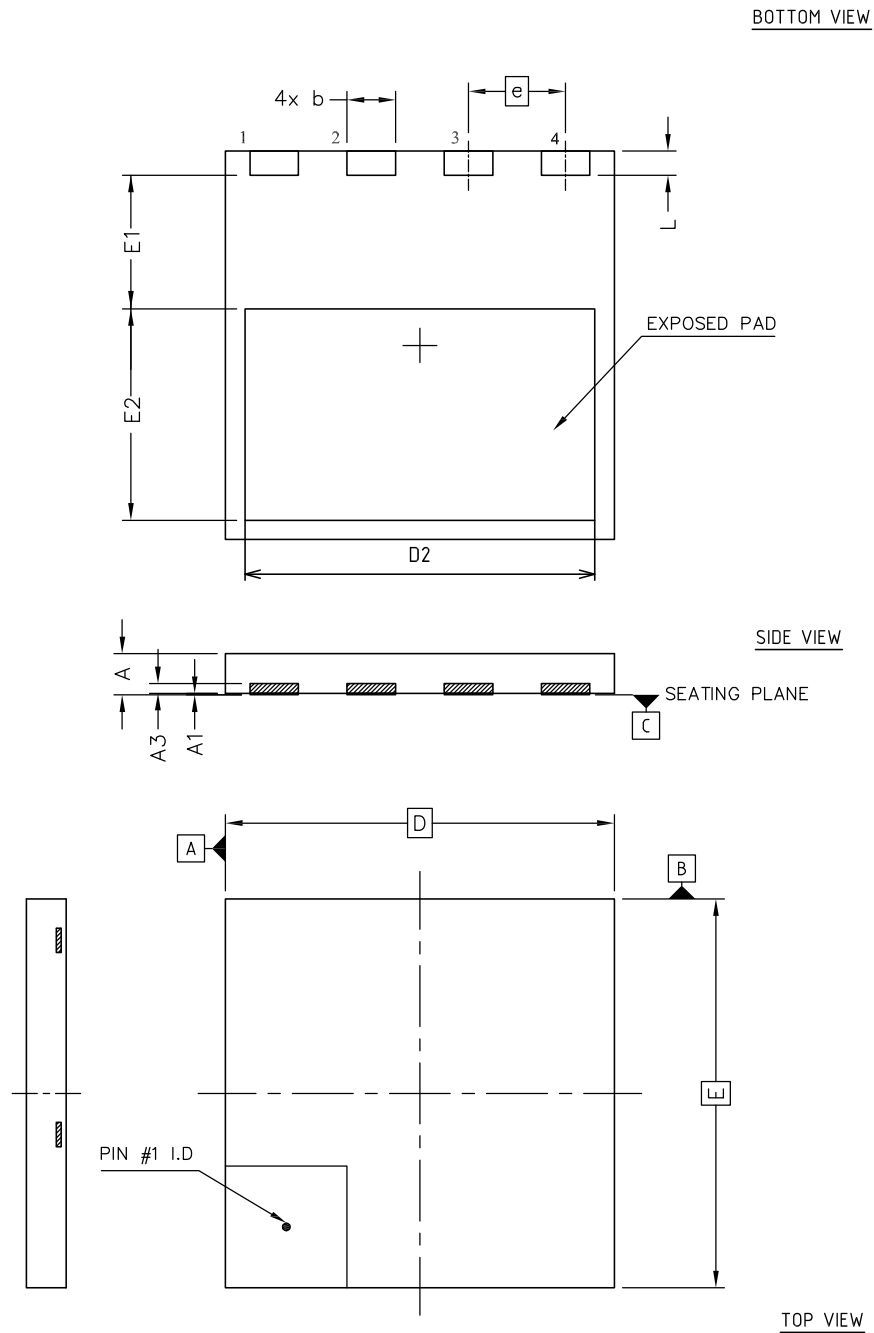


## 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

### 4.1 PowerFLAT 8x8 HV package information

**Figure 20. PowerFLAT 8x8 HV package outline**

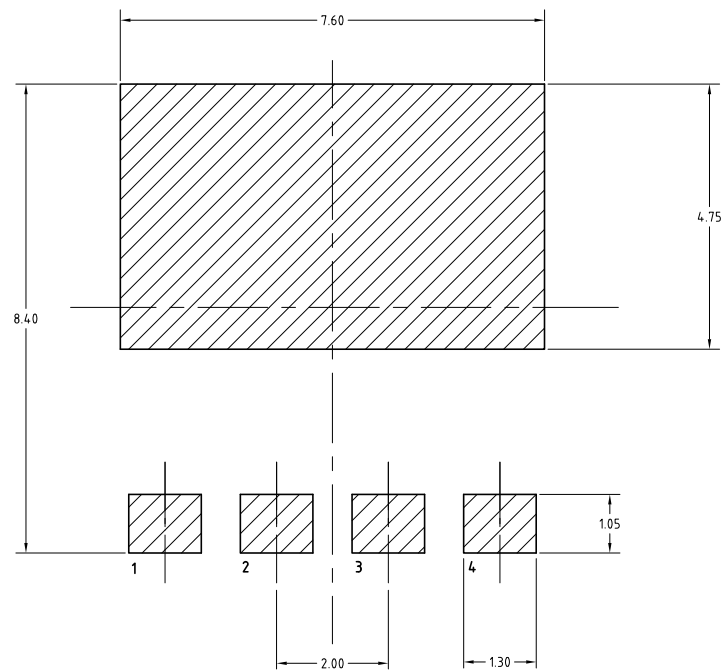


8222871\_Rev\_4

**Table 7. PowerFLAT 8x8 HV mechanical data**

Ref.	Dimensions (in mm)		
	Min.	Typ.	Max.
A	0.75	0.85	0.95
A1	0.00		0.05
A3	0.10	0.20	0.30
b	0.90	1.00	1.10
D	7.90	8.00	8.10
E	7.90	8.00	8.10
D2	7.10	7.20	7.30
E1	2.65	2.75	2.85
E2	4.25	4.35	4.45
e	2.00 BSC		
L	0.40	0.50	0.60

**Figure 21. PowerFLAT 8x8 HV footprint**

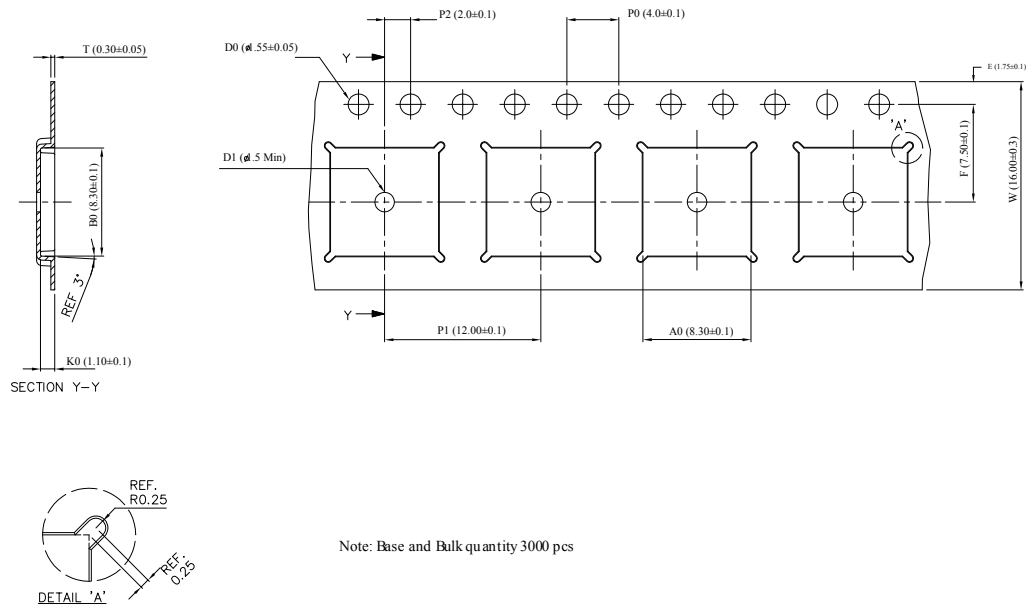


8222871\_REV\_4\_footprint

*Note: All dimensions are in millimeters.*

## 4.2 PowerFLAT 8x8 HV packing information

Figure 22. PowerFLAT 8x8 HV tape



8229819\_Tape\_revA

Note: All dimensions are in millimeters.

Figure 23. PowerFLAT 8x8 HV package orientation in carrier tape

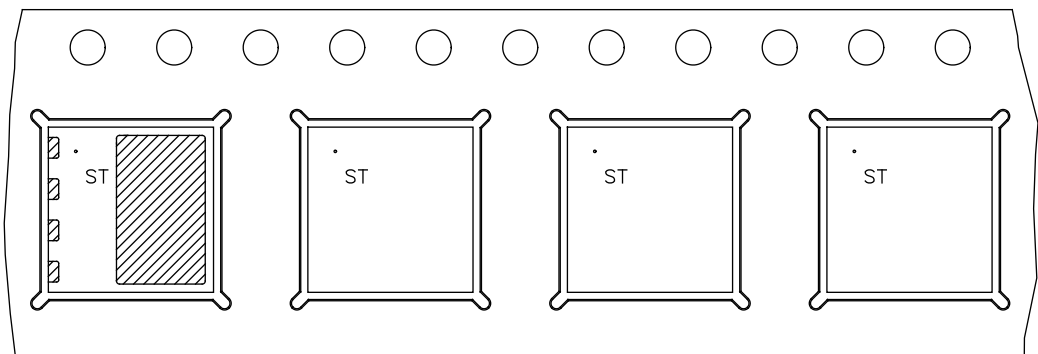
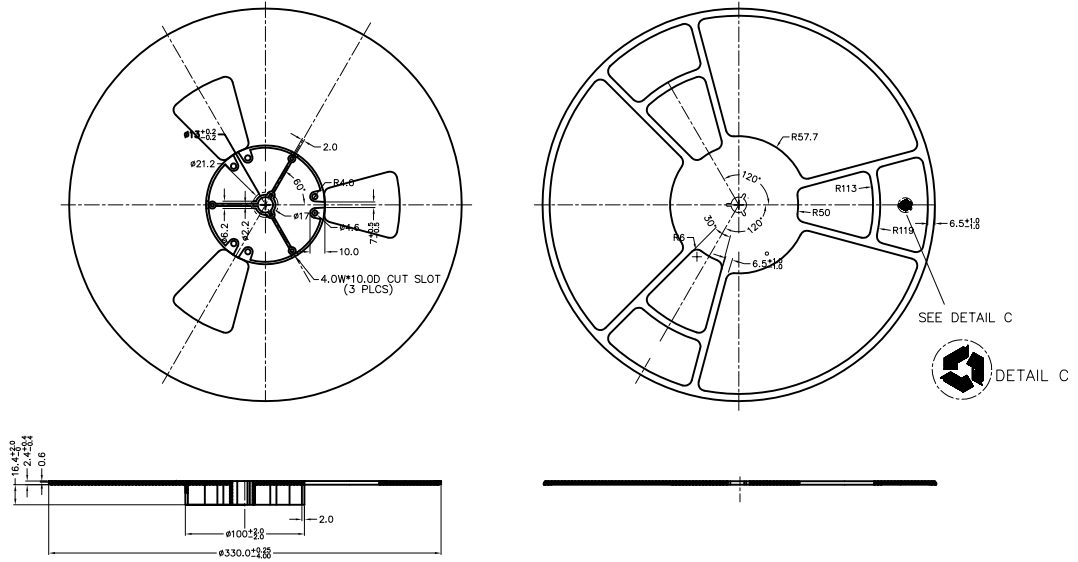


Figure 24. PowerFLAT 8x8 HV reel



8229819\_Reel\_revA

Note: All dimensions are in millimeters.

## Revision history

**Table 8. Document revision history**

Date	Revision	Changes
26-Jun-2013	1	First release.
23-Jul-2014	2	<p>Updated the title, the features and the description in cover page. Document status promoted from preliminary data to production data.</p> <p>Updated Figure 1: "Internal schematic diagram", Section 1: "Electrical ratings", Section 2: "Electrical characteristics".</p> <p>Added Section 2.1: "Electrical characteristics (curves)"</p> <p>Updated Section 3: "Test circuits", Section 4.1: "PowerFLAT™ 8x8 HV package mechanical data"..</p>
20-Nov-2015	3	<p>Updated: cover image and <i>Figure 1: "Internal schematic diagram"</i></p> <p>Table 2: "Absolute maximum ratings", Table 3: "Thermal data" and <i>Table 6: "Switching times"</i></p> <p>Updated: <i>Figure 3: "Thermal impedance"</i></p> <p>Updated: <i>Section 5: "Test circuits"</i></p> <p>Updated: Section 6.1: "PowerFLAT™ 8x8 HV package mechanical data"</p> <p>Minor text changes</p>
11-Jun-2019	4	<p>Update <a href="#">Section 1 Electrical ratings</a>.</p> <p>Added <a href="#">Figure 13. Maximum avalanche energy vs temperature</a>.</p> <p>Minor text changes.</p>

---

## Contents

<b>1</b>	<b>Electrical ratings</b> .....	<b>2</b>
<b>2</b>	<b>Electrical characteristics</b> .....	<b>3</b>
<b>2.1</b>	Electrical characteristics (curves) .....	<b>5</b>
<b>3</b>	<b>Test circuits</b> .....	<b>8</b>
<b>4</b>	<b>Package mechanical data</b> .....	<b>9</b>
<b>4.1</b>	PowerFLAT 8x8 HV package information .....	<b>9</b>
<b>4.2</b>	PowerFLAT 8x8 HV packing information .....	<b>10</b>
	<b>Revision history</b> .....	<b>13</b>

**IMPORTANT NOTICE – PLEASE READ CAREFULLY**

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, please refer to [www.st.com/trademarks](http://www.st.com/trademarks). All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2019 STMicroelectronics – All rights reserved