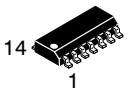
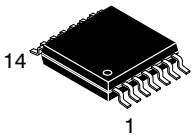
Quad 2-Input NOR Gate

MM74HC02



SOIC−14 NB,
CASE 751A−0.3



TSSOP−14,
CASE 948G−01

General Description

The MM74HC02 NOR gates utilize advanced silicon−gate CMOS technology to achieve operating speeds similar to LS−TTL gates with the low power consumption of standard CMOS integrated circuits. All gates have buffered outputs, providing high noise immunity and the ability to drive 10 LS−TTL loads. The 74HC logic family is functionally as well as pin−out compatible with the standard 74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical Propagation Delay: 8 ns
- Wide Power Supply Range: 2 V to 6 V
- Low Quiescent Supply Current: 20 μA Maximum (74HC Series)
- Moisture Level Sensitivity 1
- Low Input Current: 1 μA Maximum
- High Output Current: 4 mA Minimum
- This Device is Pb−Free and Halide Free

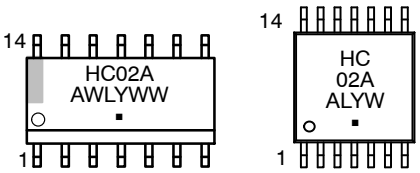
ABSOLUTE MAXIMUM RATINGS (Note 1)

Symbol	Parameter	Rating	Unit
V_{CC}	Supply Voltage	−0.5 to +7.0	V
V_{IN}	DC Input Voltage	−0.5 to V_{CC} +0.5	V
V_{OUT}	DC Output Voltage	−0.5 to V_{CC} +0.5	V
I_{IK}, I_{OK}	Clamp Diode Current	±20	mA
I_{OUT}	DC Output Current, per pin	±25	mA
I_{CC}	DC V_{CC} or GND Current, per pin	±50	mA
T_{STG}	Storage Temperature Range	−65 to +150	°C
P_D	Power Dissipation (Note 2)	600	mW
	S.O. Package only	500	
T_L	Lead Temperature (Soldering 10 seconds)	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Unless otherwise specified all voltages are referenced to ground.
2. Power dissipation temperature derating − plastic “N” package: −12 mW/°C from 65°C to 85°C.

MARKING DIAGRAM

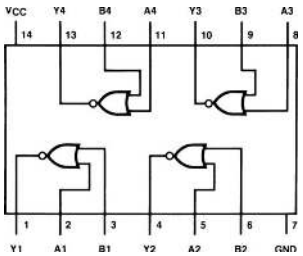


HC02A	= Specific Device Code
A	= Assembly Location
WL, L	= Wafer Lot Number
Y	= Year
WW, YW	= Work Week
▪	= Pb−Free Package

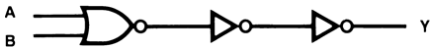
(Note: Microdot may be in either location)

CONNECTION DIAGRAM

Pin Assignment for SOIC and TSSOP



LOGIC DIAGRAM



ORDERING INFORMATION

See detailed ordering and shipping information on page 3 of this data sheet.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	Supply Voltage		2	6	V
V_{IN}, V_{OUT}	DC Input or Output Voltage		0	V_{CC}	V
T_A	Operating Temperature Range		−40	+85	°C
t_r, t_f	Input Rise or Fall Times	V_{CC} = 2.0 V	–	1000	ns
		V_{CC} = 4.5 V	–	500	
		V_{CC} = 6.0 V	–	400	

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC ELECTRICAL CHARACTERISTICS (Note 3)

Symbol	Parameter	V_{CC} (V)	Conditions	T_A = 25°C	T_A = −40°C to 85°C	T_A = −55°C to 125°C	Unit
				Typ.	Guaranteed Limits		
V_{IH}	Minimum HIGH Level Input Voltage	2.0		–	1.50	1.50	1.50	V
		4.5		–	3.15	3.15	3.15	
		6.0		–	4.20	4.20	4.20	
V_{IL}	Maximum LOW Level Input Voltage	2.0		–	0.50	0.50	0.50	V
		4.5		–	1.35	1.35	1.35	
		6.0		–	1.80	1.80	1.80	
V_{OH}	Minimum HIGH Level Output Voltage	2.0	V_{IN} = V_{IH} or V_{IL}, $\lvert I_{OUT} \rvert \le$ 20 μA	2.0	1.9	1.9	1.9	V
		4.5		4.5	4.4	4.4	4.4	
		6.0		6.0	5.9	5.9	5.9	
		4.5	V_{IN} = V_{IH} or V_{IL}, $\lvert I_{OUT} \rvert \le$ 4.0 mA	4.20	3.98	3.84	3.70	
		6.0	V_{IN} = V_{IH} or V_{IL}, $\lvert I_{OUT} \rvert \le$ 5.2 mA	5.70	5.48	5.34	5.20	
V_{OL}	Maximum LOW Level Output Voltage	2.0	V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT} \rvert \le$ 20 μA	0	0.1	0.1	0.1	V
		4.5		0	0.1	0.1	0.1	
		6.0		0	0.1	0.1	0.1	
		4.5	V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT} \rvert \le$ 4.0 mA	0.20	0.26	0.33	0.40	
		6.0	V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT} \rvert \le$ 5.2 mA	0.20	0.26	0.33	0.40	
I_{IN}	Maximum Input Current	6.0	V_{IN} = V_{CC} or GND	–	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	6.0	V_{IN} = V_{CC} or GND, I_{OUT} = 0 μA	–	2.0	20	40	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. For a power supply of 5 V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5 V. Thus the 4.5 V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5 V and 4.5 V respectively. (The V_{IH} value at 5.5 V is 3.85 V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0 V values should be used.

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5 V, T_A = 25°C, C_L = 15 pF, t_r = t_f = 6 ns)

Symbol	Parameter	Conditions	Typ.	Guaranteed Limit	Unit
t_{PHL}, t_{PLH}	Maximum Propagation Delay		8	15	ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 2.0 V to 6.0 V, C_L = 50 pF, $t_r = t_f$ = 6 ns, unless otherwise specified)

Symbol	Parameter	V_{CC} (V)	Conditions	T_A = 25°C	T_A = −40°C to 85°C	T_A = −55°C to 125°C		Unit
				Typ.	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay	2.0		45	90	113	134	ns
		4.5		9	18	23	27	
		6.0		8	15	19	23	
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time	2.0		30	75	95	110	ns
		4.5		8	15	19	22	
		6.0		7	13	16	19	
C_{PD}	Power Dissipation Capacitance (Note 4)		(per gate)	20	–	–	–	pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

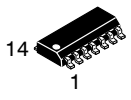
ORDERING INFORMATION

Device	Package	Shipping†
MM74HC02M	SOIC−14 NB (Pb−Free and Halide Free)	55 Units / Tube
MM74HC02MX		2500 / Tape & Reel
MM74HC02MTC	TSSOP−14 (Pb−Free and Halide Free)	96 Units / Tube
MM74HC02MTCX		2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NOTE: All packages are lead free per JEDEC: J−STD−020B standard.

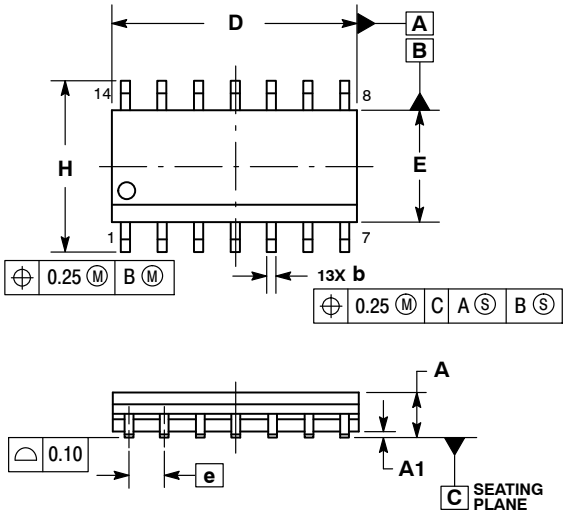
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

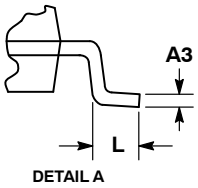


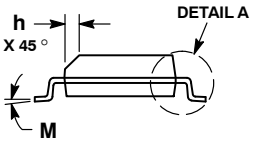
SCALE 1:1

SOIC−14 NB
CASE 751A−03
ISSUE L

DATE 03 FEB 2016



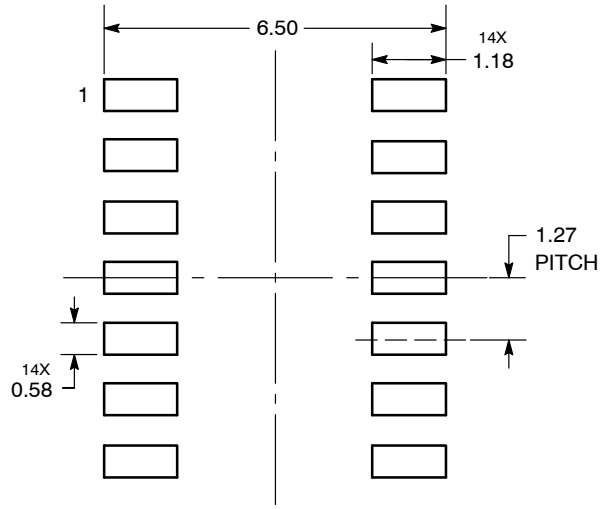




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0 °	7 °	0 °	7 °

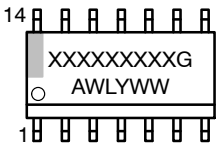
SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	**98ASB42565B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.	
DESCRIPTION:	**SOIC−14 NB**		**PAGE 1 OF 2**

SOIC−14
CASE 751A−03
ISSUE L

DATE 03 FEB 2016

STYLE 1:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. NO CONNECTION
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. NO CONNECTION
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 2:
CANCELLED

STYLE 3:
PIN 1. NO CONNECTION
2. ANODE
3. ANODE
4. NO CONNECTION
5. ANODE
6. NO CONNECTION
7. ANODE
8. ANODE
9. ANODE
10. NO CONNECTION
11. ANODE
12. ANODE
13. NO CONNECTION
14. COMMON CATHODE

STYLE 4:
PIN 1. NO CONNECTION
2. CATHODE
3. CATHODE
4. NO CONNECTION
5. CATHODE
6. NO CONNECTION
7. CATHODE
8. CATHODE
9. CATHODE
10. NO CONNECTION
11. CATHODE
12. CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 5:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. NO CONNECTION
7. COMMON ANODE
8. COMMON CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 6:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. ANODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE

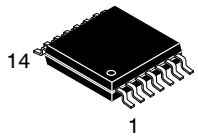
STYLE 7:
PIN 1. ANODE/CATHODE
2. COMMON ANODE
3. COMMON CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. ANODE/CATHODE
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. COMMON CATHODE
12. COMMON ANODE
13. ANODE/CATHODE
14. ANODE/CATHODE

STYLE 8:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. ANODE/CATHODE
7. COMMON ANODE
8. COMMON ANODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. NO CONNECTION
12. ANODE/CATHODE
13. ANODE/CATHODE
14. COMMON CATHODE

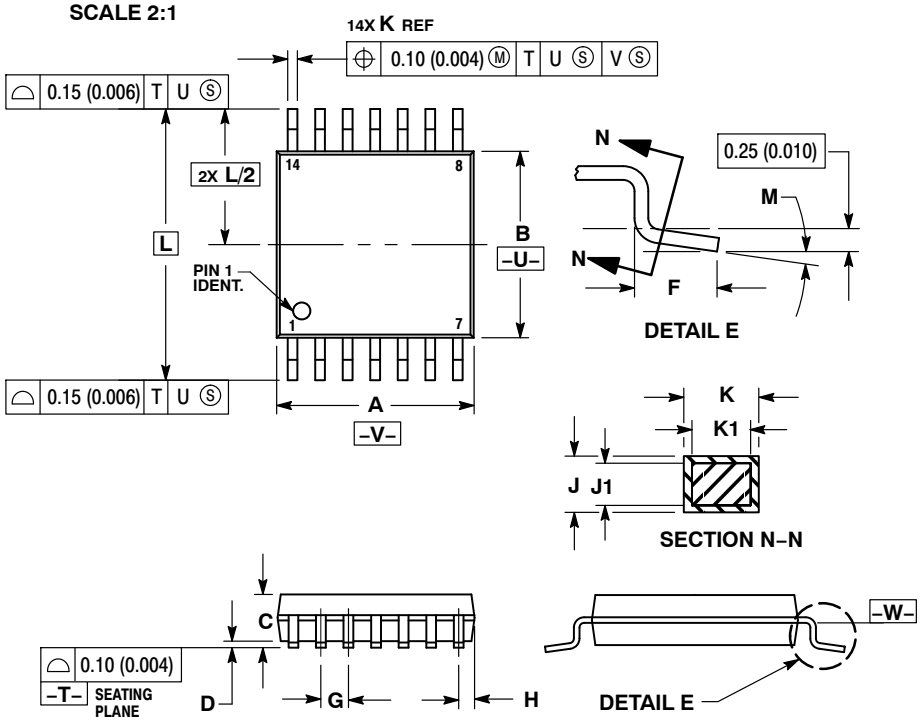
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

TSSOP−14 WB
CASE 948G
ISSUE C

DATE 17 FEB 2016



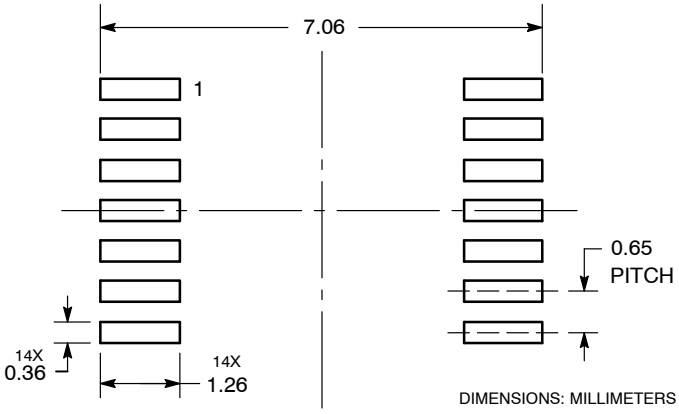
SCALE 2:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

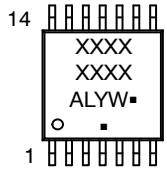
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	−−−	1.20	−−−	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

GENERIC MARKING DIAGRAM*



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	**98ASH70246A**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**TSSOP−14 WB**	**PAGE 1 OF 1**

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