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STK5C4U332J-E

Advance Information Intelligent Power Module (IPM) 600 V, 3 A

The STK5C4U332J-E is a fully-integrated inverter power stage consisting of a high-voltage driver, six IGBT's and a thermistor, suitable for driving permanent magnet synchronous (PMSM) motors, brushless-DC (BLDC) motors and AC asynchronous motors. The IGBT's are configured in a 3-phase bridge with separate emitter connections for the lower legs for maximum flexibility in the choice of control algorithm.

The power stage has a full range of protection functions including cross-conduction protection, external shutdown and under-voltage lockout functions. An internal comparator and reference connected to the over-current protection circuit allows the designer to set the over-current protection level.

Features

- Three-phase 3 A / 600 V IGBT module with integrated drivers
- Typical values : $V_{CE(sat)} = 1.3 \text{ V}$, $V_F = 1.3 \text{ V}$, $E_{sw} = 115 \mu\text{J}$ at 1.5 A
- Compact 29.6 mm × 18.2 mm dual in-line package
- Cross-conduction protection
- Adjustable over-current protection level
- Integrated bootstrap diodes and resistors
- Enable pin

Certification

- UL1557 (File number : E339285)

Typical Applications

- Industrial Pumps
- Industrial Fans
- Industrial Automation
- Home Appliances

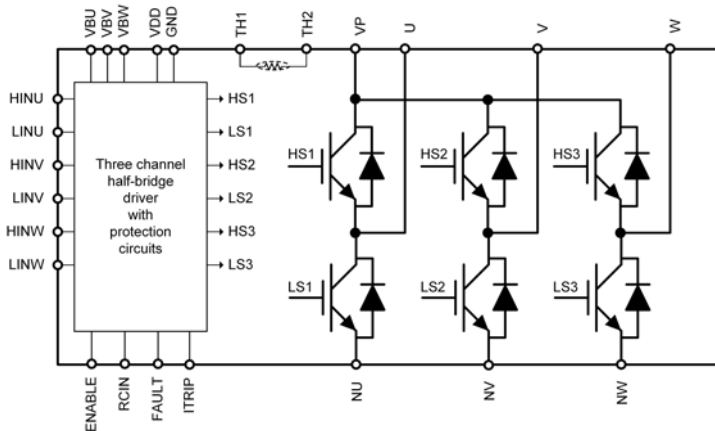


Figure 1. Functional Diagram

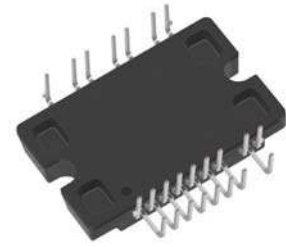
This document contains information on a new product. Specifications and information herein are subject to change without notice.



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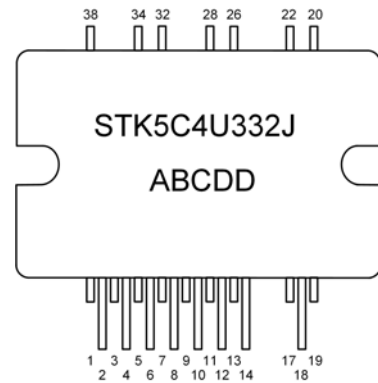
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PACKAGE PICTURE



MODULE 29.6x18.2 DIP S

MARKING DIAGRAM



STK5C4U332J = Specific Device Code
A = Year
B = Month
C = Production Site
DD = Factory Lot Code
Device marking is on package underside

ORDERING INFORMATION

| Device | Package | Shipping (Qty / Packing) |
|---------------|--|--------------------------|
| STK5C4U332J-E | MODULE 29.6x18.2 DIP S (Pb-Free) | 16 / Tube |

STK5C4U332J-E

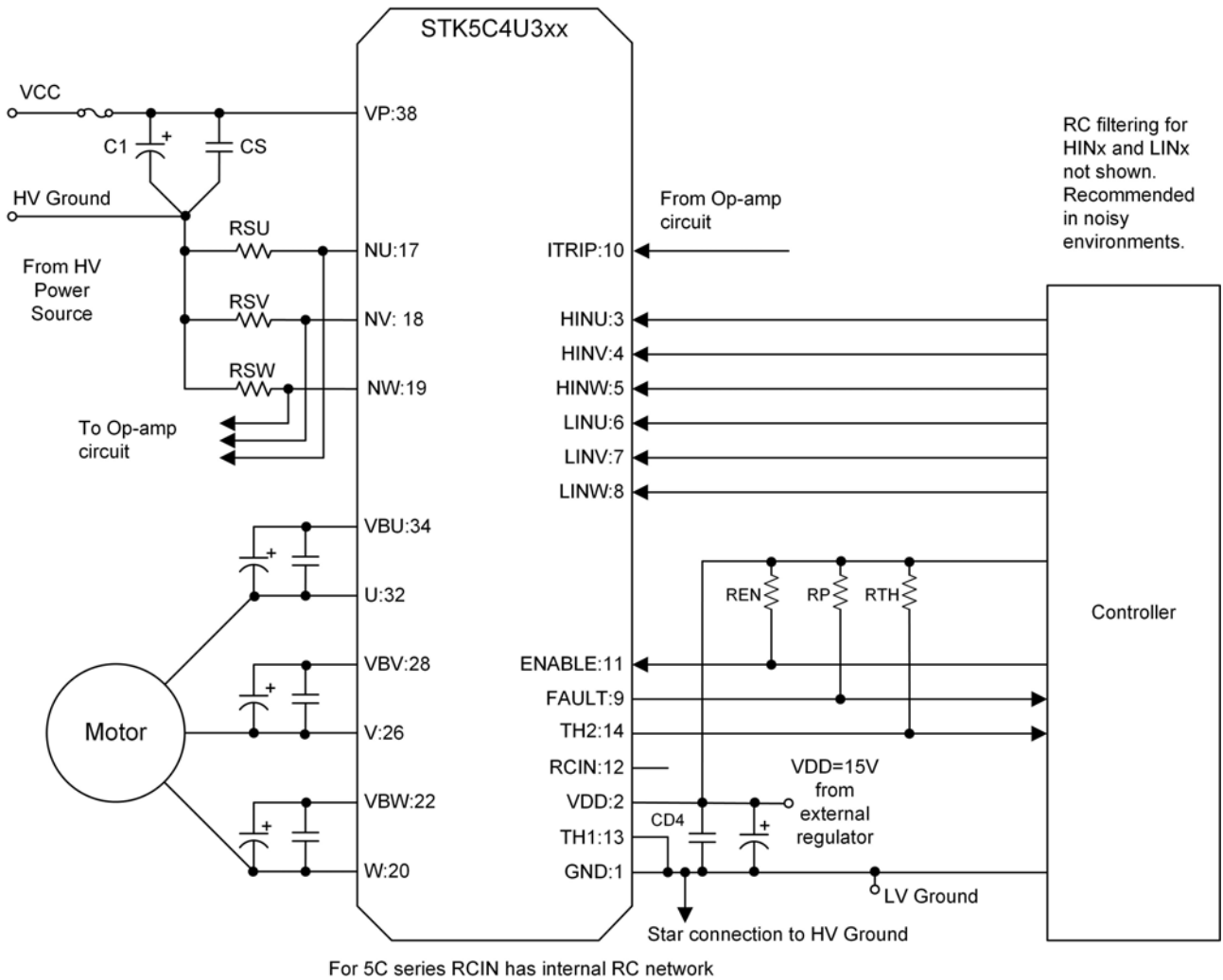


Figure 2. Application Schematic

STK5C4U332J-E

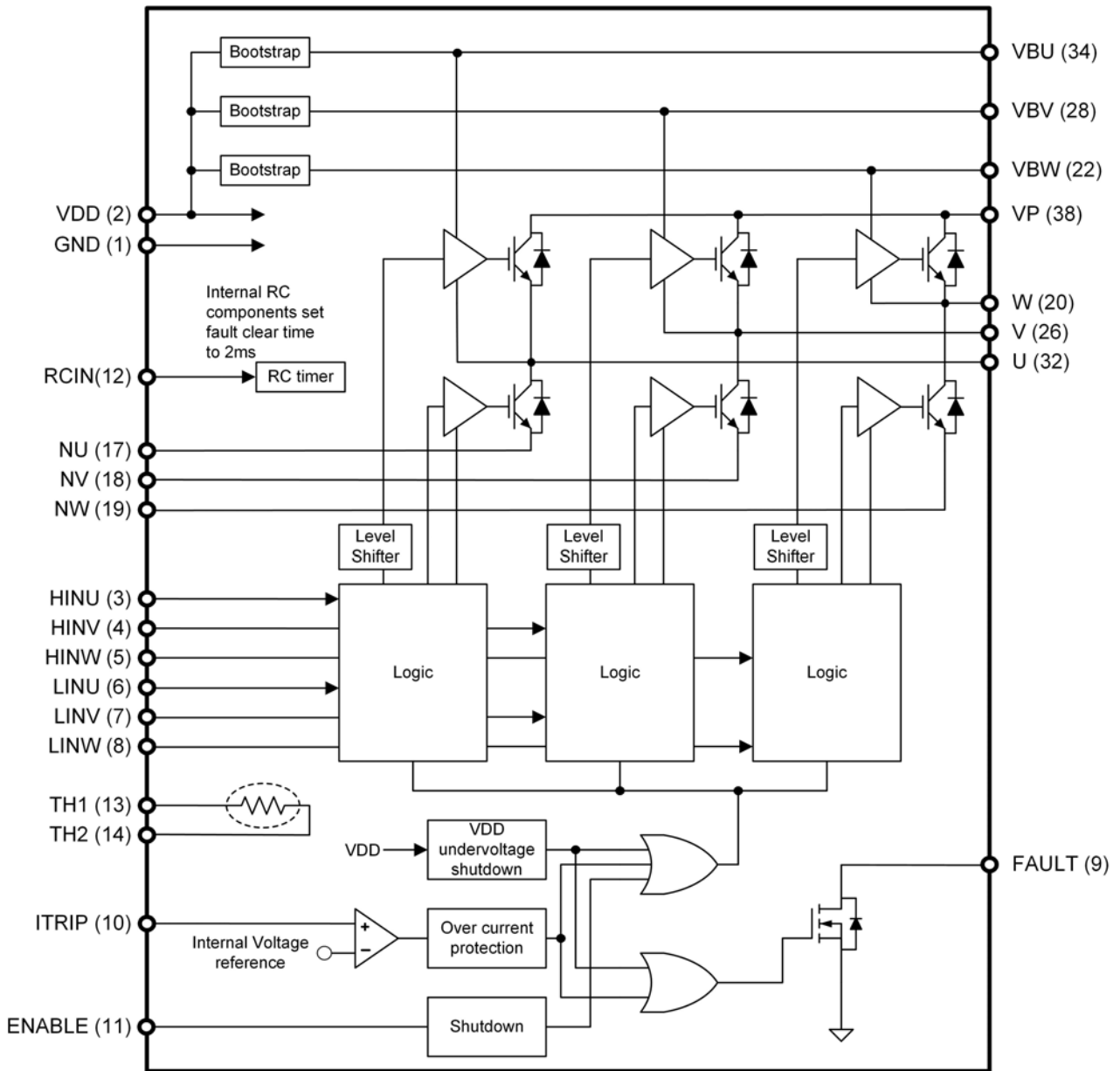


Figure 3. Simplified Block Diagram

STK5C4U332J-E

PIN FUNCTION DESCRIPTION

| Pin | Name | Description |
|-----|--------|---|
| 1 | GND | Negative Main Supply |
| 2 | VDD | +15 V Main Supply |
| 3 | HINU | Logic Input High Side Gate Driver - Phase U |
| 4 | HINV | Logic Input High Side Gate Driver - Phase V |
| 5 | HINW | Logic Input High Side Gate Driver - Phase W |
| 6 | LINU | Logic Input Low Side Gate Driver - Phase U |
| 7 | LINV | Logic Input Low Side Gate Driver - Phase V |
| 8 | LINW | Logic Input Low Side Gate Driver - Phase W |
| 9 | FAULT | Fault output |
| 10 | ITRIP | Current protection pin |
| 11 | ENABLE | Enable input |
| 12 | RCIN | R,C connection terminal for setting FAULT clear time |
| 13 | TH1 | Thermistor output 1 |
| 14 | TH2 | Thermistor output 2 |
| 17 | NU | Low Side Emitter Connection - Phase U |
| 18 | NV | Low Side Emitter Connection - Phase V |
| 19 | NW | Low Side Emitter Connection - Phase W |
| 20 | W | W phase output. Internally connected to W phase high side driver ground |
| 22 | VBW | High Side Floating Supply Voltage for W phase |
| 26 | V | V phase output. Internally connected to V phase high side driver ground |
| 28 | VBV | High Side Floating Supply voltage for V phase |
| 32 | U | U phase output. Internally connected to U phase high side driver ground |
| 34 | VBV | High Side Floating Supply voltage for U phase |
| 38 | VP | Positive Bus Input Voltage |

Note : Pins 15, 16, 21, 23, 24, 25, 27, 29, 30, 31, 33, 35, 36, 37 are not present

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ABSOLUTE MAXIMUM RATINGS (Notes 1, 2)

| Rating | Symbol | Conditions | Value | Unit |
|-----------------------------|---------------------|---|-------------------------|------------------|
| Supply voltage | V _{CC} | VP to NU,NV,NW, surge < 500 V (Note 3) | 450 | V |
| Collector-emitter voltage | V _{CE max} | VP to U,V,W; U to NU; V to NV; W to NW | 600 | V |
| Output current | I _o | VP,U,V,W,NU,NV,NW terminal current | ±3 | A |
| | | VP,U,V,W,NU,NV,NW terminal current, T _c = 100°C | ±1.5 | A |
| Output peak current | I _{op} | VP,U,V,W,NU,NV,NW terminal current, pulse width 1ms | ±6 | A |
| Gate driver supply voltages | V _{BS} | VBU to U, VBV to V, VBW to W, V _{DD} to GND (Note 4) | -0.3 to +20.0 | V |
| Input signal voltage | V _{IN} | HINU, HINV, HINW, LINU, LINV, LINW | -0.3 to V _{DD} | V |
| FAULT terminal voltage | V _{FAULT} | FAULT terminal | -0.3 to V _{DD} | V |
| RCIN terminal voltage | V _{RCIN} | RCIN terminal | -0.3 to V _{DD} | V |
| ITRIP terminal voltage | V _{ITRIP} | ITRIP terminal | -0.3 to +10.0 | V |
| ENABLE terminal voltage | V _{ENABLE} | ENABLE terminal | -0.3 to V _{DD} | V |
| Maximum power dissipation | P _d | IGBT per 1 channel | 11.3 | W |
| Junction temperature | T _j | IGBT, Gate driver IC | 150 | °C |
| Storage temperature | T _{stg} | | -40 to +125 | °C |
| Operating case temperature | T _c | IPM case temperature | -20 to +100 | °C |
| Package mounting torque | | Case mounting screw | 0.6 | Nm |
| Isolation voltage | V _{is} | 50 Hz sine wave AC 1 minute (Note 5) | 2000 | V _{rms} |

1. Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
2. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters.
3. This surge voltage developed by the switching operation due to the wiring inductance between VP and NU,NV,NW terminals.
4. V_{BS} = VBU to U, VBV to V, VBW to W.
5. Test conditions : AC 2500 V, 1 s.

RECOMMENDED OPERATING RANGES (Note 6)

| Rating | Symbol | | Min | Typ | Max | Unit |
|-----------------------------|----------------------|------------------------------------|------|-----|-----------------|------|
| Supply voltage | V _{CC} | VP to NU,NV,NW | 0 | 280 | 450 | V |
| Gate driver supply voltage | V _{BS} | VBU to U, VBV to V, VBW to W | 12.5 | 15 | 17.5 | V |
| | V _{DD} | V _{DD} to GND (Note 4) | 13.5 | 15 | 16.5 | V |
| ON-state input voltage | V _{IN(ON)} | HINU, HINV, HINW, LINU, LINV, LINW | 2.5 | | V _{DD} | V |
| OFF-state input voltage | V _{IN(OFF)} | | 0 | | 0.8 | |
| PWM frequency | f _{PWM} | | 1 | | 20 | kHz |
| Dead time | DT | Turn-off to turn-on (external) | 1.3 | | | µs |
| Allowable input pulse width | P _{WIN} | ON and OFF | 1 | | | µs |
| Package mounting torque | | 'M3' type screw | 0.4 | | 0.6 | Nm |

6. Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

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ELECTRICAL CHARACTERISTICS at T_c = 25°C (Note 7)

| Parameter | Test Conditions | Symbol | Min | Typ | Max | Unit |
|---|---|--|-------------|------|------|------|
| Power output section | | | | | | |
| Collector-emitter leakage current | V _{CE} = 600 V | I _{CE} | | | 100 | μA |
| Bootstrap diode reverse current | V _{R(BD)} = 600 V | I _{R(BD)} | | | 100 | μA |
| Collector to emitter saturation voltage | I _c = 3 A, T _j = 25°C | V _{CE(sat)} | | 1.6 | 2.4 | V |
| | I _c = 1.5 A, T _j = 100°C | | | 1.3 | – | V |
| Diode forward voltage | I _F = 3 A, T _j = 25°C | V _F | | 1.5 | 2.3 | V |
| | I _F = 1.5 A, T _j = 100°C | | | 1.3 | – | V |
| Junction to case thermal resistance | Reverse conducting IGBT | θ _{j-c(T)} | – | – | 11 | °C/W |
| Switching time | I _c = 3 A, V _{CC} = 300 V, T _j = 25°C | t _{ON} | – | 0.5 | 1.2 | μs |
| | | t _{OFF} | – | 0.6 | 1.4 | μs |
| Turn-on switching loss | I _c = 1.5 A, V _{CC} = 300 V, T _j = 25°C | E _{ON} | – | 100 | – | μJ |
| Turn-off switching loss | | E _{OFF} | – | 15 | – | μJ |
| Total switching loss | | E _{TOT} | – | 115 | – | μJ |
| Turn-on switching loss | I _c = 1.5 A, V _{CC} = 300 V, T _j = 100°C | E _{ON} | – | 120 | – | μJ |
| Turn-off switching loss | | E _{OFF} | – | 20 | – | μJ |
| Total switching loss | | E _{TOT} | – | 140 | – | μJ |
| Diode reverse recovery energy | I _c = 1.5 A, V _{CC} = 300 V, T _j = 100°C (di/dt set by internal driver) | E _{REC} | – | 35 | – | μJ |
| Diode reverse recovery time | | t _{rr} | – | 150 | – | ns |
| Reverse bias safe operating area | I _c = 6 A, V _{CE} = 450 V | RBSOA | Full Square | – | | |
| Short circuit safe operating area | V _{CE} = 400 V | SCSOA | 3 | – | – | μs |
| Allowable offset voltage slew rate | U to UN, V to VN, W to WN | dv/dt | –50 | – | 50 | V/ns |
| Driver Section | | | | | | |
| Gate driver consumption current | V _{BS} = 15 V (Note 4), per driver | I _D | – | 0.1 | 0.2 | mA |
| | V _{DD} = 15 V, total | I _D | – | 1.3 | 2.6 | mA |
| High level Input voltage | HINU, HINV, HINW, LINU, LINV, LINW to GND | V _{in H} | 2.5 | – | – | V |
| Low level Input voltage | | V _{in L} | – | – | 0.8 | V |
| Logic 1 input current | V _{IN} = +3.3 V | I _{IN+} | – | 100 | 143 | μA |
| Logic 0 input current | V _{IN} = 0 V | I _{IN-} | – | – | 2 | μA |
| Bootstrap ON Resistance | I _B = 1 mA | R _B | – | 110 | 300 | Ω |
| FAULT terminal sink current | FAULT : ON / VFAULT = 0.1 V | I _{oSD} | – | 2 | – | mA |
| FAULT clearance delay time | | FLTCLR | 1 | 2 | 3 | ms |
| ENABLE ON/OFF voltage | V _{EN} ON-state voltage | V _{EN +} | 2.5 | – | – | V |
| | V _{EN} OFF-state voltage | V _{EN –} | – | – | 0.8 | V |
| ITRIP threshold voltage | ITRIP to GND | V _{ITRIP} | 0.44 | 0.49 | 0.54 | V |
| ITRIP to shutdown propagation delay | | t _{ITRIP} | – | 550 | – | ns |
| ITRIP blanking time | | t _{ITRIPBL} | 100 | 350 | – | ns |
| V _{DD} and V _{BS} supply undervoltage positive going input threshold | | V _{DDUV+} V _{BSUV+} | 10.5 | 11.1 | 11.7 | V |
| V _{DD} and V _{BS} supply undervoltage negative going input threshold | | V _{DDUV-} V _{BSUV-} | 10.3 | 10.9 | 11.5 | V |
| V _{DD} and V _{BS} supply undervoltage I _{lockout} hysteresis | | V _{DDUVH} V _{BSUVH} | 0.14 | 0.2 | – | V |

7. Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

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TYPICAL CHARACTERISTICS

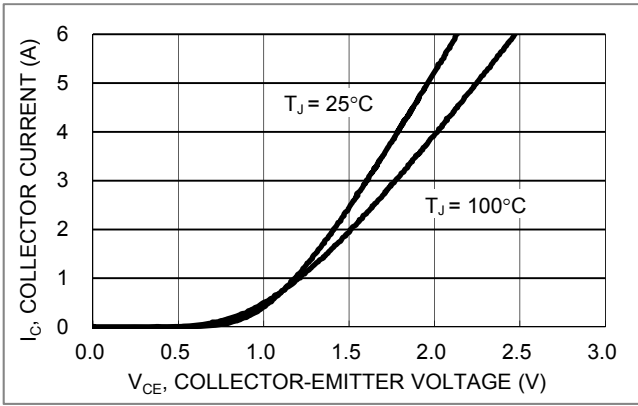


Figure 4. V_{CE} versus I_D for different temperatures ($V_{DD} = 15\text{ V}$)

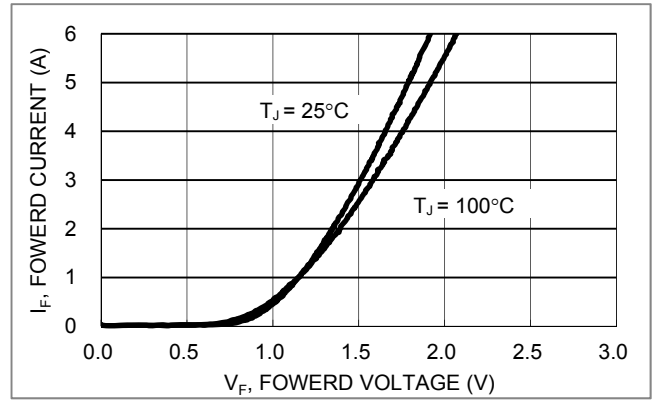


Figure 5. V_F versus I_D for different temperatures

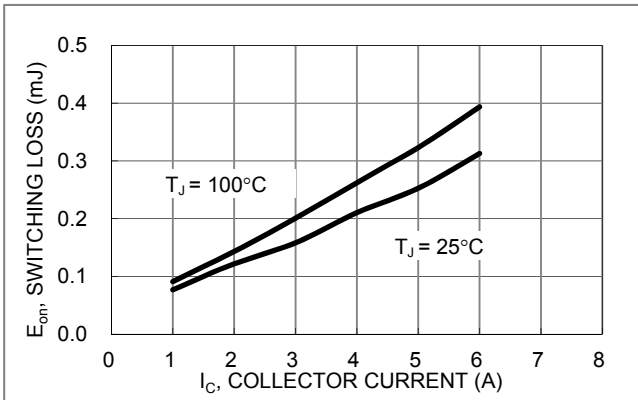


Figure 6. E_{ON} versus I_D for different temperatures

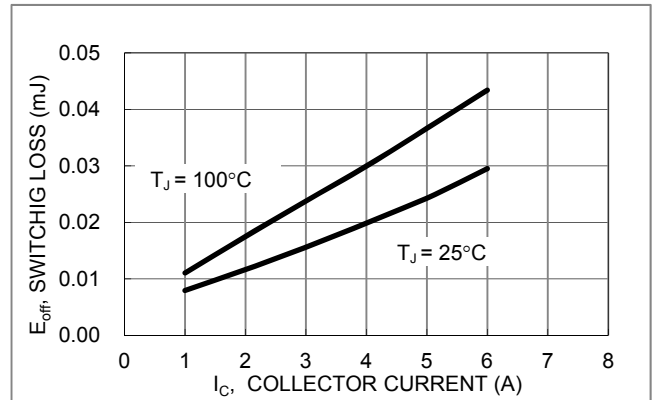


Figure 7. E_{OFF} versus I_D for different temperatures

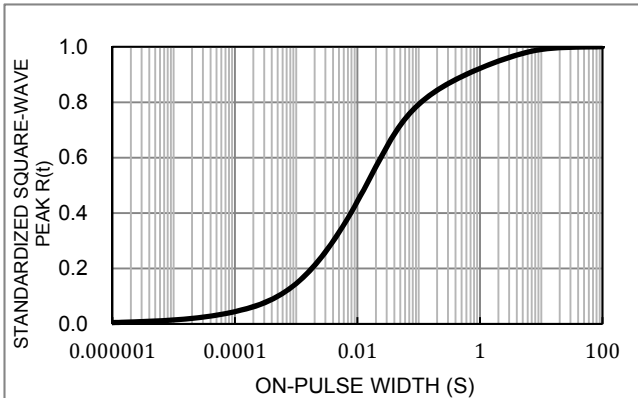


Figure 8. Thermal impedance plot

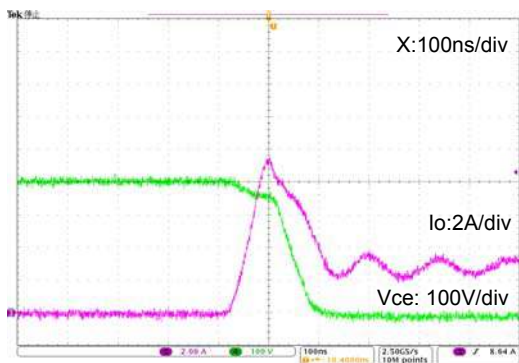


Figure 9. Turn-on waveform $T_J = 100^\circ\text{C}$, $V_{CC} = 400\text{ V}$

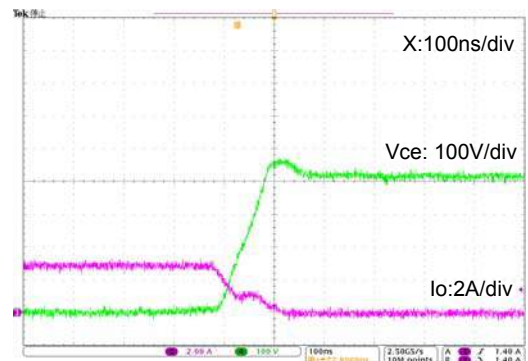


Figure 10. Turn-off waveform $T_J = 100^\circ\text{C}$, $V_{CC} = 400\text{ V}$

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APPLICATIONS INFORMATION

Input / Output Timing Chart

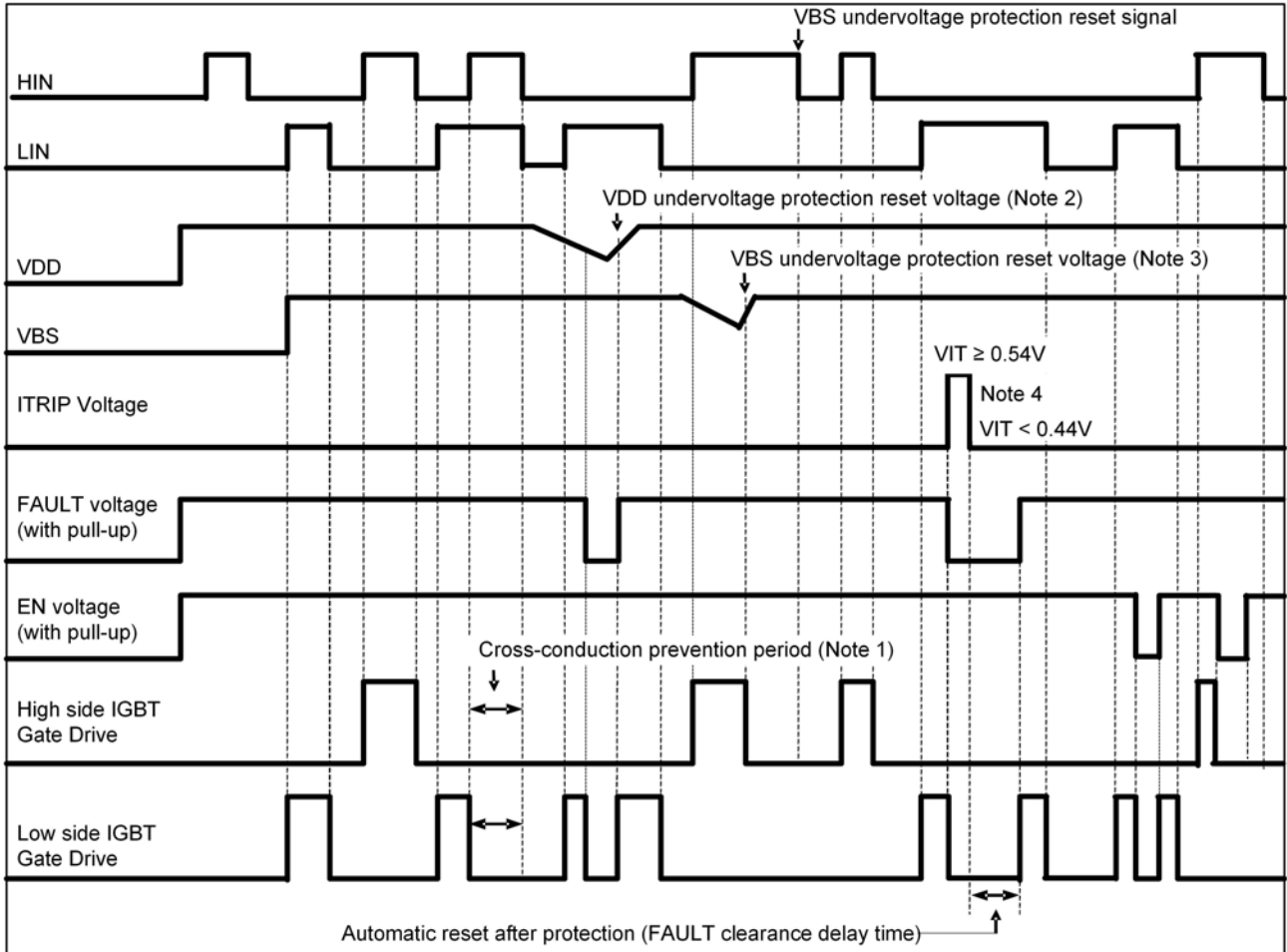


Figure 11. Input/Output Timing Chart

Notes

1. This section of the timing diagram shows the effect of cross-conduction prevention.
2. This section of the timing diagram shows that when the voltage on V_{DD} decreases sufficiently all gate output signals will go low, switching off all six IGBTs. When the voltage on V_{DD} rises sufficiently, normal operation will resume.
3. This section shows that when the bootstrap voltage V_{BS} drops, the corresponding high side output (U or V or W) is switched off. When V_{BS} rises sufficiently, normal operation will resume.
4. This section shows that when the voltage on ITRIP exceeds the threshold, all IGBT's are turned off. Normal operation resumes later after the over-current condition is removed.
5. After V_{DD} has risen above the threshold to enable normal operation, the driver waits to receive an input signal on the LIN input before enabling the driver for the HIN signal.

Input / Output Logic Table

| INPUT | | | | OUTPUT | | | |
|-------|-----|-------|--------|----------------|---------------|----------------|-------|
| HIN | LIN | Itrip | Enable | High side IGBT | Low side IGBT | U,V,W | FAULT |
| H | L | L | H | ON (Note 5) | OFF | VP | OFF |
| L | H | L | H | OFF | ON | NU,NV,NW | OFF |
| L | L | L | H | OFF | OFF | High Impedance | OFF |
| H | H | L | H | OFF | OFF | High Impedance | OFF |
| X | X | H | H | OFF | OFF | High Impedance | ON |
| X | X | X | L | OFF | OFF | High Impedance | OFF |

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Thermistor characteristics

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|-------------------------|------------------|------------------------|------|------|------|------|
| Resistance | R ₂₅ | T _c = 25°C | 99 | 100 | 101 | kΩ |
| | R ₁₀₀ | T _c = 100°C | 5.18 | 5.38 | 5.60 | kΩ |
| B-Constant (25 to 50°C) | B | | 4208 | 4250 | 4293 | K |
| Temperature Range | | | -40 | | +125 | °C |

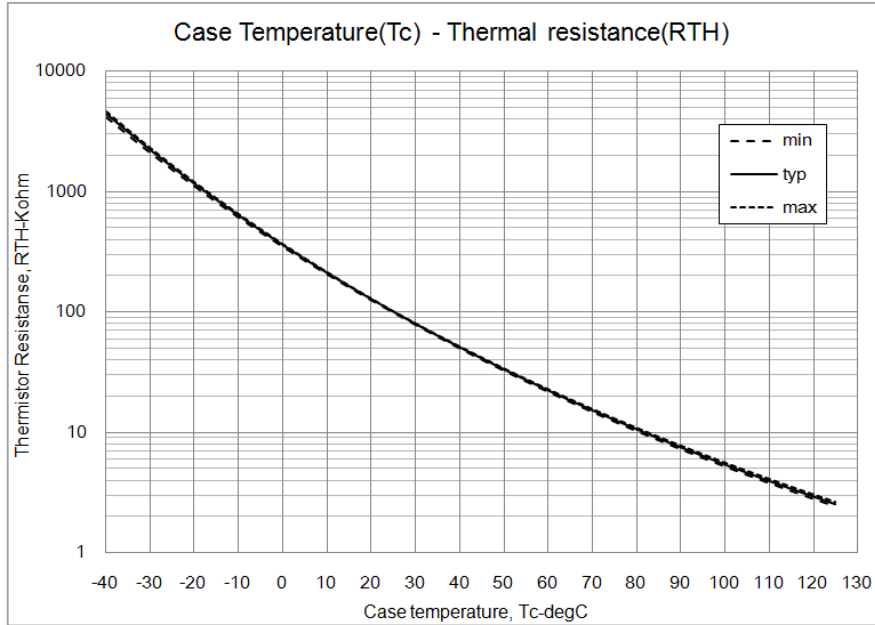


Figure 12. Thermistor Resistance versus Case Temperature

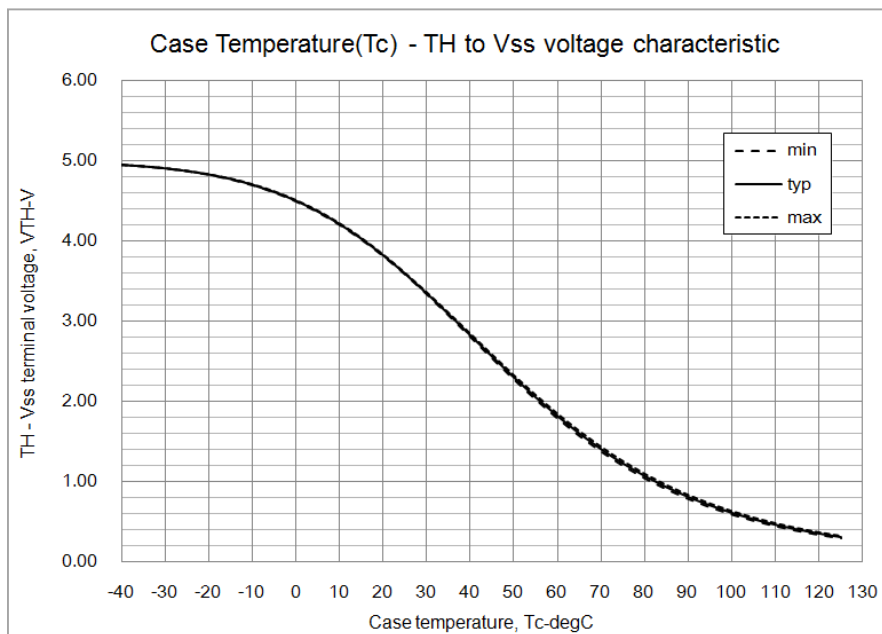


Figure 13. Thermistor Voltage versus Case Temperature
Conditions : RTH = 39 kΩ, pull-up voltage 5.0 V (see Figure 2)

Fault output

The FAULT output is an open drain output requiring a pull-up resistor. If the pull-up voltage is 5 V, use a pull-up resistor with a value of 6.8 kΩ or higher. If the pull-up voltage is 15 V, use a pull-up resistor with a value of 20 kΩ or higher. The FAULT output is triggered if there is a V_{DD} undervoltage or an overcurrent condition.

Undervoltage lockout protection

If V_{DD} goes below the V_{DD} supply undervoltage lockout falling threshold, the FAULT output is switched on. The FAULT output stays on until V_{DD} rises above the V_{DD} supply undervoltage lockout rising threshold. After V_{DD} has risen above the threshold to enable normal operation, the driver waits to receive an input signal on the LIN input before enabling the driver for the HIN signal.

Overcurrent protection

An over-current condition is detected if the voltage on the ITRIP pin is larger than the reference voltage. There is a blanking time of typically 350 ns to improve noise immunity. After a shutdown propagation delay of typically 0.55 μs, the FAULT output is switched on. The FAULT output is held on for a time determined by the resistor and capacitor connected to the RCIN pin. If RCIN pin is unconnected, the internal RC components set fault clear time to 2 ms (typical).

The over-current protection threshold should be set to be equal or lower to 2 times the module rated current (IO).

An additional fuse is recommended to protect against system level or abnormal over-current fault conditions.

Capacitors on High Voltage and V_{DD} supplies

Both the high voltage and V_{DD} supplies require an electrolytic capacitor and an additional high frequency capacitor.

Enable pin

The ENABLE terminal pin is used to enable or shut down the built-in driver. If the voltage on the ENABLE pin rises above the ENABLE ON-state voltage, the output drivers are enabled. If the voltage on the ENABLE pin falls below the ENABLE OFF-state voltage, the drivers are disabled.

Minimum input pulse width

When input pulse width is less than 1 μs, an output may not react to the pulse. (Both ON signal and OFF signal)

Calculation of bootstrap capacitor value

The bootstrap capacitor value CB is calculated using the following approach. The following parameters influence the choice of bootstrap capacitor:

- VBS : Bootstrap power supply.
15 V is recommended.
- QG : Total gate charge of IGBT at VBS = 15 V.
34 nC
- UVLO : Falling threshold for UVLO.
Specified as 12 V.
- ID_{MAX} : High side drive consumption current.
Specified as 0.4 mA
- t_{ONMAX} : Maximum ON pulse width of high side IGBT.

Capacitance calculation formula:

$$CB = (QG + ID_{MAX} * t_{ONMAX}) / (VBS - UVLO)$$

CB is recommended to be approximately 3 times the value calculated above. The recommended value of CB is in the range of 1 to 47 μF, however, the value needs to be verified prior to production. When not using the bootstrap circuit, each high side driver power supply requires an external independent power supply.

The internal bootstrap circuit uses a MOSFET. The turn on time of this MOSFET is synchronized with the turn on of the low side IGBT. The bootstrap capacitor is charged by turning on the low side IGBT.

If the low side IGBT is held on for a long period of time (more than one second for example), the bootstrap voltage on the high side MOSFET will slowly discharge.

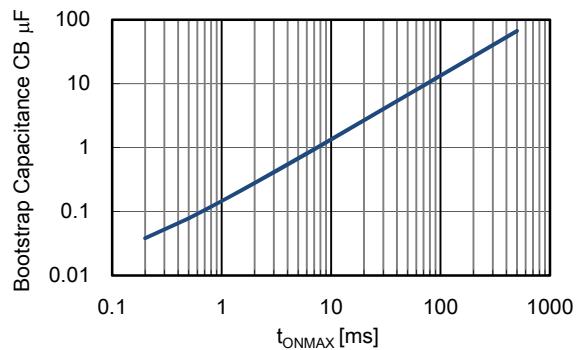


Figure 14. Bootstrap capacitance versus t_{ONMAX}

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Mounting Instructions

| Item | Recommended Condition |
|-----------|--|
| Pitch | 26.0 ±0.1 mm (Please refer to Package Outline Diagram) |
| Screw | Diameter : M3 Screw head types : pan head, truss head, binding head |
| Washer | Plane washer dimensions (Figure 14) D = 7 mm, d = 3.2 mm and t = 0.5 mm JIS B 1256 |
| Heat sink | Material: Aluminum or Copper Warpage (the surface that contacts IPM) : -50 to 50 μm Screw holes must be countersunk. No contamination on the heat sink surface that contacts IPM. |
| Torque | Temporary tightening : 50 to 60% of final tightening on first screw Temporary tightening : 50 to 60% of final tightening on second screw Final tightening : 0.4 to 0.6 Nm on first screw Final tightening : 0.4 to 0.6 Nm on second screw |
| Grease | Silicone grease. Thickness : 50 to 100 μm Uniformly apply silicone grease to whole back. Thermal foils are only recommended after careful evaluation. Thickness, stiffness and compressibility parameters have a strong influence on performance. |

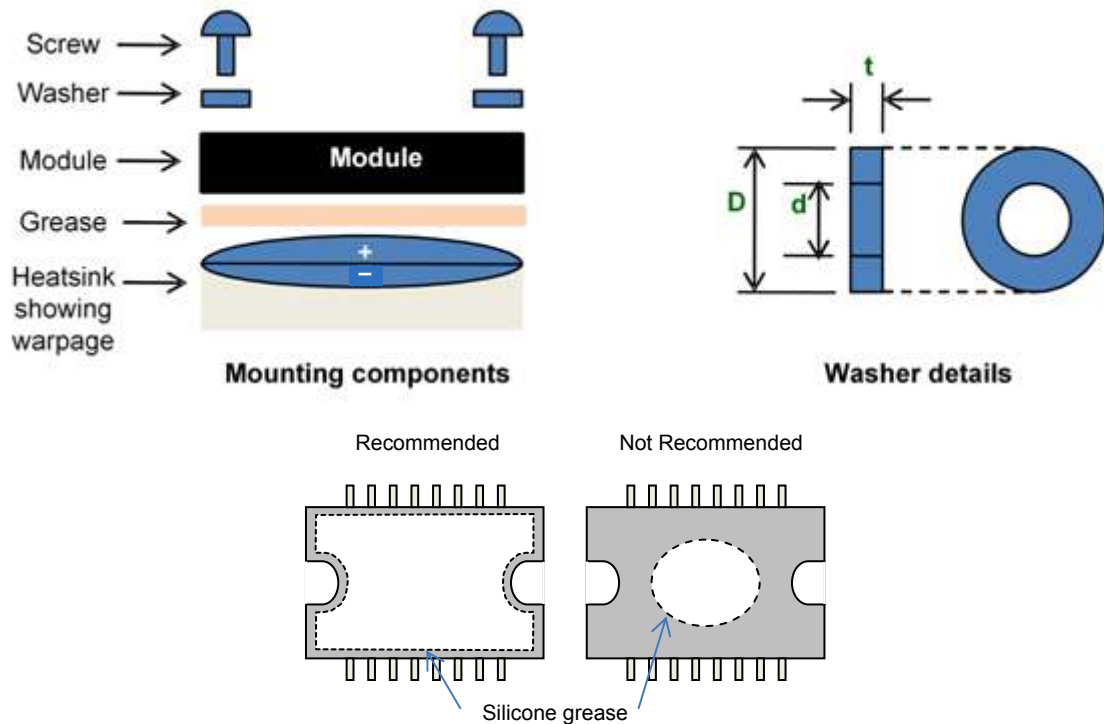


Figure 15. Module Mounting details : components ; washer drawing ; need for even spreading of thermal grease

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TEST CIRCUITS

■ ICE

| | U+ | V+ | W+ | U- | V- | W- |
|---|----|----|----|----|----|----|
| M | 38 | 38 | 38 | 32 | 26 | 20 |
| N | 32 | 26 | 20 | 17 | 18 | 19 |

U+,V+,W+ : High side phase
 U-,V-,W- : Low side phase

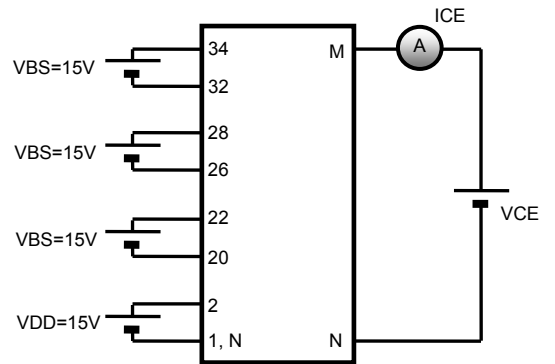


Figure 16. Test Circuit for ICE

■ VCE(sat) (Test by pulse)

| | U+ | V+ | W+ | U- | V- | W- |
|---|----|----|----|----|----|----|
| M | 38 | 38 | 38 | 32 | 26 | 20 |
| N | 32 | 26 | 20 | 17 | 18 | 19 |
| m | 3 | 4 | 5 | 6 | 7 | 8 |

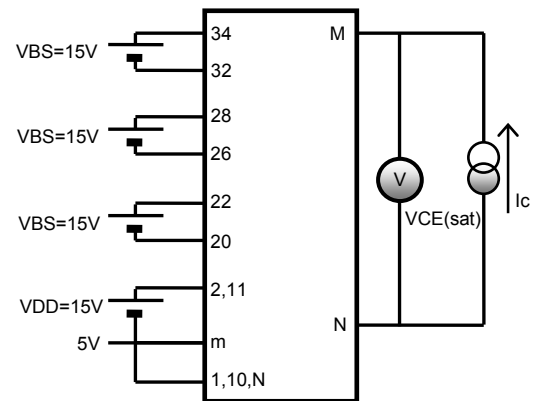


Figure 17. Test circuit for VCE(sat)

■ VF (Test by pulse)

| | U+ | V+ | W+ | U- | V- | W- |
|---|----|----|----|----|----|----|
| M | 38 | 38 | 38 | 32 | 26 | 20 |
| N | 32 | 26 | 20 | 17 | 18 | 19 |

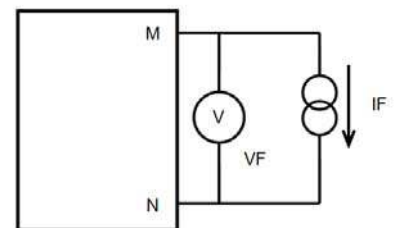


Figure 18. Test circuit for VF

STK5C4U332J-E

■ RB (Test by pulse)

| | U+ | V+ | W+ |
|---|----|----|----|
| M | 2 | 2 | 2 |
| N | 34 | 28 | 22 |

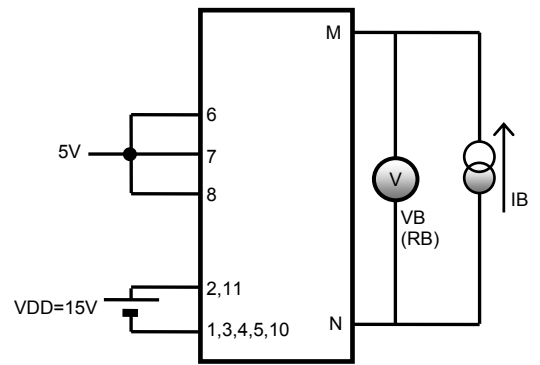


Figure 19. Test circuit for RB

■ ID

| | VBS U+ | VBS V+ | VBS W+ | VDD |
|---|--------|--------|--------|-----|
| M | 34 | 28 | 22 | 2 |
| N | 32 | 26 | 20 | 1 |

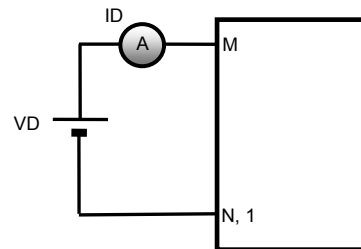


Figure 20. Test circuit for ID

■ Switching time (The circuit is a representative example of the low side U phase.)

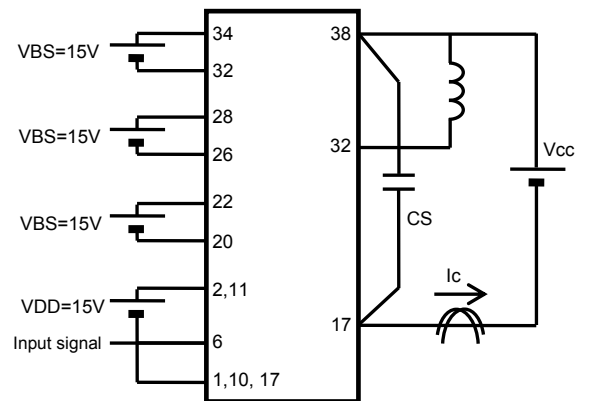
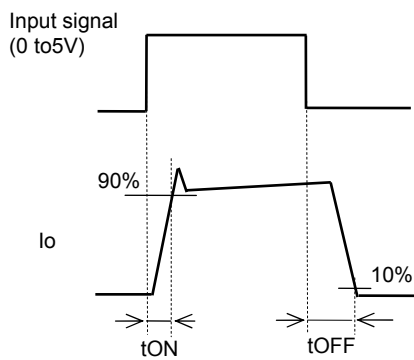


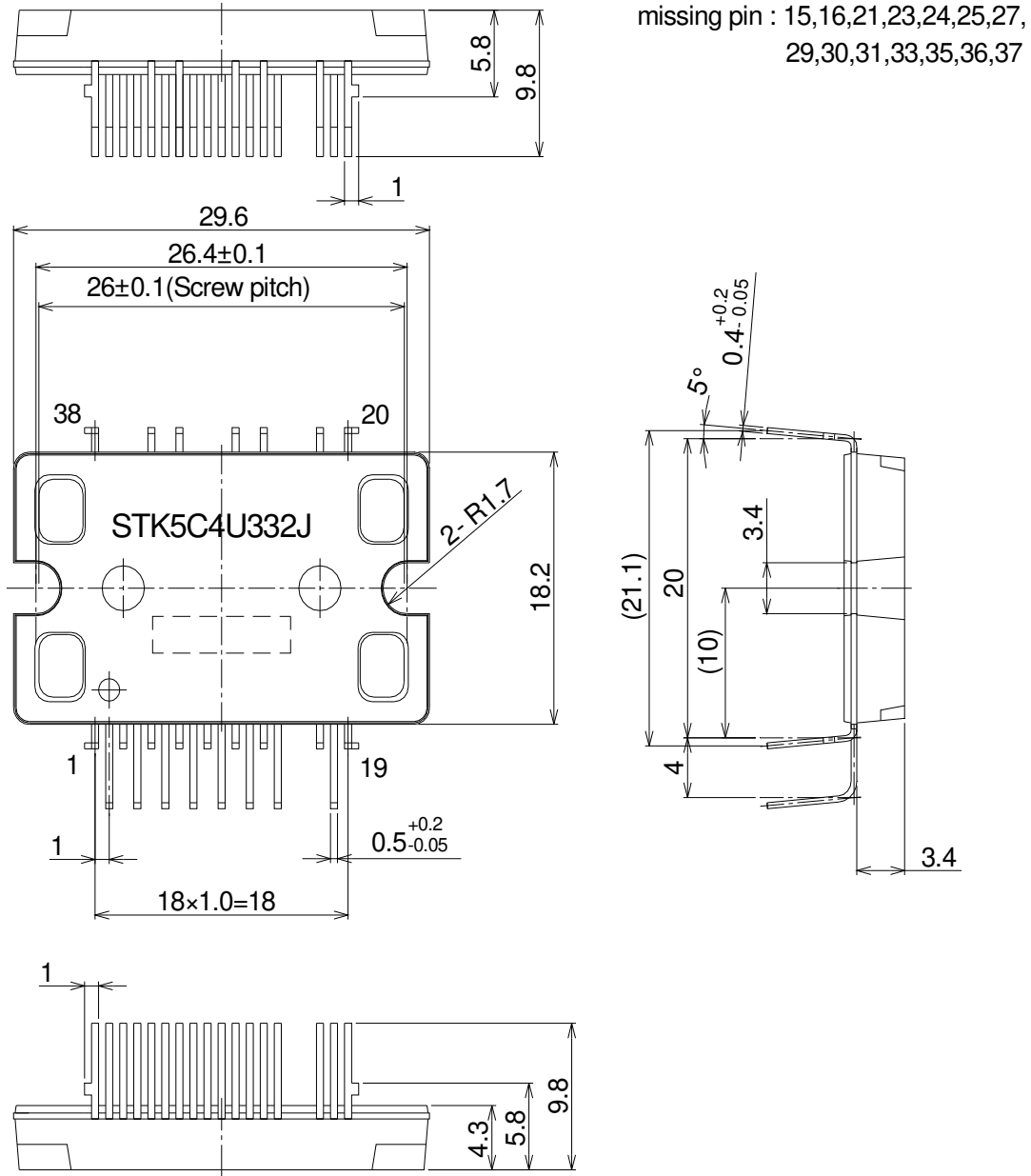
Figure 21. Switching time test circuit

STK5C4U332J-E

PACKAGE DIMENSIONS

unit : mm

The tolerances of length are +/- 0.5 mm unless otherwise specified.



missing pin : 15,16,21,23,24,25,27,
29,30,31,33,35,36,37

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