

## Features

- ESD protection for one line with uni-direction
- Provide transient protection for the protected line to
  - IEC 61000-4-2 (ESD)  $\pm 30\text{kV}$  (air/contact)**
  - IEC 61000-4-4 (EFT) 80A (5/50ns)**
  - IEC 61000-4-5 (Lightning) 6.5A (8/20 $\mu\text{s}$ )**
- Suitable for, **24V and below**, operating voltage applications
- **0402 small DFN package** saves board space
- Protect one I/O line or one power line
- Fast turn-on and low clamping voltage
- Solid-state silicon-avalanche and active circuit triggering technology
- **Green part**

## Applications

- USB Type-C CC and SBU protection
- USB VBUS protection
- Power supply protection
- Handheld portable applications
- Low speed data or control line protection
- Peripherals
- Consumer electronics

## Description

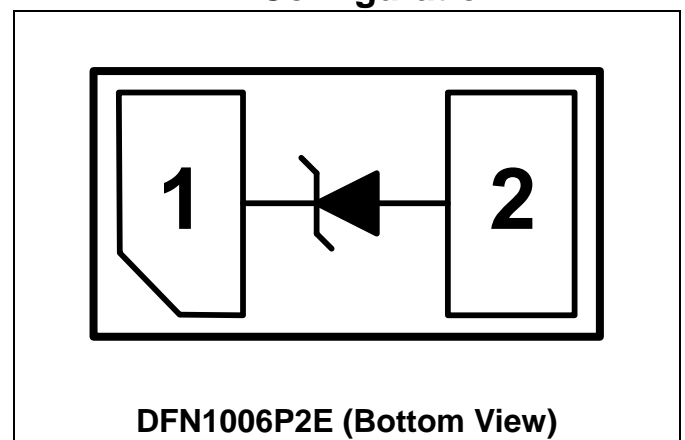
AZ4124-01F is a design which includes a uni-directional ESD rated clamping cell to protect one power line, one control line, or one low-speed data line in an electronic system. The AZ4124-01F has been specifically designed to protect sensitive components which are connected to power and control lines from over-voltage damage caused by Electrostatic Discharging (ESD), Electrical Fast Transients

(EFT), Lightning, and Cable Discharge Event (CDE).

AZ4124-01F is a unique design which includes proprietary clamping cell in a single package. During transient conditions, the proprietary clamping cell prevents over-voltage on the power line, control line, or data line, protecting any downstream components.

AZ4124-01F may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 ( $\pm 15\text{kV}$  air,  $\pm 8\text{kV}$  contact discharge).

## Circuit Diagram / Pin Configuration





## SPECIFICATIONS

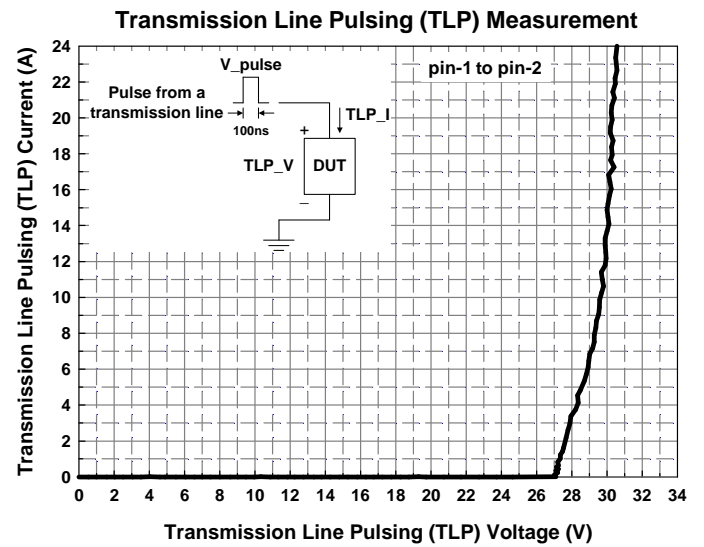
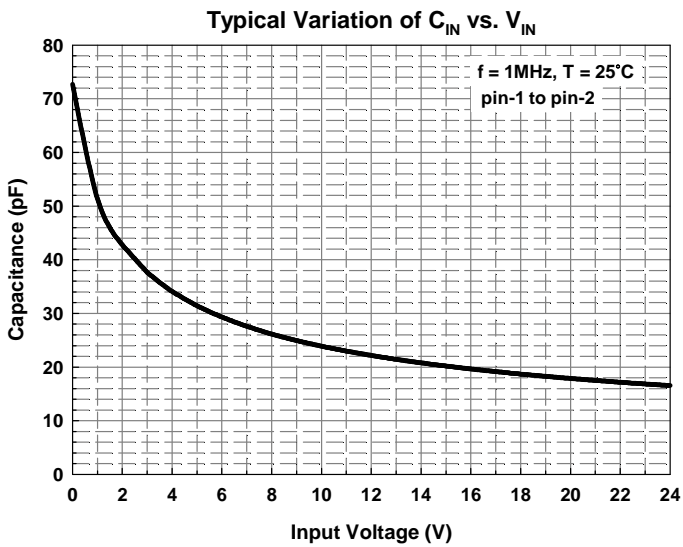
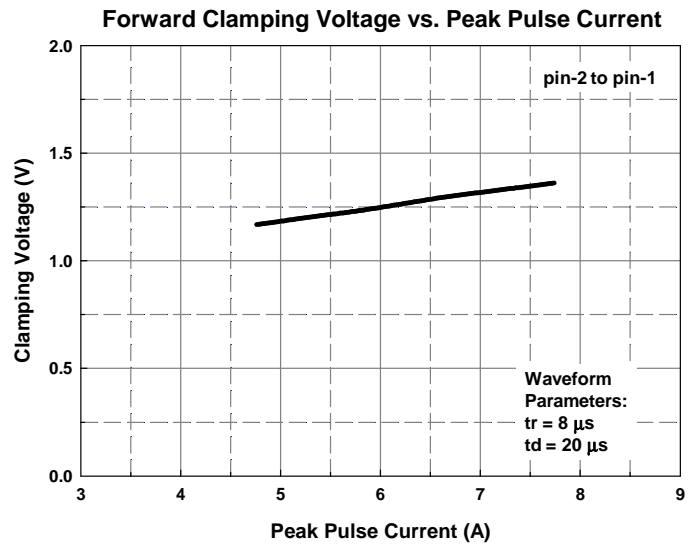
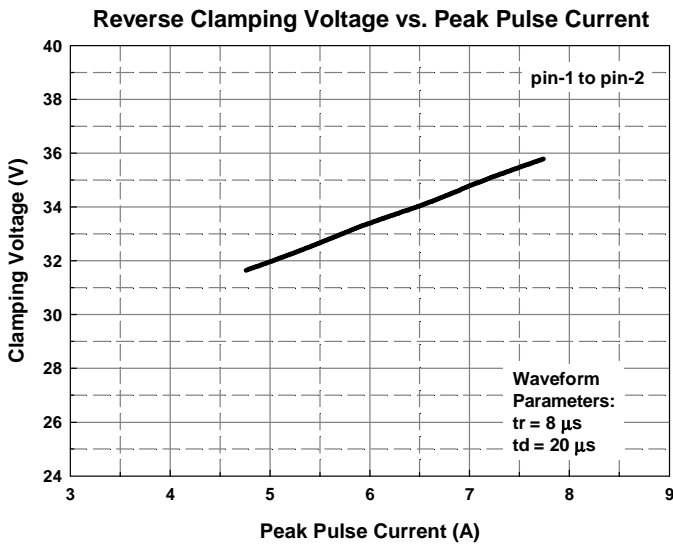
ABSOLUTE MAXIMUM RATINGS (T <sub>A</sub> = 25°C, unless otherwise specified)			
PARAMETER	SYMBOL	RATING	UNIT
Peak Pulse Current (tp=8/20μs)	I <sub>PP</sub>	6.5	A
Operating Voltage (pin-1 to pin-2)	V <sub>DC</sub>	25	V
ESD per IEC 61000-4-2 (Air)	V <sub>ESD-1</sub>	±30	kV
ESD per IEC 61000-4-2 (Contact)	V <sub>ESD-2</sub>	±30	kV
Lead Soldering Temperature	T <sub>SOL</sub>	260 (10 sec.)	°C
Operating Temperature	T <sub>OP</sub>	-55 to +125	°C
Storage Temperature	T <sub>STO</sub>	-55 to +150	°C

ELECTRICAL CHARACTERISTICS						
PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Reverse Stand-Off Voltage	V <sub>RWM</sub>	Pin-1 to pin-2, T = 25°C.			24	V
Reverse Leakage Current	I <sub>Leak</sub>	V <sub>RWM</sub> = 24V, T = 25°C, pin-1 to pin-2.			0.5	μA
Reverse Breakdown Voltage	V <sub>BV</sub>	I <sub>BV</sub> = 1mA, T = 25°C, pin-1 to pin-2.	25.5		31	V
Forward Voltage	V <sub>F</sub>	I <sub>F</sub> = 15mA, T = 25°C, pin-2 to pin-1.	0.6		1.2	V
Surge Clamping Voltage	V <sub>CL-surge</sub>	I <sub>PP</sub> = 5A, T = 25°C, pin-1 to pin-2.		32		V
ESD Clamping Voltage (Note 1)	V <sub>CL-ESD</sub>	IEC 61000-4-2 +8kV (I <sub>TLP</sub> = 16A), T = 25°C, contact mode, pin-1 to pin-2.		30		V
ESD Dynamic Turn-on Resistance	R <sub>dynamic</sub>	IEC 61000-4-2, 0~+8kV, contact mode, T = 25 °C, pin-1 to pin-2.		0.19		Ω
Channel Input Capacitance	C <sub>IN</sub>	V <sub>IN</sub> = 0V, f = 1MHz, pin-1 to pin-2, T = 25 °C.		72	85	pF

Note 1: ESD Clamping Voltage was measured by Transmission Line Pulsing (TLP) System.

TLP conditions: Z<sub>0</sub>= 50Ω, t<sub>p</sub>= 100ns, t<sub>r</sub>= 1ns.

## Typical Characteristics



## Application Information

The AZ4124-01F is designed to protect one line against system ESD / EFT / Lightning pulses by clamping it to an acceptable reference. It provides uni-directional protection.

The usage of the AZ4124-01F is shown in Fig. 1. Protected lines, such as data lines, control lines, or power lines, are connected to pin 1. The pin 2 should be connected to a ground plane on the board. In order to minimize parasitic inductance in the board traces, all path lengths connected to the pins of AZ4124-01F should be kept as short as possible.

In order to obtain enough suppression of ESD induced transient, a good circuit board is critical. Thus, the following guidelines are recommended:

- Minimize the path length between the protected lines and the AZ4124-01F.
- Place the AZ4124-01F near the input terminals or connectors to restrict transient coupling.
- The ESD current return path to ground should be kept as short as possible.
- Use ground planes whenever possible.
- NEVER route critical signals near board edges and near the lines which the ESD transient easily injects to.

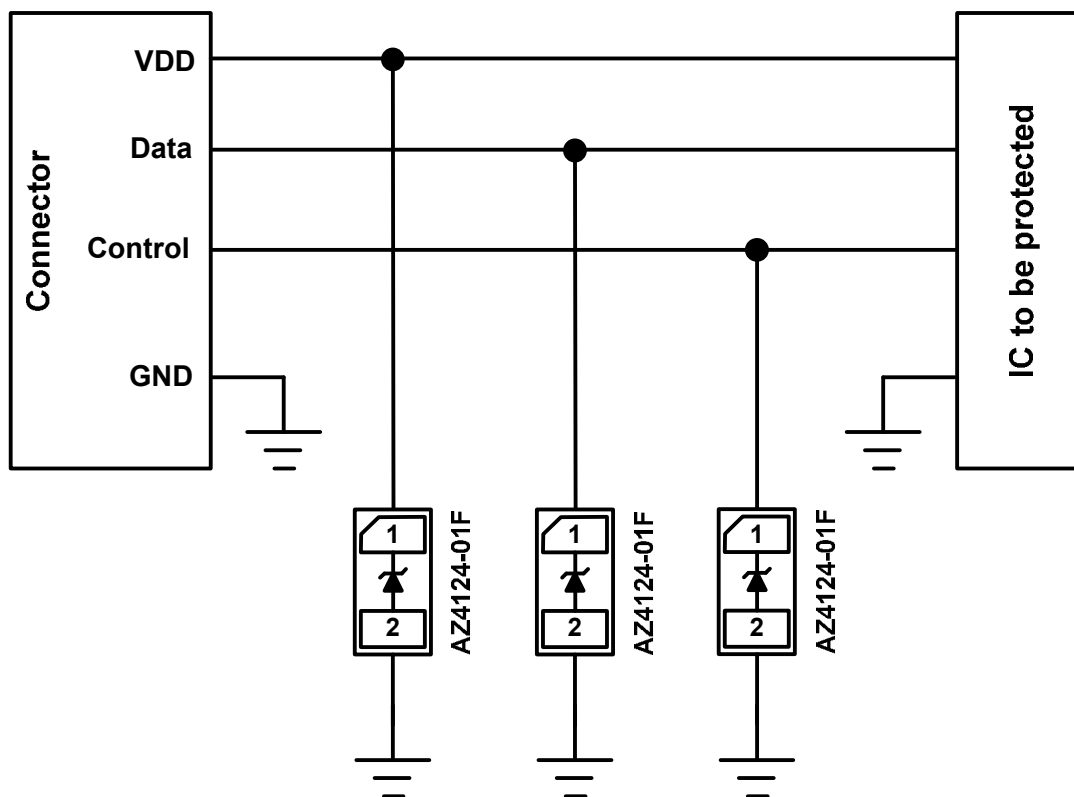
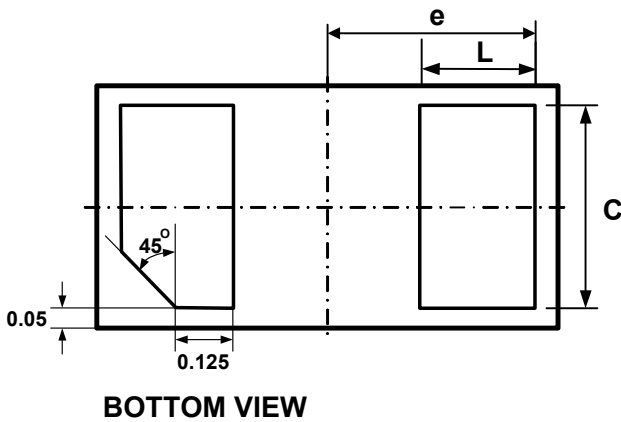
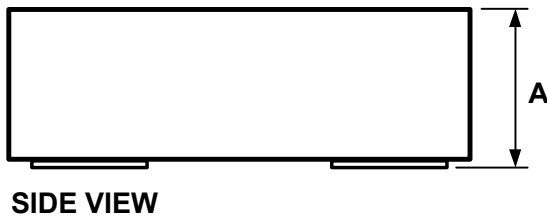
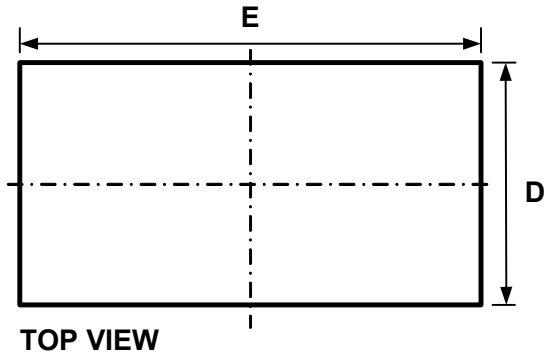


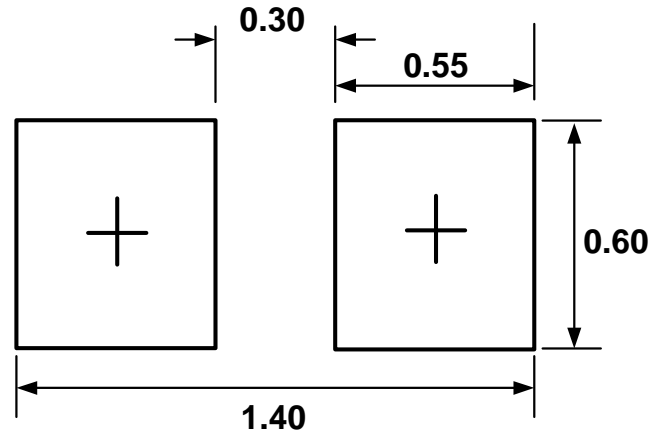
Fig. 1

## Mechanical Details

### DFN1006P2E PACKAGE DIAGRAMS



### LAND LAYOUT



(Unit: mm)

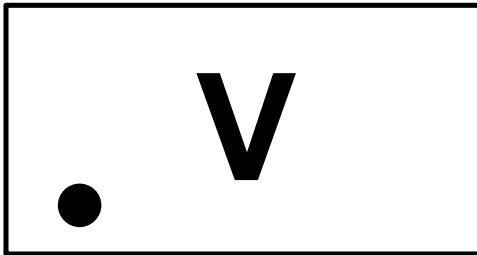
#### Notes:

This LAND LAYOUT is for reference purposes only. Please consult your manufacturing partners to ensure your company's PCB design guidelines are met.

### PACKAGE DIMENSIONS

SYMBOL	MILLIMETERS	
	MIN.	MAX.
E	0.95	1.05
D	0.55	0.65
A	0.45	0.55
e	0.45 BSC	
L	0.20	0.30
C	0.45	0.55

## MARKING CODE



Top View

Part Number	Marking Code
AZ4124-01F.R7GR (Green Part)	V

Note. Green means Pb-free, RoHS, and Halogen free compliant.

V = Device Code

## Ordering Information

PN#	Material	Type	Reel size	MOQ	MOQ/internal box	MOQ/carton
AZ4124-01F.R7GR	Green	T/R	7 inch	12,000/reel	4 reels = 48,000/box	6 boxes = 288,000/carton

## Revision History

Revision	Modification Description
Revision 2019/09/09	Formal Release.