

RF Power Field Effect Transistor

N-Channel Enhancement-Mode Lateral MOSFET

Designed for GSM and GSM EDGE base station applications with frequencies from 1800 to 2000 MHz. Suitable for FM, TDMA, CDMA and multicarrier amplifier applications. To be used in Class AB for GSM and GSM EDGE cellular radio applications.

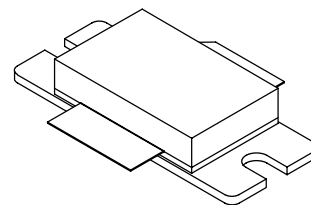
- GSM and GSM EDGE Performances @ 1805 MHz
Power Gain — 13.5 dB (Typ) @ 90 Watts CW
Efficiency — 52% (Typ) @ 90 Watts CW
- Capable of Handling 10:1 VSWR, @ 26 Vdc, 90 Watts CW Output Power

Features

- Internally Matched for Ease of Use
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Excellent Thermal Stability
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- RoHS Compliant
- In Tape and Reel. R3 Suffix = 250 Units per 56 mm, 13 inch Reel.

MRF18090AR3

**1805-1880 MHz, 90 W, 26 V
LATERAL N-CHANNEL
RF POWER MOSFET**



**CASE 465B-03, STYLE 1
NI-880**

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Table 1. Maximum Ratings

| Rating | Symbol | Value | Unit |
|----------------------------------------------------------------------------------------|-----------|--------------|--------------------------|
| Drain-Source Voltage | V_{DSS} | -0.5, +65 | Vdc |
| Gate-Source Voltage | V_{GS} | -0.5, +15 | Vdc |
| Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C | P_D | 250 1.43 | W W/ $^\circ\text{C}$ |
| Storage Temperature Range | T_{stg} | - 65 to +150 | $^\circ\text{C}$ |
| Case Operating Temperature | T_C | 150 | $^\circ\text{C}$ |
| Operating Junction Temperature | T_J | 200 | $^\circ\text{C}$ |

Table 2. Thermal Characteristics

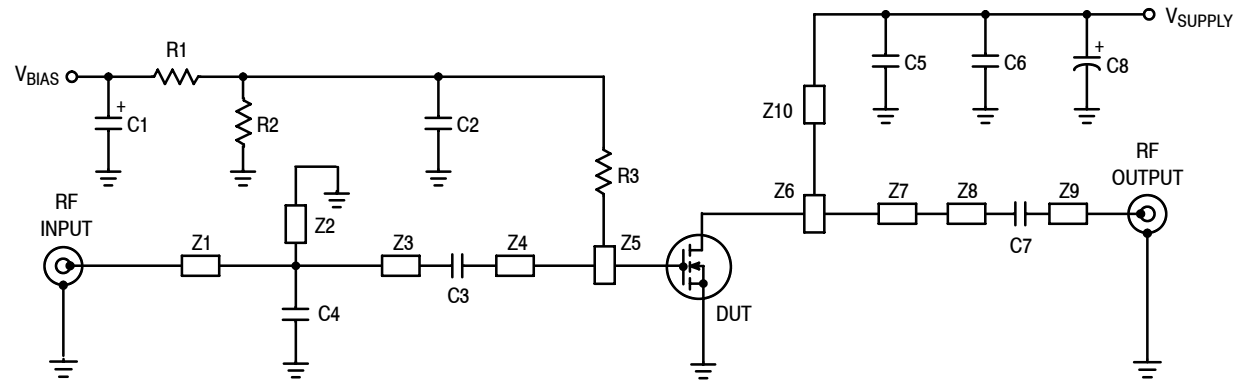
| Characteristic | Symbol | Value | Unit |
|--------------------------------------|-----------------|-------|---------------------------|
| Thermal Resistance, Junction to Case | $R_{\theta JC}$ | 0.7 | $^\circ\text{C}/\text{W}$ |

Table 3. ESD Protection Characteristics

| Test Conditions | Class |
|------------------|--------------|
| Human Body Model | 2 (Minimum) |
| Machine Model | M3 (Minimum) |

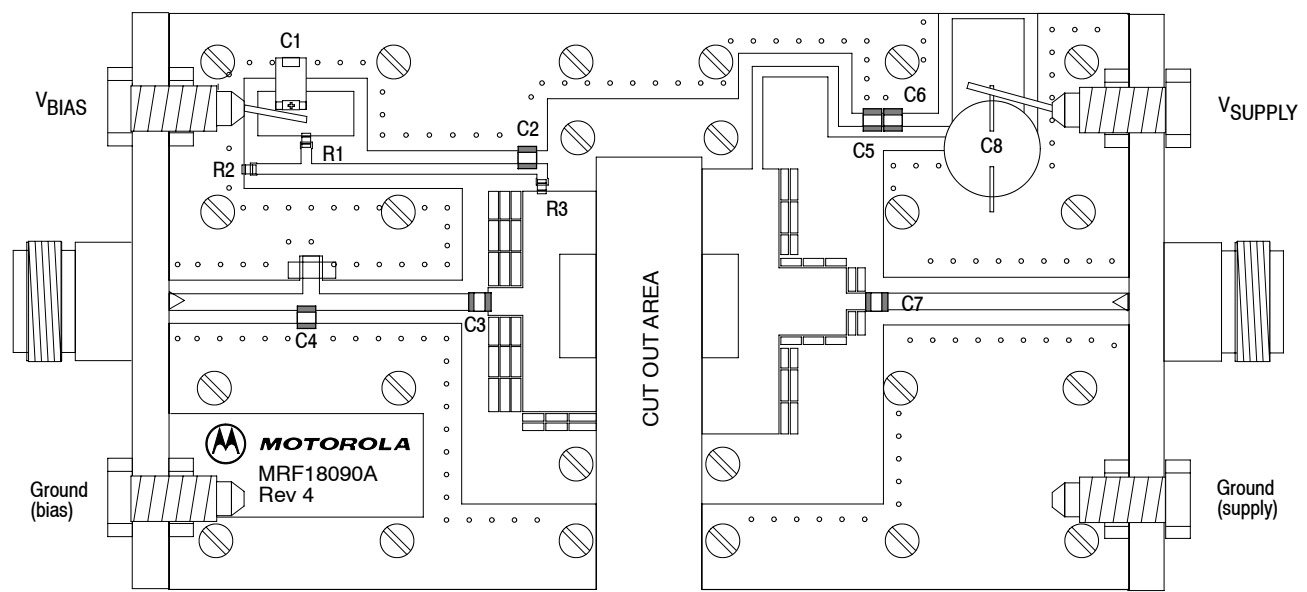
Table 4. Electrical Characteristics ($T_C = 25^\circ\text{C}$ unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|-----------------------------------------------------------------------------------------------------------------------------------|---------------|------|------|-----|-----------------|
| Off Characteristics | | | | | |
| Drain-Source Breakdown Voltage ($V_{GS} = 0\text{ Vdc}$, $I_D = 100\ \mu\text{Adc}$) | $V_{(BR)DSS}$ | 65 | — | — | Vdc |
| Zero Gate Voltage Drain Current ($V_{DS} = 26\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$) | I_{DSS} | — | — | 10 | μAdc |
| Gate-Source Leakage Current ($V_{GS} = 5\text{ Vdc}$, $V_{DS} = 0\text{ Vdc}$) | I_{GSS} | — | — | 1 | μAdc |
| On Characteristics | | | | | |
| Gate Quiescent Voltage ($V_{DS} = 26\text{ Vdc}$, $I_D = 750\text{ mAdc}$) | $V_{GS(Q)}$ | 2.5 | 3.7 | 4.5 | Vdc |
| Drain-Source On-Voltage ($V_{GS} = 10\text{ Vdc}$, $I_D = 1\text{ Adc}$) | $V_{DS(on)}$ | — | 0.1 | — | Vdc |
| Forward Transconductance ($V_{DS} = 10\text{ Vdc}$, $I_D = 3\text{ Adc}$) | g_{fs} | — | 7.2 | — | S |
| Dynamic Characteristics | | | | | |
| Reverse Transfer Capacitance ($V_{DS} = 26\text{ Vdc} \pm 30\text{ mV(rms)ac}$ @ 1 MHz, $V_{GS} = 0\text{ Vdc}$) | C_{rss} | — | 4.2 | — | pF |
| Functional Tests (In Freescale Test Fixture) | | | | | |
| Common-Source Amplifier Power Gain @ 90 W ($V_{DD} = 26\text{ Vdc}$, $I_{DQ} = 750\text{ mA}$, $f = 1805\text{ MHz}$) | G_{ps} | 12.0 | 13.5 | — | dB |
| Drain Efficiency @ 90 W ($V_{DD} = 26\text{ Vdc}$, $I_{DQ} = 750\text{ mA}$, $f = 1805\text{ MHz}$) | η | 47 | 52 | — | % |
| Input Return Loss ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 90\text{ W CW}$, $I_{DQ} = 750\text{ mA}$, $f = 1805\text{ MHz}$) | IRL | — | — | -10 | dB |



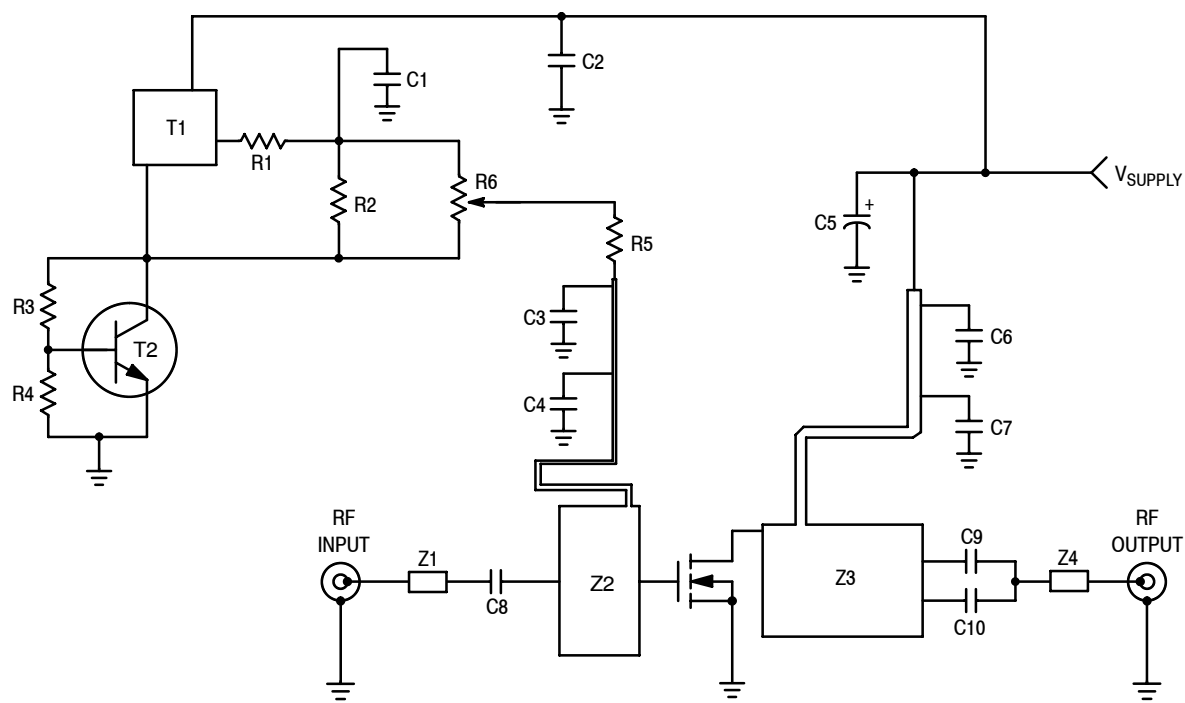
| | | | |
|--------|---------------------------------------------|-----|------------------------------------------------|
| C1 | 10 μ F, 35 V Tantalum Capacitor | Z3 | 0.819" x 0.087" Microstrip |
| C2, C3 | 10 pF, 100B Chip Capacitors | Z4 | 0.181" x 0.144" Microstrip |
| C4 | 3.3 pF, 100B Chip Capacitor | Z5 | 0.383" x 1.148" Microstrip |
| C5, C6 | 6.8 pF, 100B Chip Capacitors | Z6 | 0.400" x 1.380" Microstrip |
| C7 | 12 pF, 100B Chip Capacitor | Z7 | 0.351" x 0.351" Microstrip |
| C8 | 220 μ F, 63 V Electrolytic Capacitor | Z8 | 0.126" x 0.087" Microstrip |
| R1, R2 | 10 k Ω , 1/8 W Chip Resistors (0805) | Z9 | 1.280" x 0.087" Microstrip |
| R3 | 1.0 k Ω , 1/8 W Chip Resistor (0805) | Z10 | \approx 1.275" x 0.055" Microstrip |
| Z1 | 0.697" x 0.087" Microstrip | PCB | Taconic TLX8-0300, 0.030", $\epsilon_r = 2.55$ |
| Z2 | 0.087" x 0.197" Microstrip | | |

Figure 1. MRF18090A 1805 - 1880 MHz Test Fixture Schematic



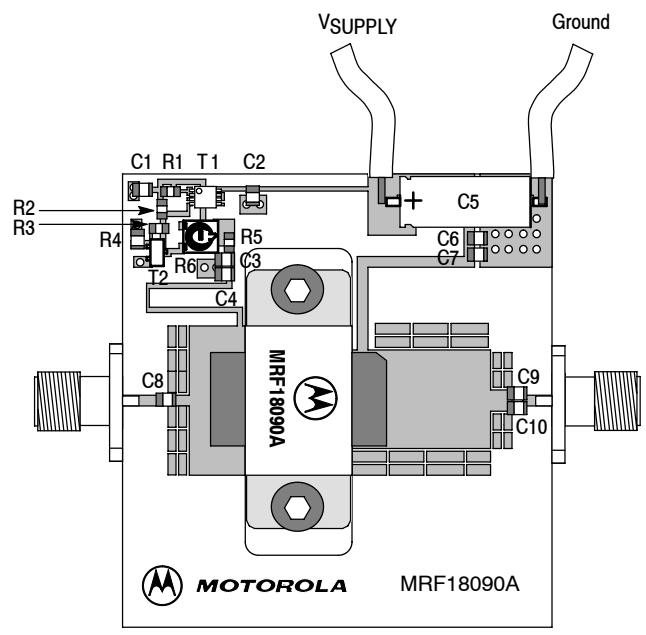
Freescale has begun the transition of marking Printed Circuit Boards (PCBs) with the Freescale Semiconductor signature/logo. PCBs may have either Motorola or Freescale markings during the transition period. These changes will have no impact on form, fit or function of the current product.

Figure 2. MRF18090A 1805 - 1880 MHz Test Fixture Component Layout



- | | | | |
|-------------|------------------------------------------|----|----------------------------------------------|
| C1, C3 | 1 μ F Chip Capacitors (0805) | R5 | 10 k Ω Chip Resistor (0603) |
| C2 | 0.1 μ F Chip Capacitor (0805) | R6 | 5 k Ω , SMD Potentiometer |
| C4 | 1 nF Chip Capacitor (0805) | T1 | LP2951 Micro-8 Voltage Regulator |
| C5 | 220 μ F, 50 V Electrolytic Capacitor | T2 | BC847 SOT-23 NPN Transistor |
| C6, C7 | 8.2 pF, 100A Chip Capacitors | Z1 | 0.210" x 0.055" Microstrip |
| C8, C9, C10 | 22 pF, 100A Chip Capacitors | Z2 | 0.419" x 0.787" Microstrip |
| R1 | 10 Ω Chip Resistor (0805) | Z3 | 0.836" x 0.512" Microstrip |
| R2, R3 | 1 k Ω Chip Resistors (0805) | Z4 | 0.164" x 0.055" Microstrip |
| R4 | 2.2 k Ω Chip Resistor (0805) | | Substrate = 0.5 mm Teflon [®] Glass |

Figure 3. 1805 - 1880 MHz Demo Board Schematic



Freescale has begun the transition of marking Printed Circuit Boards (PCBs) with the Freescale Semiconductor signature/logo. PCBs may have either Motorola or Freescale markings during the transition period. These changes will have no impact on form, fit or function of the current product.

Figure 4. 1805 - 1880 MHz Demo Board Component Layout

TYPICAL CHARACTERISTICS

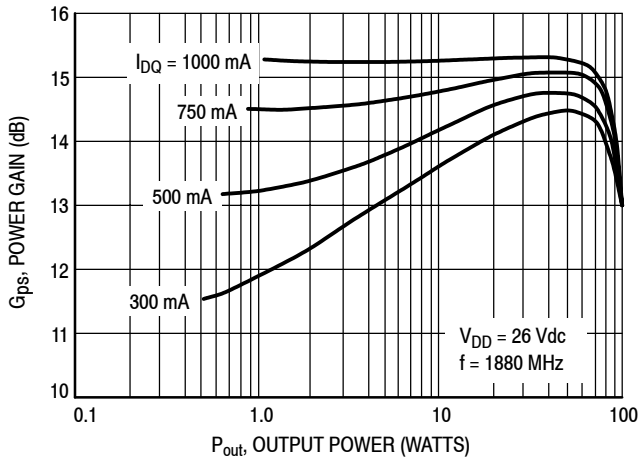


Figure 5. Power Gain versus Output Power

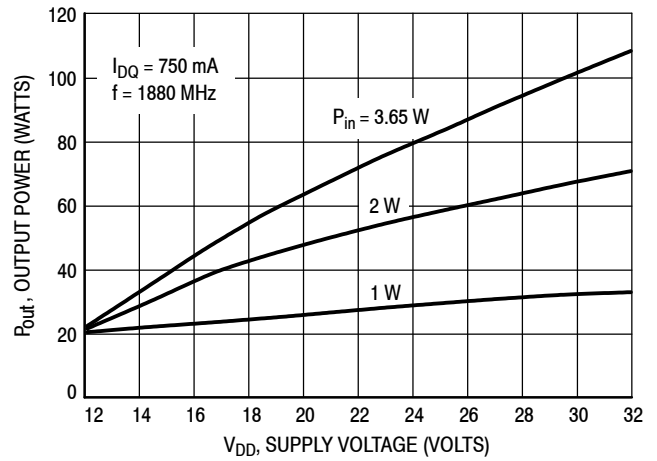


Figure 6. Output Power versus Supply Voltage

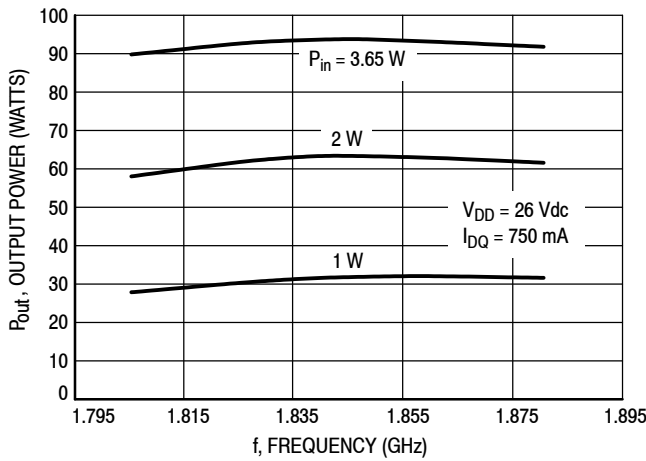


Figure 7. Output Power versus Frequency

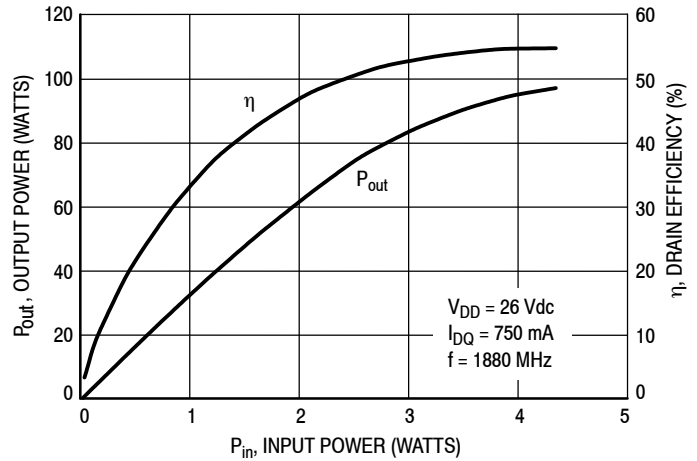


Figure 8. Output Power and Efficiency versus Input Power

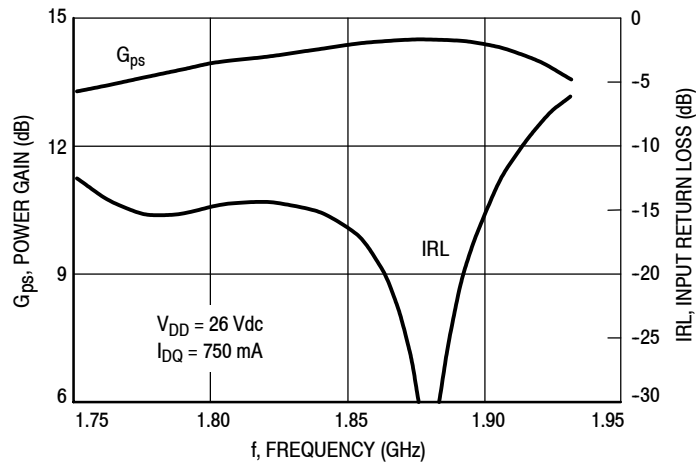
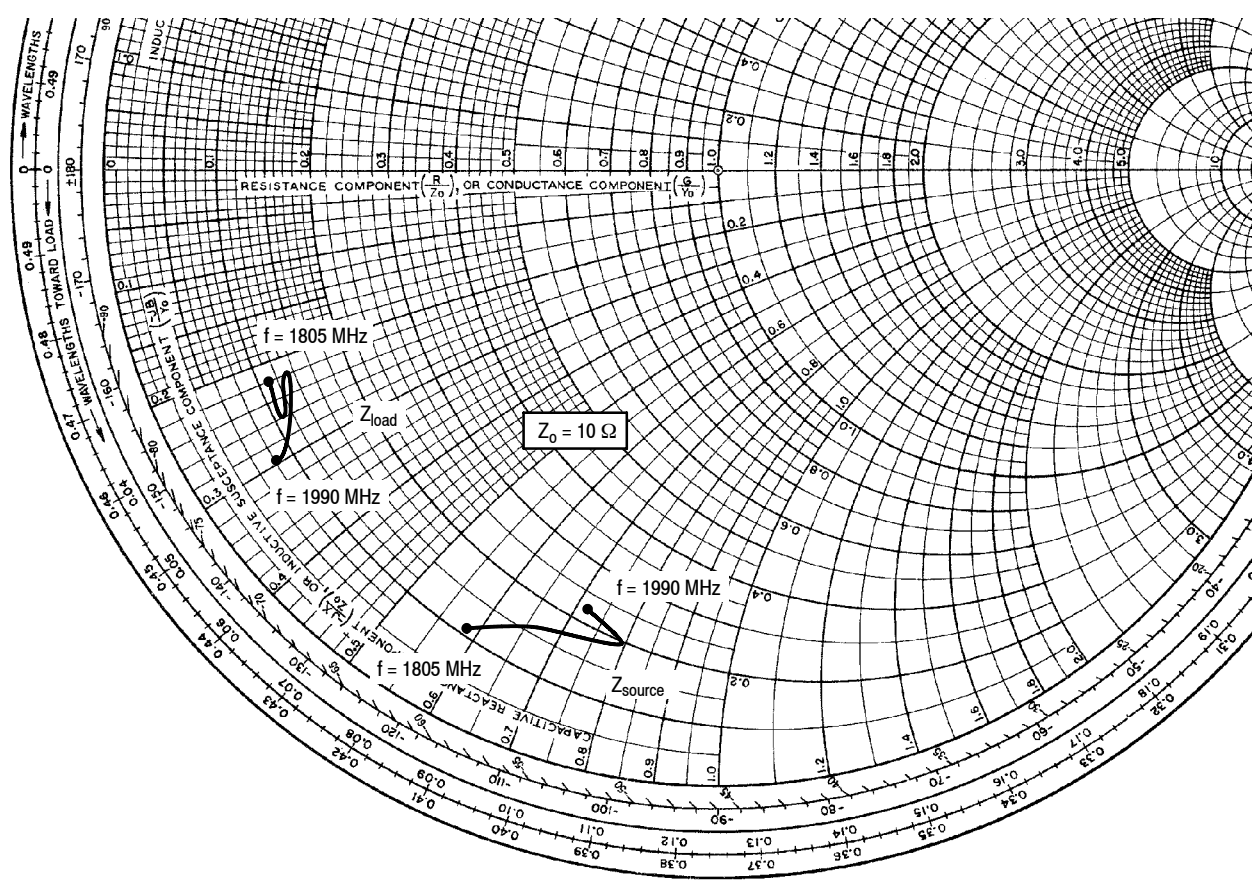


Figure 9. Wideband Gain and IRL (at Small Signal)

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$V_{DD} = 26\text{ V}$, $I_{DQ} = 750\text{ mA}$, $P_{out} = 90\text{ Watts (CW)}$

| f MHz | Z_{source} Ω | Z_{load} Ω |
|----------|--------------------------|------------------------|
| 1805 | $1.10 - j5.85$ | $1.15 - j2.16$ |
| 1880 | $1.56 - j6.75$ | $1.13 - j2.60$ |
| 1930 | $2.05 - j8.00$ | $1.30 - j2.23$ |
| 1990 | $2.30 - j7.30$ | $0.82 - j2.90$ |

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

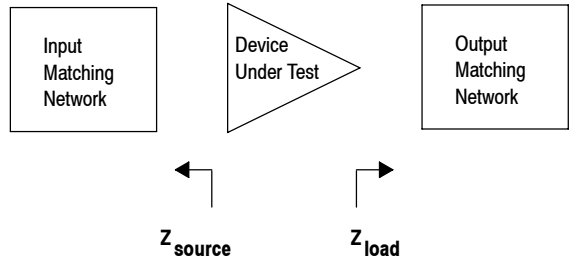
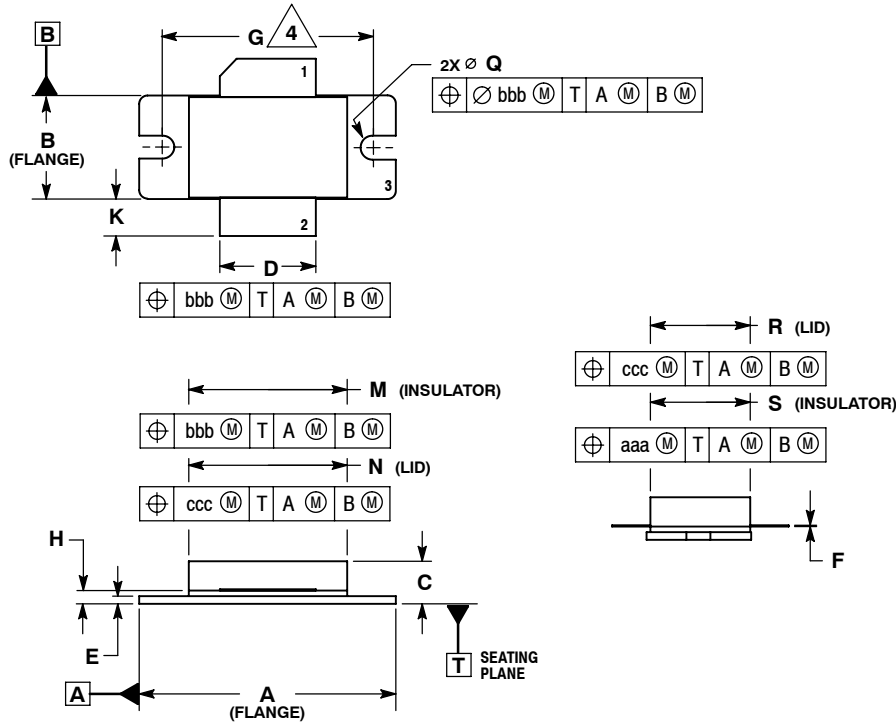


Figure 10. Large Signal Source and Load Impedance

PACKAGE DIMENSIONS



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.
4. RECOMMENDED BOLT CENTER DIMENSION OF 1.16 (29.57) BASED ON M3 SCREW.

| DIM | INCHES | | MILLIMETERS | |
|-----|-------------------|-------------------|------------------|------------------|
| | MIN | MAX | MIN | MAX |
| A | 1.335 | 1.345 | 33.91 | 34.16 |
| B | 0.535 | 0.545 | 13.6 | 13.8 |
| C | 0.147 | 0.200 | 3.73 | 5.08 |
| D | 0.495 | 0.505 | 12.57 | 12.83 |
| E | 0.035 | 0.045 | 0.89 | 1.14 |
| F | 0.003 | 0.006 | 0.08 | 0.15 |
| G | 1.100 BSC | | 27.94 BSC | |
| H | 0.057 | 0.067 | 1.45 | 1.70 |
| K | 0.175 | 0.205 | 4.44 | 5.21 |
| M | 0.872 | 0.888 | 22.15 | 22.55 |
| N | 0.871 | 0.889 | 19.30 | 22.60 |
| Q | \emptyset 1.118 | \emptyset 1.138 | \emptyset 3.00 | \emptyset 3.51 |
| R | 0.515 | 0.525 | 13.10 | 13.30 |
| S | 0.515 | 0.525 | 13.10 | 13.30 |
| aaa | 0.007 REF | | 0.178 REF | |
| bbb | 0.010 REF | | 0.254 REF | |
| ccc | 0.015 REF | | 0.381 REF | |

STYLE 1:

- PIN 1. DRAIN
- 2. GATE
- 3. SOURCE

CASE 465B-03
ISSUE D
NI-880

PRODUCT DOCUMENTATION

Refer to the following documents to aid your design process.

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

REVISION HISTORY

The following table summarizes revisions to this document.

| Revision | Date | Description |
|----------|-----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 8 | Oct. 2008 | <ul style="list-style-type: none"> • Modified data sheet to reflect RF Test Reduction described in Product and Process Change Notification number, PCN12779, p. 1, 2 • Added Product Documentation and Revision History, p. 8 |
| | Dec. 2010 | <ul style="list-style-type: none"> • Data sheet archived. Part no longer manufactured. |

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