19-0197; Rev 1; 1/95

MAXIM

CCFL Backlight and LCD Contrast Controllers

General Description

The MAX753/MAX754 drive cold-cathode fluorescent lamps (CCFLs) and provide the LCD backplane bias (contrast) power for color or monochrome LCD panels. These ICs are designed specifically for backlit notebook-computer applications.

Both the backplane bias and the CCFL supply can be shut down independently. When both sections are shut down, supply current drops to 25µA. The LCD contrast and CCFL brightness can be adjusted by clocking separate digital inputs or using external potentiometers. LCD contrast and backlight brightness settings are preserved in their respective counters while in shutdown. On power-up, the LCD contrast counter and CCFL brightness counter are set to one-half scale.

The ICs are powered from a regulated 5V supply. The magnetics are connected directly to the battery, for maximum power efficiency.

The CCFL driver uses a Royer-type resonant architecture. It can provide from 100mW to 6W of power to one or two tubes. The MAX753 provides a negative LCD bias voltage; the MAX754 provides a positive LCD bias voltage.

Applications

Notebook Computers

Palmtop Computers

Pen-Based Data Systems

Personal Digital Assistants

Portable Data-Collection Terminals

Features

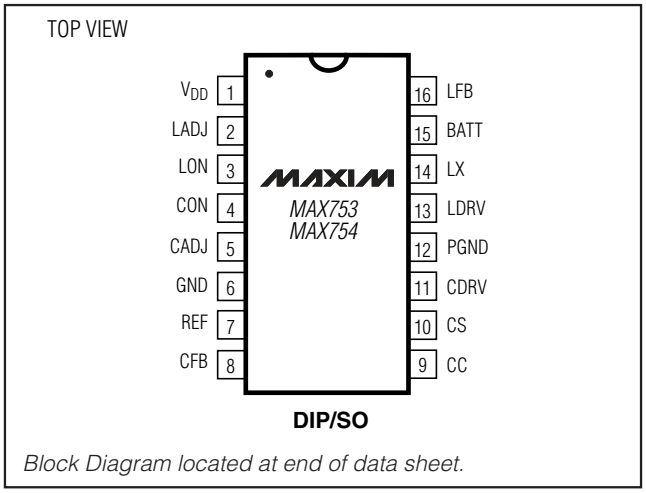
- ♦ **Drives Backplane and Backlight**
- ♦ **4V to 30V Battery Voltage Range**
- ♦ **Low 500µA Supply Current**
- ♦ **Digital or Potentiometer Control of CCFL Brightness and LCD Bias Voltage**
- ♦ **Negative LCD Contrast (MAX753)**
- ♦ **Positive LCD Contrast (MAX754)**
- ♦ **Independent Shutdown of Backlight and Backplane Sections**
- ♦ **25µA Shutdown Supply Current**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX753CPE	0°C to +70°C	16 Plastic DIP
MAX753CSE	0°C to +70°C	16 Narrow SO
MAX753C/D	0°C to +70°C	Dice*
MAX753EPE	-40°C to +85°C	16 Plastic DIP
MAX753ESE	-40°C to +85°C	16 Narrow SO
MAX754CPE	0°C to +70°C	16 Plastic DIP
MAX754CSE	0°C to +70°C	16 Narrow SO
MAX754C/D	0°C to +70°C	Dice*
MAX754EPE	-40°C to +85°C	16 Plastic DIP
MAX754ESE	-40°C to +85°C	16 Narrow SO

** Contact factory for dice specifications.*

Pin Configuration



Block Diagram located at end of data sheet.

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

CCFL Backlight and LCD Contrast Controllers

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND .....-0.3V, +7V
PGND to GND .....±0.3V
BATT to GND .....-0.3V, +36V
LX to GND .....±50V
CS to GND .....-0.6V, (V_{DD} + 0.3V)
Inputs/Outputs to GND (LADJ, CADJ, LON, CON, REF, CFB, CC, CDRV, LDRV, LFB) .....-0.3V, (V_{DD} + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 10.53mW/°C above +70°C) 842mW
Narrow SO (derate 8.70mW/°C above +70°C) 696mW

Operating Temperature Ranges
MAX75_C_ _ .....0°C to +70°C
MAX75_E_ _.....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +160°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 5V, BATT = 15V, CON = LON = 5V, LX = GND = PGND = 0V, I_{REF} = 0mA, all digital input levels are 0V or 5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SUPPLY AND REFERENCE						
BATT Input Range			4		30	V
V_{DD} Supply Range			4.5		5.5	V
REF Output Voltage	No external load		1.21	1.25	1.29	V
REF Line Regulation	4V < V_{DD} < 6V				0.1	%/V
REF Load Regulation	0µA < I_L < 100µA			5	15	mV
V_{DD} Quiescent Current	LON = CON = CS = LFB = CFB = LADJ = CADJ = 5V			0.5	2	mA
V_{DD} Shutdown Current	LON = CON = CS = LFB = CFB = LADJ = CADJ = LX = BATT = 0V (Note 1)			25	40	µA
DIGITAL INPUTS AND DRIVER OUTPUTS						
Input Low Voltage	LON, CON, CADJ, LADJ; V_{DD} = 4.5V				0.8	V
Input High Voltage	LON, CON, CADJ, LADJ; V_{DD} = 5.5V		2.4			V
Input Leakage Current	LON, CON, CADJ, LADJ; V_{IN} = 0V or 5V				±1	µA
Driver Sink/Source Current	LDRV = CDRV = 2V			0.5		A
Driver On-Resistance	LDRV, CDRV; V_{DD} = 4.5V	Output high			10	Ω
		Output low			7	
CCFT CONTROLLER						
Zero-Crossing-Comparator Threshold Voltage (CS)			-10		20	mV
Overcurrent-Comparator Threshold Voltage (CS)			1.2		1.3	V
CS Input Bias Current	V_{CS} = 0V				-5	µA
VCO Frequency	Minimum, CFB = 5V		32		47	kHz
	Maximum, CFB = 0V		85		115	
DAC Resolution	Guaranteed monotonic		5			Bits

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 5V, BATT = 15V, CON = LON = 5V, LX = GND = PGND = 0V, I_{REF} = 0mA, all digital input levels are 0V or 5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Feedback Voltage (CFB)	At full scale (DAC code = 31)	1210	1250	1290	mV
	At preset DAC, CON = 0V, CADJ = 5V (code = 15)	745	782	820	
	At zero scale (code = 0)	320	343	365	
Feedback-Amplifier Input Bias Current				±100	nA
Feedback-Amplifier Unity-Gain Bandwidth			1		MHz
Feedback-Amplifier Slew Rate			0.4		V/µs
Feedback-Amplifier Output Current	Source current, CFB = 0V, CC = 2.5V	50			µA
	Sink current, CFB = 5V, CC = 2.5V	200			
LCD CONTROLLER					
Switch On-Time	BATT = 4V	2		5	µs
	BATT = 16V	0.5		1.5	
Switching Period	BATT = 4V, LX = 0V	35		70	µs
DAC Resolution	Guaranteed monotonic	6			Bits
MAX753 Feedback Voltage (REF-LFB)	At full scale (DAC code = 63)	1200	1240	1280	mV
	At preset DAC, LON = 0V, LADJ = 5V (code = 31)	893	928	963	
	At zero scale (code = 0)	595	625	655	
MAX754 Feedback Voltage (LFB)	At full scale (DAC code = 63)	1210	1250	1290	mV
	At preset DAC, LON = 0V, LADJ = 5V (code = 31)	905	938	971	
	At zero scale (code = 0)	610	635	660	
LFB Input Leakage Current				±150	nA
BATT Input Current	LON = CON = CS = LFB = CFB = LADJ = CADJ = LX = 0V		12	20	µA
LX Input Current	LON = CON = CS = LFB = CFB = LADJ = CADJ = 0V, LX = BATT = 15V		12	20	µA
TIMING (Note 2)					
Reset Pulse Width (t_R)		110			ns
Reset Setup Time (t_{RS})		0			ns
Reset Hold Time (t_{RH})		0			ns
CADJ, LADJ High Width (t_{SH})		100			ns
CADJ, LADJ Low Width (t_{SL})		100			ns
CADJ Low to CON Low or LADJ Low to LON Low (t_{SD})		50			ns

Note 1: Maximum shutdown current occurs at BATT = LX = 0V.
Note 2: Timing specifications are guaranteed by design and not production tested.

CCFL Backlight and LCD Contrast Controllers

Pin Description

PIN	NAME	FUNCTION
1	V_{DD}	5V Power-Supply Input
2	LADJ	Digital Input for LCD Backplane Bias Adjustment. See Table 1.
3	LON	Digital Input to Control LCD Bias Section. See Table 1.
4	CON	Digital Input to Control CCFT Section. See Table 1.
5	CADJ	Digital Input for CCFT Brightness Adjustment. See Table 1.
6	GND	Analog Ground
7	REF	Reference Voltage Output, 1.25V
8	CFB	Inverting Input for the CCFT Error Amplifier
9	CC	Output of the CCFT Error Amplifier
10	CS	Connect to V_{DD}
11	CDRV	Leave unconnected
12	PGND	Power Ground Connection for LDRV
13	LDRV	Gate-Driver Output. Drives LCD backplane N-channel MOSFET.
14	LX	LCD Backplane Inductor Voltage-Sense Pin. Used to sense inductor voltage for on time determination.
15	BATT	Battery Connection. Used to sense battery voltage for on time determination.
16	LFB	Voltage Feedback for the LCD Backplane Section

Theory of Operation

CCFL Inverter

The MAX753/MAX754's CCFL inverter is designed to drive one or two cold-cathode fluorescent lamps (CCFLs) with power levels from 100mW to 6W. These lamps commonly provide backlighting for LCD panels in portable computers.

Drive Requirements for CCFL Tubes

CCFL backlights require a high-voltage, adjustable AC power source. The MAX753/MAX754 generate this AC waveform with a self-oscillating, current-fed, parallel resonant circuit, also known as a Royer-type oscillator.

Figure 1 shows one such circuit. The Royer oscillator is comprised of T1, C9, the load at the secondary, Q4, and Q5. The circuit self-oscillates at a frequency determined by the effective primary inductance and capacitance. Q4 and Q5 are self-driven by the extra winding. The current source feeding the Royer oscillator is comprised of L1, D5, and the MAX758A. When current from the current source increases, so does the lamp current.

The lamp current is half-wave rectified by D7A and D7B, and forms a voltage across resistor R8. The MAX753's error amplifier compares the average of this voltage to the output of its internal DAC. Adjusting the DAC output from zero scale to full scale (digital control) causes the error amplifier to vary the tube current from a minimum to a maximum. The DAC's transfer function is shown in Figure 2.

On power-up or after a reset, the counter sets the DAC output to mid scale. Each rising edge of CADJ (with CON high) decrements the DAC output. When decremented beyond full scale, the counter rolls over and sets the DAC to the maximum value. In this way, a single pulse applied to CADJ decreases the DAC set-point by one step, and 31 pulses increase the set-point by one step.

The error amplifier's output voltage controls the peak current output of the MAX758A. The peak switch current is therefore controlled by the output of the error amplifier. The lower the error amplifier's output, the lower the peak current. Since the current through the current source is related to the current through the tube, the lower the error amplifier's output, the lower the tube current.

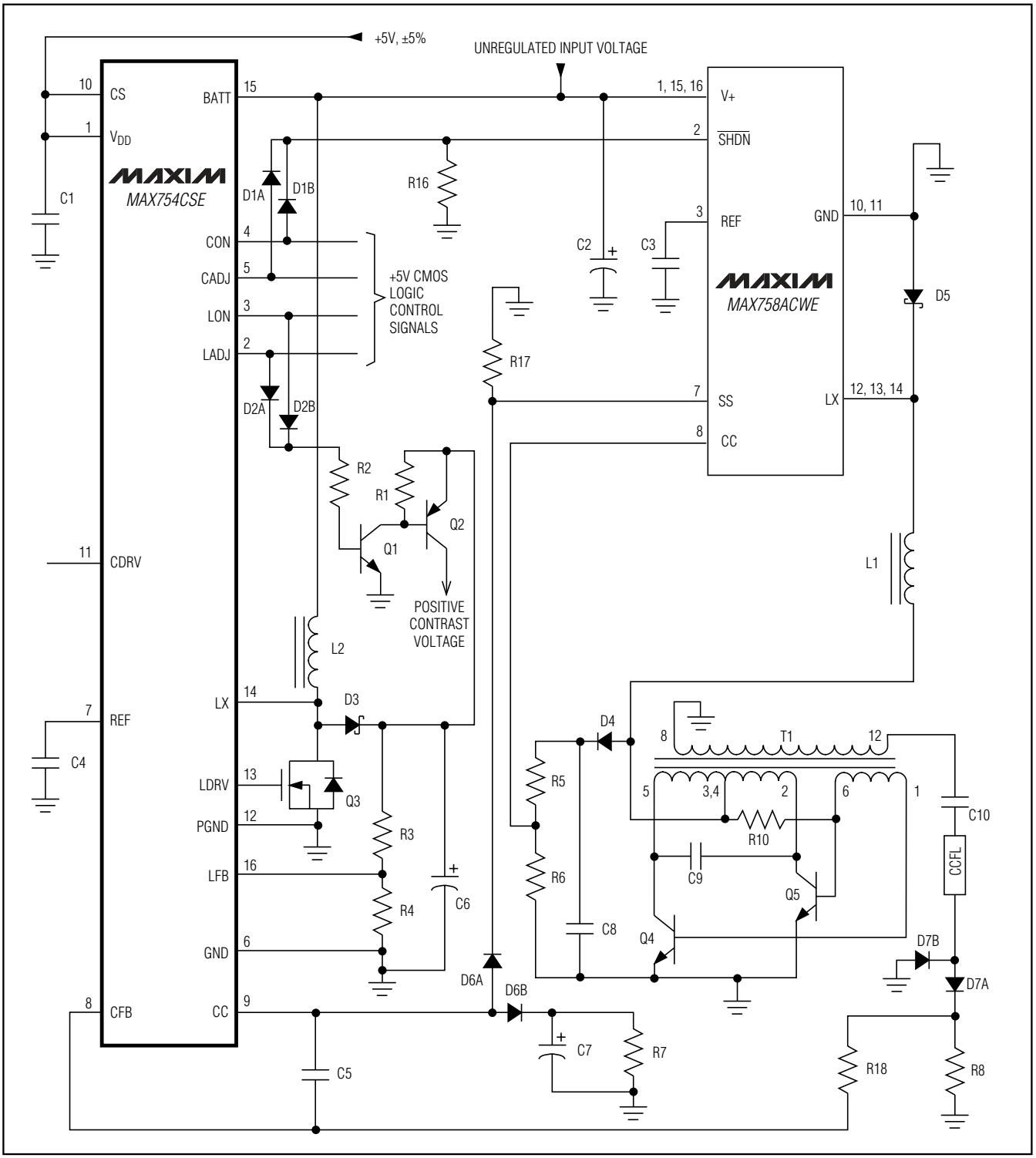


Figure 1. CCFL and Positive LCD Power Supply

CCFL Backlight and LCD Contrast Controllers

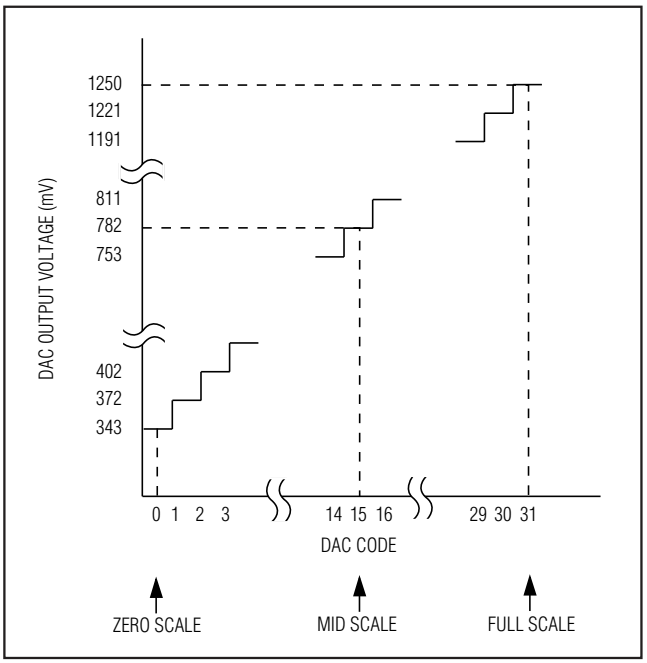


Figure 2. CCFT DAC Transfer Function

In Figure 1, the MAX758A, L1, and D5 form a voltage-controlled switch-mode current source. The current out of L1 is proportional to the voltage applied to the SS pin. The MAX758A contains a current-mode pulse-width-modulating buck regulator that switches at 170kHz. The voltage on the SS pin sets the switch current limit and thus sets the current out of L1.

CCFL Current-Regulation Loop

Figure 3 shows a block diagram of the regulation loop, which maintains a fixed CCFL average lamp current despite changes in input voltage and lamp impedance. This loop regulates the average value of the half-wave rectified lamp current. The root mean square lamp current is related to, but not equal to, the average lamp current. Assuming a sinusoidal lamp current, select R8 as follows:

$$R8 = \frac{\pi V_{REF}}{\sqrt{2}\ I_{LAMP,RMS}}$$

where V_{REF} = 1.25V and $I_{LAMP,RMS}$ is the desired full-scale root mean square lamp current.

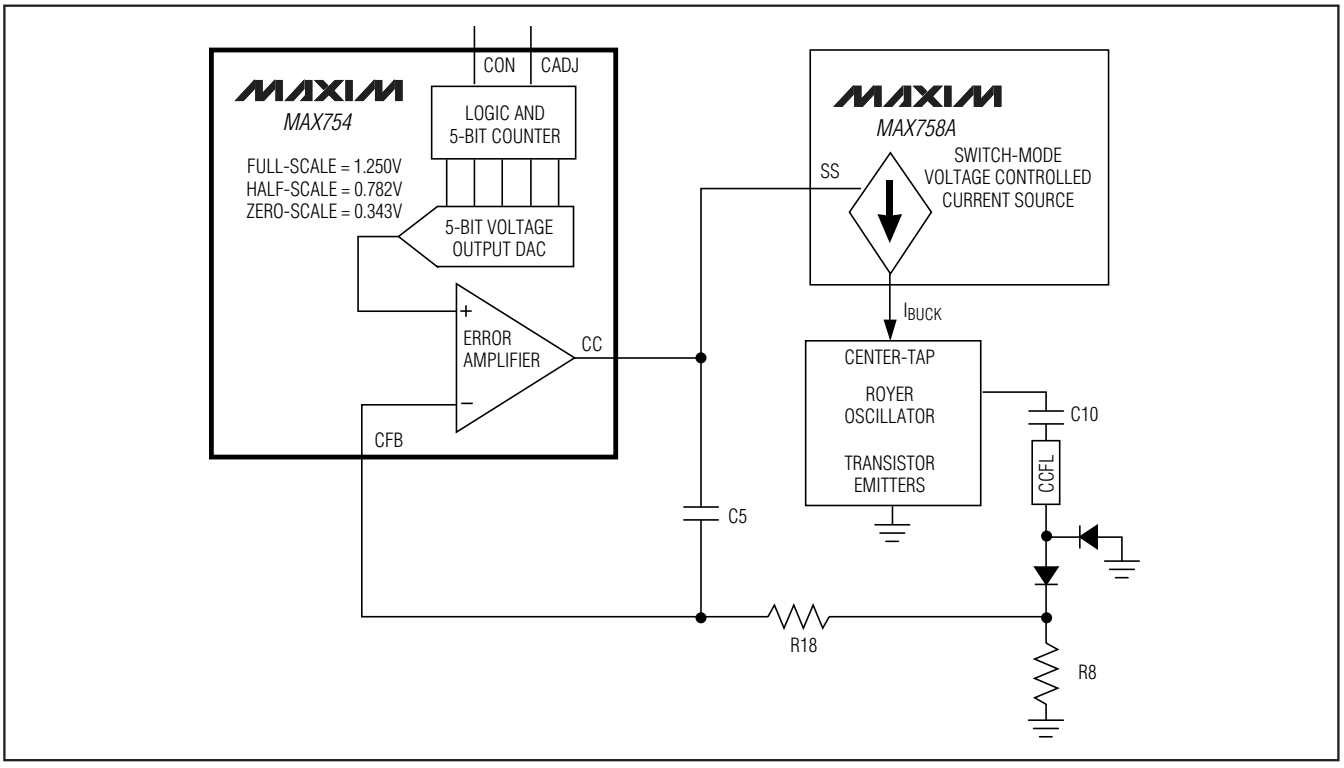


Figure 3. CCFL Tube Current-Regulation Loop

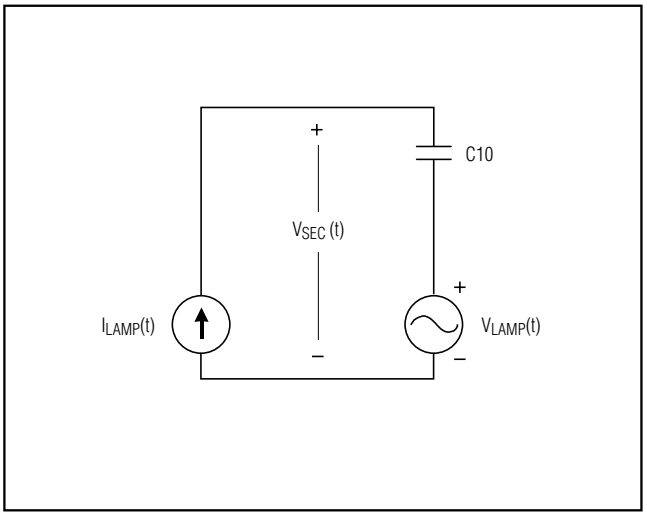


Figure 4. Simple Model of the CCFL

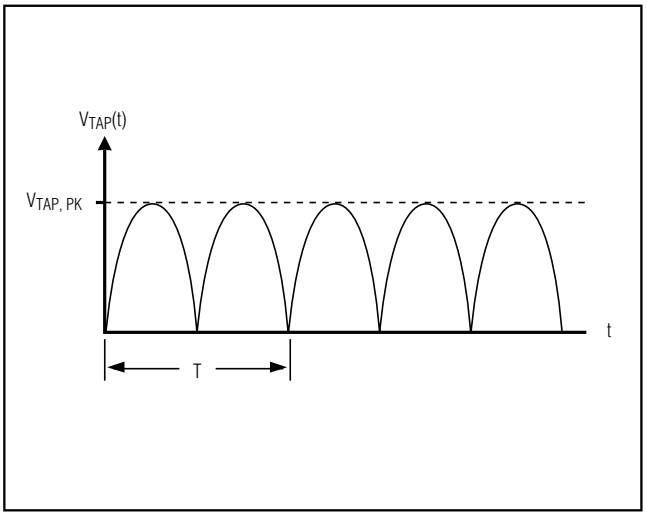


Figure 5. Voltage at the Center Tap of T1

The minimum operating input voltage is determined by the transformer turns ratio (n), the lamp operating voltage (V_{LAMP}), and the ballast capactor (C10). Using a simple model of the CCFL (see Figure 4) we can calculate what the T1 center-tap voltage will be at maximum lamp current. The voltage on the CCFL is in phase with the current through it. Let us define $I_{LAMP}(t) = \sqrt{2} I_{LAMP,RMS} \cos(\omega t)$ and $V_{LAMP}(t) = \sqrt{2} V_{LAMP,RMS} \cos(\omega t)$; then the peak voltage at the center tap will be as follows:

$$V_{TAP,PK} = - \frac{\sqrt{2}\ I_{LAMP,RMS}}{n\omega C10 \sin(\phi)}$$

where,

$$\phi = \tan^{-1}\left(\frac{-I_{LAMP,RMS}}{\omega C10 V_{LAMP,RMS}} \right) ,$$

n is the secondary-to-primary turns ratio of T1, and ω is the frequency of Royer oscillation in radians per second. The voltage on the center tap of T1 is a full-wave rectified sine wave (see Figure 5). The average voltage at V_{TAP} must equal the average voltage at the LX node of the MAX758A, since there cannot be any DC voltage on inductor L1; thus the minimum operating voltage must be greater than the average voltage at V_{TAP}.

LCD Bias Generators

The MAX753/MAX754's LCD bias generators provide adjustable output voltages for powering LCD displays. The MAX753's LCD converter generates a negative output, while the MAX754's generates a positive output. The MAX753/MAX754 employ a constant-peak-current pulse-frequency-modulation (PFM) switching regulator. The MAX753 adds a simple diode-capacitor voltage inverter to the switching regulator.

Constant-Current PFM Control Scheme

The LCD bias generators in these devices use a constant-peak-current PFM control scheme. Figure 6, which shows the MAX754's boost switching regulator, illustrates this control method. When Q3 closes (Q3 "on") a voltage equal to BATT is applied to the inductor, causing current to flow from the battery, through the inductor and switch, and to ground. This current ramps up linearly, storing energy in the inductor's magnetic field. When Q3 opens, the inductor voltage reverses, and current flows from the battery, through the inductor and diode, and into the output capacitor. The devices regulate the output voltage by varying how frequently the switch is opened and closed.

The MAX753/MAX754 not only regulate the output voltage, but also maintain a constant peak inductor current, regardless of the battery voltage. The ICs vary the switch on-time to produce the constant peak current, and vary its off-time to ensure that the inductor current reaches zero at the end of each cycle.

The internal circuitry senses both the output voltage and the voltage at the LX node, and turns on the MOSFET only if: 1) The output voltage is out of regulation, and 2) the voltage at LX is less than the battery voltage. The first condition keeps the output in regulation, and the second ensures that the inductor current always resets to zero (i.e., the part always operates in discontinuous-conduction mode).

CCFL Backlight and LCD Contrast Controllers

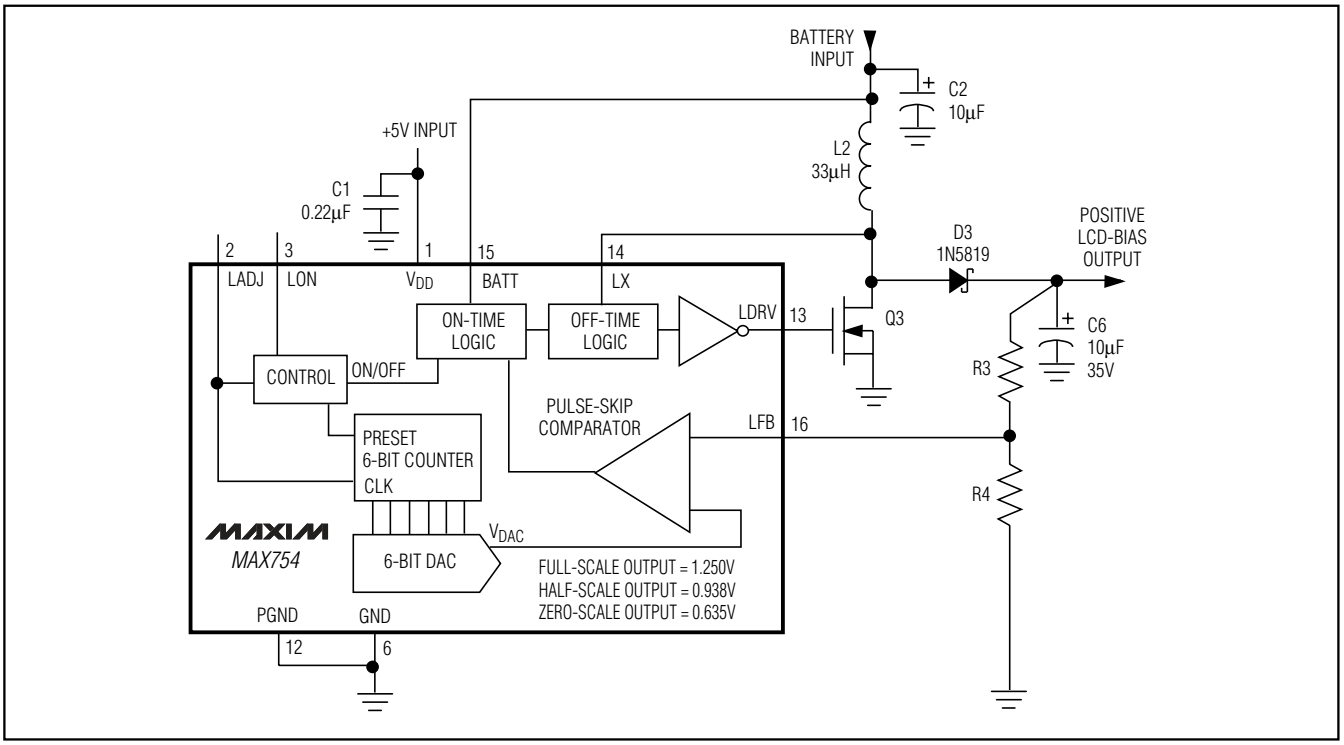


Figure 6. MAX754 Positive LCD-Bias Generator

Table 1. CCFL Circuit Component Descriptions

ITEM	DESCRIPTION
C5	Integrating Capacitor. 1 / (C5 x R18) sets the dominant pole for the feedback loop, which regulates the lamp current. Set the dominant pole at least two decades below the Royer frequency to eliminate the AC component of the voltage on R8. For example, if your Royer is oscillating at 50kHz = 314159rad/s, you should set 1 / (C5 x R18) ≤ 3142rad/s.
R18	Integrating Resistor. The output source-current capability of the CC pin (50µA) limits how small R18 can be. Do not make R18 smaller than 70kΩ, otherwise CC will not be able to servo CFB to the DAC voltage (i.e., the integrator will not be able to integrate) and the loop will not be able to regulate.
R8	R8 converts the half-wave rectified lamp current into a voltage. The average voltage on R8 is **not** equal to the root mean square voltage on R8. The accuracy of R8 is important since it, along with the MAX754 reference, sets the full-scale lamp current. Use a ±1%-accurate resistor.
D7A, D7B	D7A and D7B half-wave rectify the CCFL lamp current. Half-wave rectification of the lamp current and then averaging is a simple way to perform AC-to-DC conversion. D7A and D7B's forward voltage drop and speed are unimportant; they do not need to pass currents larger than about 10mA, and their reverse breakdown voltage can be as low as 10V.
CCFL	The circuit of Figure 1, with the components shown in the bill of materials (Table 4), will drive a 500V_{RMS} operating cold-cathode fluorescent lamp at 6W of power with a +12V input voltage. The lower the input voltage, the less power the circuit can deliver.

Table 1. CCFL Circuit Component Descriptions (continued)

ITEM	DESCRIPTION
C10	The ballast capacitor linearizes the CCFL impedance and guarantees no DC current through the lamp. 15pF will work with just about any lamp. Depending on the lamp, you can try higher values, but this may cause the regulation loop to become unstable. Larger values of C10 allow the circuit to operate with lower input voltages. Don't forget that C10 must be a high-voltage capacitor and cannot be polarized. A lamp with a $1500V_{RMS}$ maximum strike voltage will require C10 to withstand $1500 \times \sqrt{2} = 2121V$.
T1	T1 must have high primary inductance (greater than 30µH), otherwise an inflated value of C9 will be required in order to keep the Royer frequency below 60kHz (the maximum allowed by most lamps). A higher T1 secondary-to-primary turns ratio allows lower-voltage operation, but increases the size of the transformer.
C9	You must select a value for C9 high enough to keep the lamp current reasonably sinusoidal and yet low enough that T1's core does not saturate. For the Sumida EPS207 with a 171:1 turns ratio, choose a 0.22µF value for C9. The characteristic impedance of the resonant tank equals $\sqrt{\frac{L_{MAG}}{C9}}$, where L_{MAG} is the magnetizing inductance of T1. The characteristic impedance is defined as the ratio of the voltage across the parallel LC circuit divided by the current flowing between the inductor and capacitor. This circulating current is not delivered to the load. If C9 has too large a value, it will cause excessive circulating currents, which will in turn saturate the core of T1. It's easy to tell when you have excess circulating current in the resonant tank, because when you touch T1 you burn your finger. However, reducing the value of C9 decreases tank Q, which increases the harmonic content of the lamp-current waveform. If the lamp-current waveform does not look sinusoidal, then the circuit may not regulate to the right root mean square current.
R10	R10 sets the base current for Q4 and Q5. If you choose too large a value for R10, Q4 and Q5 will overheat. Too small a value will waste base current and slightly degrade efficiency. The optimal value will depend on how much power you are trying to deliver to the lamp. 510Ω is a good "always works but may not be the most efficient" value for use with the FMMT619 transistors from ZETEX.
R5, R6	This resistive divider senses the voltage at the center tap of T1. When the CC pin on the MAX758A rises above 1.25V, the internal switch turns off, interrupting power to the Royer oscillator and limiting the open-lamp transformer center-tap voltage.
D6B, C7, R7	D6B, C7, and R7 form a soft-start clamp, which limits the rate-of-rise of the peak current in the MAX758A. Make sure R7 is at least 100kΩ so it does not excessively load the CC pin.
D6A, R17	D6A and R17 are also part of the soft-start clamp. The voltage on the SS pin controls the peak current in the MAX758A's switch. Make sure R17 is at least 100kΩ so it does not excessively load the CC pin.
L1	Inductor for the Switching-Current Source. Use a 47µH to 150µH inductor with a 1A to 1.5A saturation current.
D5	Schottky Catch Diode. Use a 1A to 1.5A Schottky diode with low forward-voltage power.
C2	Supply Bypass Capacitor. Use low-ESR capacitor.

Table 2. CCFL Circuit Design Example (Note 1)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
CCFL Specifications					
Strike Voltage (V_S)	$V_{S,RMS}$	1100		1500	V_{RMS}
Discharging Tube Current (I_L)	$I_{LAMP,RMS}$	0.001376		0.005	A_{RMS}
Discharging Tube Voltage (V_L)	$V_{LAMP,RMS}$		435		V_{RMS}
LCD Contrast Voltage Specifications					
Bias Voltage	V_{LCD}	16.3		32.6	V
Output Current	I_{LCD}	0.0245			A
Royer Specifications					
T1 Turns Ratio (Sec/Pri) (Note 2)	n		171		
T1 Resonating Inductance (Note 2)	L_{MAG}		0.000045		H
C9 Value (Note 3)	C_{RES}		2.2E-07		F
C10 Value	C_{BAL}		1.5E-11		F
Royer Frequency	w		317820.86		rad/s
MAX754 Specifications					
Reference Voltage	V_{REF}		1.25		V
Second Volts Constant	sV	0.000008		2.4E-05	sV
CCFL Circuit Calculations					
R8 Current-Sensing Resistor	R8		555.36037		Ω
Secondary Voltage Phase vs. Tube Voltage	phi		-1.1776341		Radian
T1 Center-Tap Peak Voltage	$V_{TAP,PK}$		9.3903817		V_{PEAK}
Secondary Limit Voltage	V_{LIM}		1350		V_{RMS}
T1 Center-Tap Limit Peak Voltage			11.164844		V_{PEAK}
R5/R6	$R_{OTP,RATIO}$		0.1341944		Ω/Ω
LCD Circuit Calculations					
$V_{IN(min)}$ Full-Load Switching Period	T_{FL}		1.639E-06		s
L2 Inductance	L2	1.96E-05		2.4E-05	H
L2 Peak Currrent				1.22704	A
R4/R3	$R_{LCD,RATIO}$		0.0398724		Ω/Ω
Application Circuit Operating Range					
Input Voltage	V_{IN}	5.978103		18	V

Note 1: To perform your own calculations for the parameters given in Table 2 (Design Example), use the equations given in Table 3 (Design Equations).

Note 2: T1 = Sumida's EPS207

Note 3: C9 = Wima's SMD 7.3 __/63

Table 3. Spreadsheet Design Equations

PARAMETER	SYMBOL	MIN	TYP	MAX
CCFL Specifications				
Strike Voltage (V_S)	$V_{S,RMS}$	1100		1500
Discharging Tube Current (I_L)	$I_{LAMP,RMS}$	= 0.28 * $I_{LAMP,RMS(max)}$		0.005
Discharging Tube Voltage (V_L)	$V_{LAMP,RMS}$		435	
LCD Contrast Voltage Specifications				
Bias Voltage	V_{LCD}	= $V_{LCD(max)}$ / 2		32.6
Output Current	I_{LCD}	0.0245		
Royer Specifications				
T1 Turns Ratio (Sec/Pri)	n		171	
T1 Resonating Inductance	L_{MAG}		0.000045	
C9 Value	C_{RES}		2.2E-07	
C10 Value	C_{BAL}		1.5E-11	
Royer Frequency	w		= SQRT [1 / (L_{MAG} * C_{RES})]	
MAX754 Specifications				
Reference Voltage	V_{REF}		1.25	
Second Volts Constant	sV	0.000008		2.4E-05
CCFL Circuit Calculations				
R8 Current-Sensing Resistor	R8		= PI() * V_{REF} * SQRT(2) / (2 * $I_{LAMP,RMS(max)}$)	
Secondary Voltage Phase vs. Tube Voltage	phi		= ATAN (-$I_{LAMP,RMS(max)}$ / (C_{BAL} * w * + $V_{LAMP,RMS}$)	
T1 Center-Tap Peak Voltage	$V_{TAP,PK}$		= -SQRT(2) * $I_{LAMP,RMS(max)}$ / (C_{BAL} * w * SIN(phi)) / n	
Secondary Limit Voltage	V_{LIM}		= $V_{S,RMS(max)}$ * 0.9	
T1 Center-Tap Limit Peak Voltage			= SQRT(2) * V_{LIM} / n	
R5/R6	$R_{OTP,RATIO}$		= V_{REF} / (D25 - 0.6 - V_{REF})	
LCD Circuit Calculations				
$V_{IN(min)}$ Full-Load Switching Period	T_{FL}		= sV(min) / $V_{IN(min)}$ + sV(min) / ($V_{LCD(max)}$ - $V_{IN(min)}$)	
L2 Inductance	L2	= L2(max) * 0.8		= sV(min) ^ 2 / (2 * T_{FL} * $V_{LCD(max)}$ * $I_{LCD(min)}$)
L2 Peak Currrent				= sV(max) / L2(min)
R4/R3	$R_{LCD,RATIO}$		= V_{REF} / ($V_{LCD(max)}$ - V_{REF})	
Application Circuit Operating Range				
Input Voltage	V_{IN}	= (2 / PI()) * $V_{TAP,PK}$		18

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Table 4. Bill of Materials

RESISTOR	VALUE (Ω)	TOLERANCE (%)
R1	100,000	±10
R2	100,000	±10
R3	1,000,000	±1
R4	40,200	±1
R5	100,000	±1
R6	13,300	±1
R7	100,000	±10
R8	549	±1
R10	680	±5
R16	100,000	±10
R17	100,000	±10
R18	100,000	±5

CAPACITOR	VALUE (µF)	WORKING VOLTAGE (V)	CHARACTERISTICS
C1	0.1	6	
C2	22	20	Low ESR
C3	0.1	20	
C4	0.1	6	
C5	0.01	6	Non-polarized
C6	10	50	
C7	1	6	
C8	1	30	
C9	22	63	
C10	1.5E-5	3000	High voltage

OTHER COMPONENTS	SURFACE-MOUNT PART NUMBER	PACKAGE	BREAKDOWN VOLTAGE (V)	GENERIC PART NO.	MANUFACTURER
Q1	CMPTA06	SOT-23	80	MPSA06	Central Semi.
Q2	CMPT2907A	SOT-23	60	2N2907	Central Semi.
Q3	MMFT3055ELT1	SOT-23	60	3055EL	Motorola
Q4	FMMT619	SOT-23	50		Zetex
Q5	FMMT619	SOT-23	50		Zetex
D1A	CMPD4150	SOT-23	75	1N4150	Central Semi.
D1B	CMPD4150	SOT-23	75	1N4150	Central Semi.
D2A	CMPD4150	SOT-23	75	1N4150	Central Semi.
D2B	CMPD4150	SOT-23	75	1N4150	Central Semi.
D3	EC10QS05	D-64	50	1N5819	Nihon
D4	CMPD4150	SOT-23	75	1N4150	Central Semi.
D5	EC10QS02L	D-64	20	1N5817	Nihon
D6A	CMPD4150	SOT-23	75	1N4150	Central Semi.
D6B	CMPD4150	SOT-23	75	1N4150	Central Semi.
D7A	CMPD4150	SOT-23	75	1N4150	Central Semi.
D7B	CMPD4150	SOT-23	75	1N4150	Central Semi.

Note: For T1, Use Sumida EPS207. Request No. USC-145, Special No. 6358-JP5-010.

Positive LCD Bias: MAX754

The voltage-regulation loop is comprised of resistors R3 and R4, the pulse-skip comparator, the internal DAC, the on-time and off-time logic, and the external power components. The comparator compares a fraction of the output voltage to the voltage generated by an on-chip 6-bit DAC. The part regulates by keeping the voltage at LFB equal to the DAC's output voltage. Thus, you can set the output to different voltages by varying the DAC's output.

Varying the DAC output voltage (digital control) adjusts the external voltage from 50% to 100% of full scale. On power-up or after a reset, the counter sets the DAC output to mid scale. Each rising edge of LADJ (with LON high) decrements the DAC output. When decremented beyond zero scale, the counter rolls over and sets the DAC to the maximum value. In this way, a single pulse applied to LADJ decreases the DAC set point by one step, and 63 pulses increase the set point by one step.

The MAX754's DAC transfer function is shown in Figure 7. The following equation relates the switching regulator's regulated output voltage to the DAC's voltage:

$$V_{OUT} = V_{DAC}\left(1 + \frac{R3}{R4}\right)$$

Table 5 is the logic table for the LADJ and LON inputs, which control the internal DAC and counter. As long as the timing specifications for LADJ and LON are observed, any sequence of operations can be implemented.

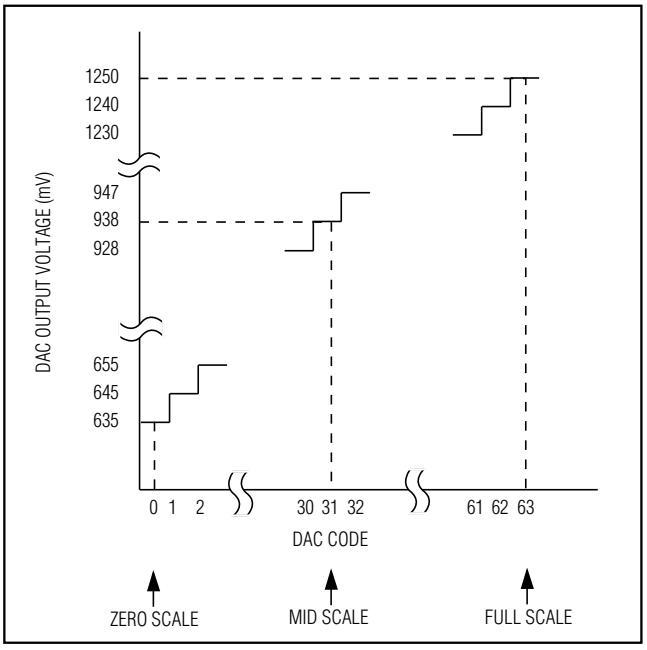

Figure 7. MAX754 LCD DAC Transfer Function

Negative LCD Bias: MAX753

The LCD bias generator of the MAX753 (Figure 8) generates its negative output by combining the switching regulator of the MAX754 with a simple diode-capacitor voltage inverter. To best understand the circuit, look at the part in a steady-state condition. Assume, for instance, that the output is being regulated to -30V, and that the battery voltage is +10V. When Q3 turns on, two things occur: current ramps up in the inductor, just like with the boost converter; and the charge on C15 (transferred from the inductor on the previous cycle) is transferred to C6, boosting the negative output. At the end of the cycle, the voltage on C15 is 30V + Vd, where Vd is the forward voltage drop of Schottky diode D3, and 30V is the magnitude of the output.

When the MOSFET turns off, the inductor's energy is transferred to capacitor C15, charging the capacitor to a positive voltage (V_{HIGH}) that is higher than $|V_{OUT}|$. In this instance, diode D8 allows current to flow from the right-hand side of the flying capacitor (C15) to ground.

When the MOSFET turns on, the left-hand side of capacitor C15 is clamped to ground, forcing the right-hand side to $-V_{HIGH}$. This voltage is more negative than the output, forcing D3 to conduct, and transferring charge from the flying capacitor C15 to the output capacitor C6. This charge transfer happens quickly, resulting in a voltage spike at the output due to the product of the output capacitor's equivalent series resistance (ESR) and the current that flows from C15 to C6. To limit this drop, resistor R19 has been placed in series with D3. R19 limits the rate of current flow. At the end of this cycle, the flying capacitor has been discharged to 30V + Vd.

If BATT(MAX) (i.e., either the fully charged battery voltage, or the wall-cube voltage) is greater than $|V_{OUT(MIN)}|$, tie the cathode of D8 to BATT instead of GND, as shown by the dashed lines in Figure 8. Efficiency is lower with this method, so tie the cathode of D8 to GND whenever possible.

The MAX753's regulation loop is similar to that of the MAX754. The MAX753, however, uses different power components, and its feedback resistors are returned to the reference (1.25V) rather than ground.

The MAX753's PFM comparator compares a fraction of the output voltage to the voltage generated by the on-chip 6-bit DAC. The part regulates by keeping the voltage at LFB equal to the DAC's output voltage. Thus, you can set the LCD bias voltage to different voltages by varying the DAC's output.

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Table 5. Logic-Signal Truth Table

CCF CONTROL					
LON	**LADJ**	**CON**	**CADJ**	**CCFT STATUS**	**CCFT DAC**
X	X	0	0	Off	Hold
X	X	0	1	On	Reset
X	X	1	0	On	Hold
X	X	1	0→1	On	Dec
LCD BIAS CONTROL					
LON	**LADJ**	**CON**	**CADJ**	**LCD STATUS**	**LCD DAC**
0	0	X	X	Off	Hold
0	1	X	X	On	Reset
1	0	X	X	On	Hold
1	0→1	X	X	On	Dec

Hold = maintain last DAC value in counter
Reset = set DAC counter to half scale
Dec = decrement DAC counter one step
Off = section turned off, sleep state
On = section turned on
X = don't care

Table 6. Component Suppliers

MANUFACTURER	ADDRESS	PHONE	FAX
Central Semiconductor	145 Adams Ave. Hauppauge, NY 11788	(516) 435-1110	(516) 435-1824
Coiltronics	6000 Park of Commerce Blvd. Boca Raton, FL 33287	(407) 241-7876	(407) 241-9339
Maxim	120 San Gabriel Dr. Sunnyvale, CA 94025	(408) 737-7600	(408) 470-5841
Nihon (NIEC)*	c/o Quantum Marketing 12900 Rolling Oaks Rd. Twin Oaks, CA 93518	(805) 867-2555	(805) 867-2698
Sumida	5999 New Wilke Rd., Suite 110 Rolling Meadows, IL 60008	(708) 956-0666	(708) 956-0702
Wima	2269 Saw Mill River Rd., Suite 400 P.O. Box 217 Elmsford, NY 10523	(914) 347-2474	(914) 347-7230
Zetex	87 Modular Ave. Commack, NY 11725	(516) 543-7100	(516) 864-7630

* Contact John D. Deith, ask for "Maxim Discount" on orders less than 5k units.

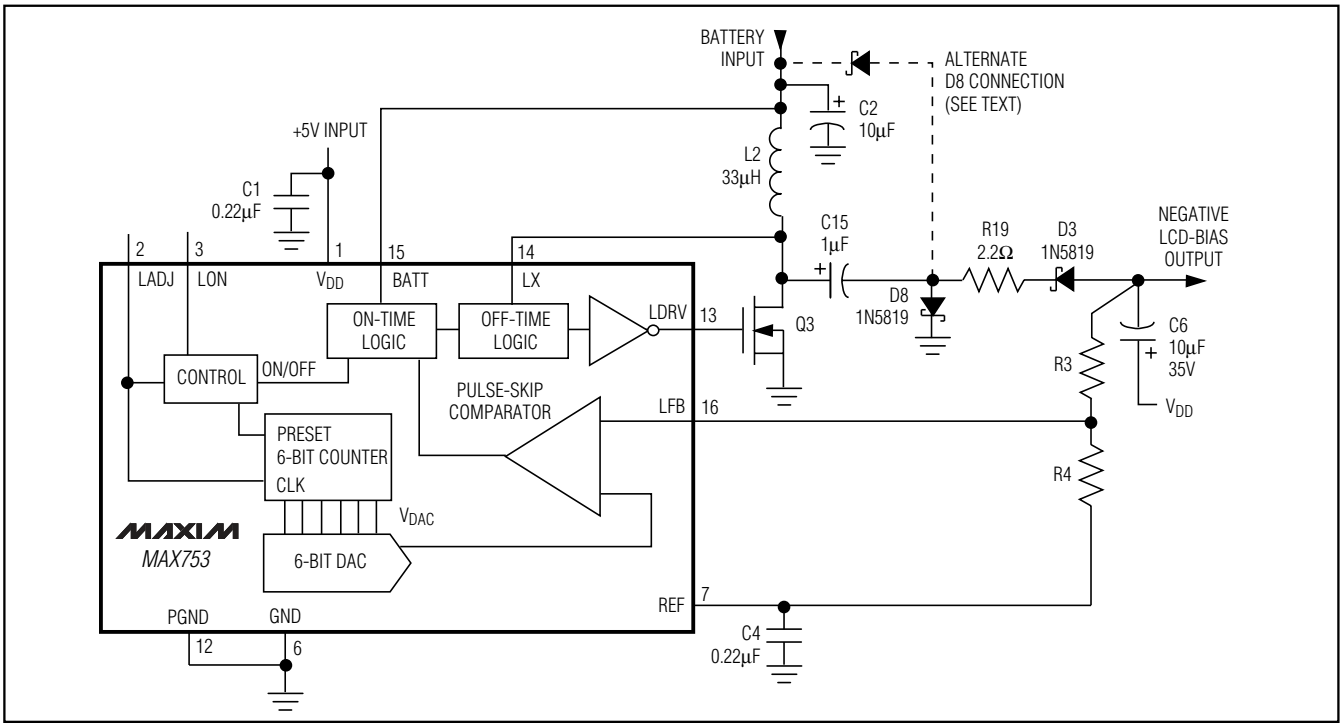

Figure 8. MAX753 Negative LCD-Bias Generator

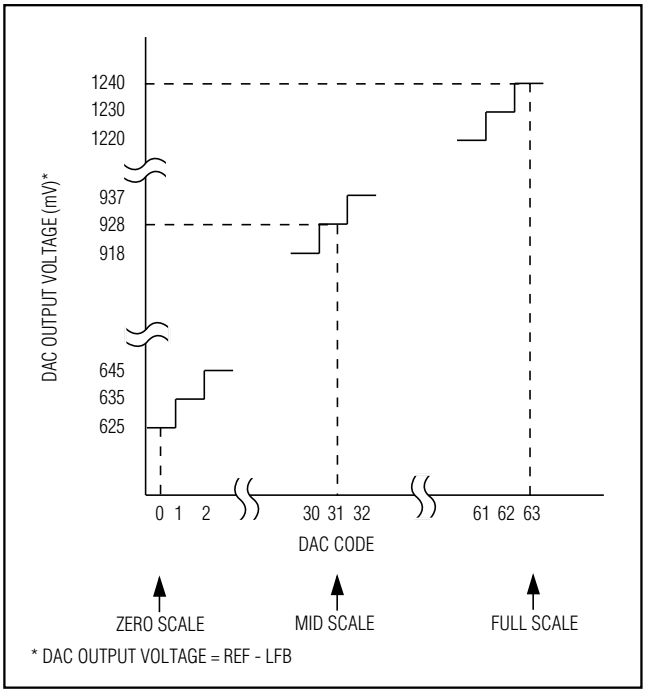

Figure 9. MAX753 LCD DAC Transfer Function

The MAX753's DAC transfer function is shown in Figure 9. The following equation relates the switching regulator's regulated output voltage to the DAC's voltage (REF - LFB):

$$V_{OUT} = REF - \left(1 + \frac{R3}{R4}\right)(REF - LFB)$$

The value REF - LFB (and not LFB) is specified in the *Electrical Characteristics*. The most negative output voltage occurs for the largest value of REF - LFB.

The MAX753's combination boost converter and charge-pump inverter was chosen over a conventional buck-boost inverter because it allows the use of low-cost N-channel MOSFETs instead of more expensive P-channel ones. Additionally, its efficiency is 5% to 10% better than a standard buck-boost inverter.

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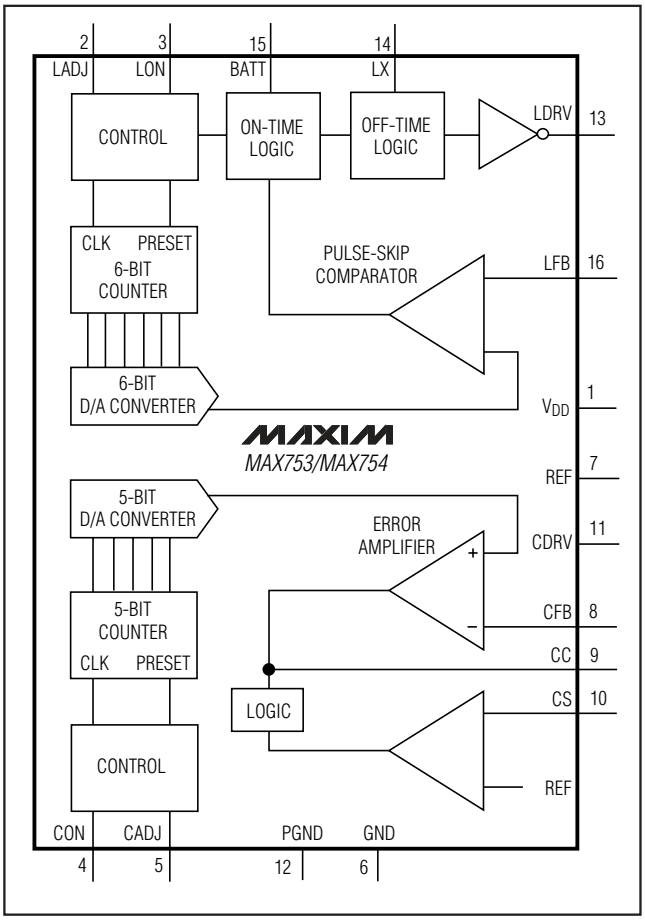
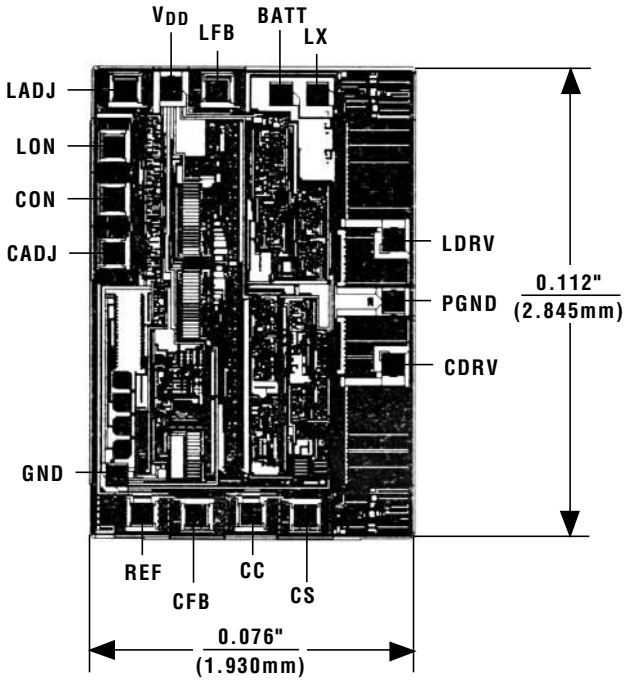
Block Diagram



Chip Topography



TRANSISTOR COUNT: 321;
SUBSTRATE CONNECTED TO V_{DD}.

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