# MJL21195 (PNP), MJL21196 (NPN)

# Silicon Power Transistors

The MJL21195 and MJL21196 utilize Perforated Emitter technology and are specifically designed for high power audio output, disk head positioners and linear applications.

**Features**

- Total Harmonic Distortion Characterized
- High DC Current Gain
- Excellent Gain Linearity
- High SOA
- Epoxy Meets UL 94, V−0 @ 0.125 in
- These Devices are Pb−Free and are RoHS Compliant*

**MAXIMUM RATINGS**

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Collector−Emitter Voltage | $V_{CEO}$ | 250 | Vdc |
| Collector−Base Voltage | $V_{CBO}$ | 400 | Vdc |
| Emitter−Base Voltage | $V_{EBO}$ | 5 | Vdc |
| Collector−Emitter Voltage − 1.5 V | $V_{CEX}$ | 400 | Vdc |
| Collector Current − Continuous | $I_C$ | 16 | Adc |
| Collector Current − Peak (Note 1) | $I_{CM}$ | 30 | Adc |
| Base Current − Continuous | $I_B$ | 5 | Adc |
| Total Power Dissipation<br>@ $T_C$ = 25°C<br>Derate Above 25°C | $P_D$ | <br>200<br>1.43 | <br>W<br>W/°C |
| Operating and Storage Junction Temperature Range | $T_J$, $T_{stg}$ | − 65 to +150 | °C |
| ESD − Human Body Model | HBM | 3B | V |
| ESD − Machine Model | MM | C | V |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Pulse Test: Pulse Width = 5.0 μs, Duty Cycle ≤10%.

**THERMAL CHARACTERISTICS**

| Characteristic | Symbol | Max | Unit |
|---|---|---|---|
| Thermal Resistance, Junction−to−Case | $R_{\theta JC}$ | 0.7 | °C/W |

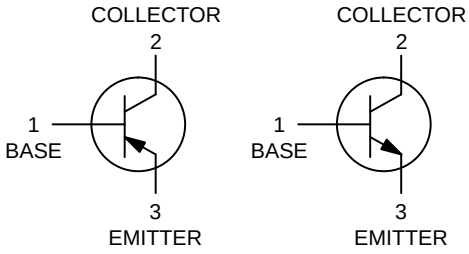
*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

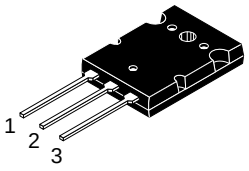
**ON Semiconductor®**

**http://onsemi.com**

## 16 A COMPLEMENTARY SILICON POWER TRANSISTORS 250 V, 200 W

**COMPLEMENTARY**




**TO−264**
**CASE 340G**
**STYLE 2**

**MARKING DIAGRAM**


x = 5 or 6
A = Assembly Location
YY = Year
WW = Work Week
G = Pb−Free Package

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MJL21195G | TO−264 (Pb−Free) | 25 Units / Rail |
| MJL21196G | TO−264 (Pb−Free) | 25 Units / Rail |

**ELECTRICAL CHARACTERISTICS** ($T_C$ = 25°C unless otherwise noted)

| Characteristic | Symbol | Min | Typical | Max | Unit |
|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** (Note 2) | | | | | |
| Collector−Emitter Sustaining Voltage ($I_C$ = 100 mAdc, $I_B$ = 0) | $V_{CEO(sus)}$ | 250 | – | – | Vdc |
| Collector Cutoff Current ($V_{CE}$ = 200 Vdc, $I_B$ = 0) | $I_{CEO}$ | – | – | 100 | μAdc |
| **OFF CHARACTERISTICS** (Note 3) | | | | | |
| Emitter Cutoff Current ($V_{CE}$ = 5 Vdc, $I_C$ = 0) | $I_{EBO}$ | – | – | 100 | μAdc |
| Collector Cutoff Current ($V_{CE}$ = 250 Vdc, $V_{BE(off)}$ = 1.5 Vdc) | $I_{CEX}$ | – | – | 100 | μAdc |
| **SECOND BREAKDOWN** (Note 3) | | | | | |
| Second Breakdown Collector Current with Base Forward Biased<br>($V_{CE}$ = 50 Vdc, t = 1 s (Nonrepetitive))<br>($V_{CE}$ = 80 Vdc, t = 1 s (Nonrepetitive)) | $I_{S/b}$ | <br>4.0<br>2.25 | <br>–<br>– | <br>–<br>– | Adc |
| **ON CHARACTERISTICS** (Note 3) | | | | | |
| DC Current Gain<br>($I_C$ = 8 Adc, $V_{CE}$ = 5 Vdc)<br>($I_C$ = 16 Adc, $I_B$ = 5 Adc) | $h_{FE}$ | <br>25<br>8.0 | <br>–<br>– | <br>100<br>– | – |
| Base−Emitter On Voltage ($I_C$ = 8 Adc, $V_{CE}$ = 5 Vdc) | $V_{BE(on)}$ | – | – | 2.2 | Vdc |
| Collector−Emitter Saturation Voltage<br>($I_C$ = 8 Adc, $I_B$ = 0.8 Adc)<br>($I_C$ = 16 Adc, $I_B$ = 3.2 Adc) | $V_{CE(sat)}$ | <br>–<br>– | <br>–<br>– | <br>1.4<br>4 | Vdc |
| **DYNAMIC CHARACTERISTICS** (Note 3) | | | | | |
| Total Harmonic Distortion at the Output<br>($V_{RMS}$ = 28.3 V, f = 1 kHz, $P_{LOAD}$ = 100 $W_{RMS}$)<br>$h_{FE}$ unmatched<br>(Matched pair $h_{FE}$ = 50 @ 5 A/5 V)<br>$h_{FE}$ matched | $T_{HD}$ | <br>–<br><br>– | <br>0.8<br><br>0.08 | <br>–<br><br>– | % |
| Current Gain Bandwidth Product ($I_C$ = 1 Adc, $V_{CE}$ = 10 Vdc, $f_{test}$ = 1 MHz) | $f_T$ | 4 | – | – | MHz |
| Output Capacitance ($V_{CB}$ = 10 Vdc, $I_E$ = 0, $f_{test}$ = 1 MHz) | $C_{ob}$ | – | – | 500 | pF |

2. Pulse Test: Pulse Width = 5.0 μs, Duty Cycle ≤10%.
3. Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤2%.

**PNP MJL21195**

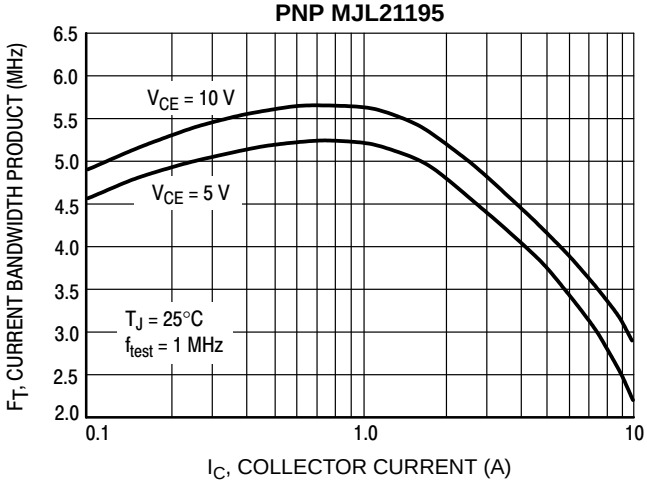



**Figure 1. Typical Current Gain Bandwidth Product**

**NPN MJL21196**

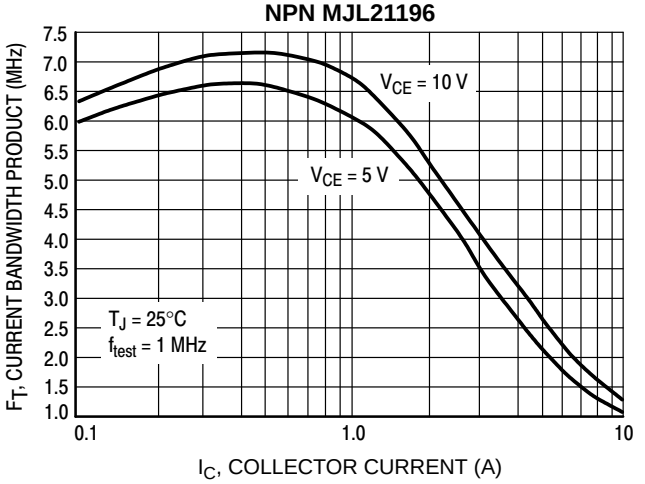



**Figure 2. Typical Current Gain Bandwidth Product**

## TYPICAL CHARACTERISTICS

**PNP MJL21195**

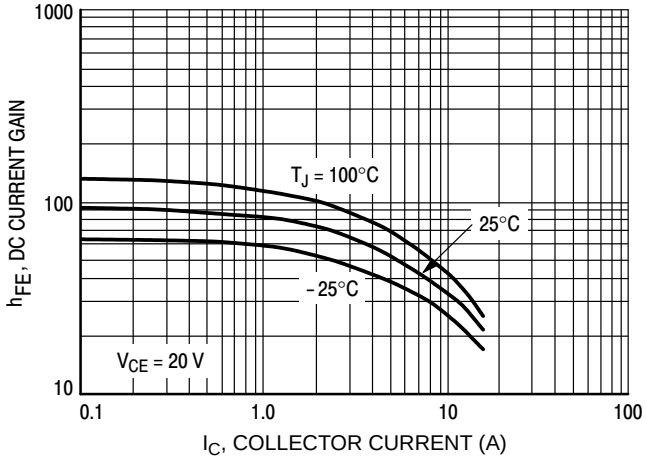



**Figure 3. DC Current Gain, $V_{CE}$ = 20 V**

**NPN MJL21196**

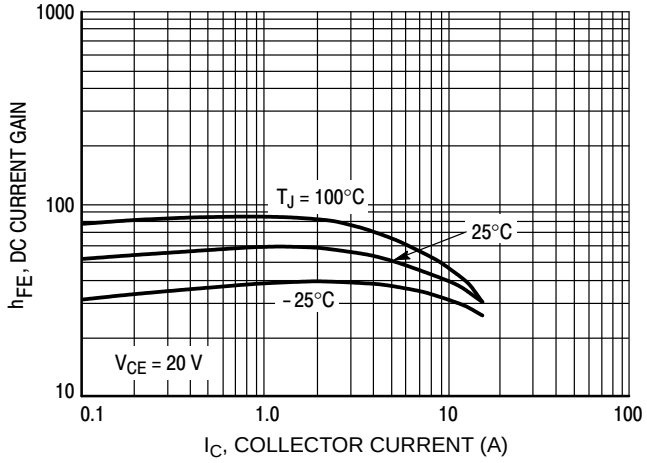



**Figure 4. DC Current Gain, $V_{CE}$ = 20 V**

**PNP MJL21195**

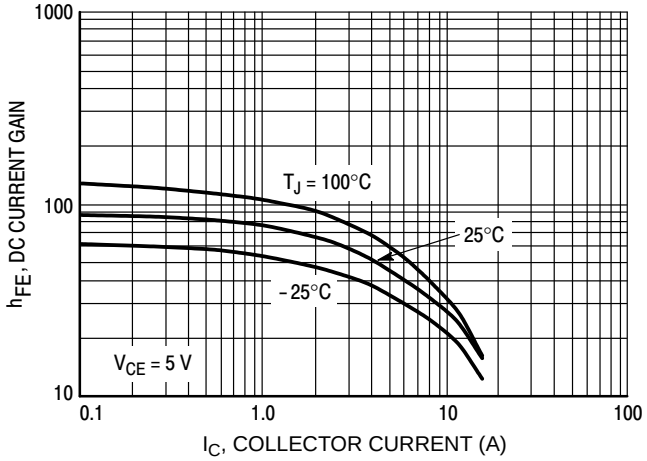



**Figure 5. DC Current Gain, $V_{CE}$ = 5 V**

**NPN MJL21196**

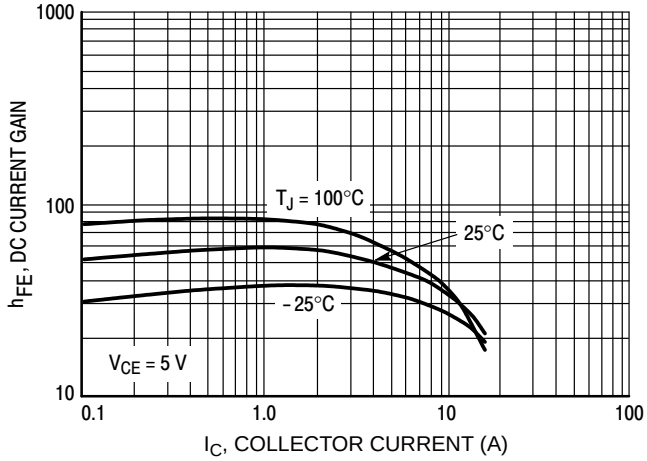



**Figure 6. DC Current Gain, $V_{CE}$ = 5 V**

**PNP MJL21195**

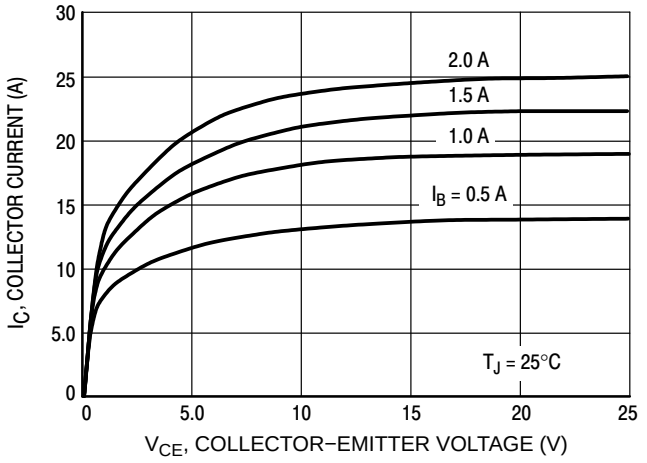



**Figure 7. Typical Output Characteristics**

**NPN MJL21196**

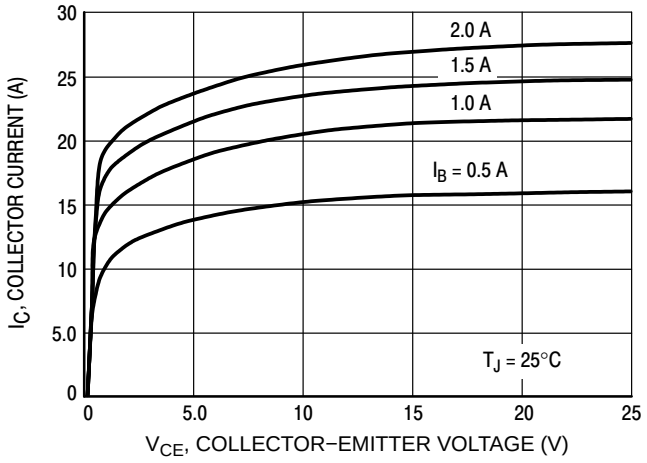



**Figure 8. Typical Output Characteristics**

## TYPICAL CHARACTERISTICS

**PNP MJL21195**

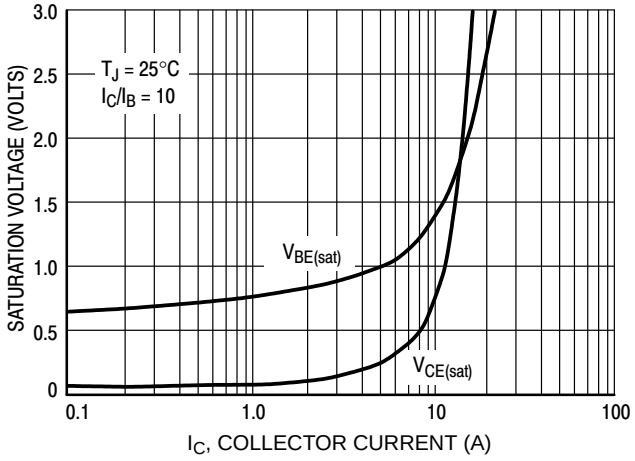



**Figure 9. Typical Saturation Voltages**

**NPN MJL21196**

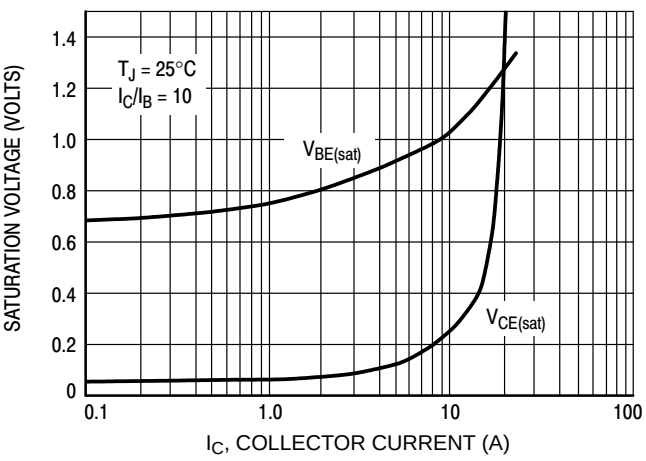



**Figure 10. Typical Saturation Voltages**

**PNP MJL21195**

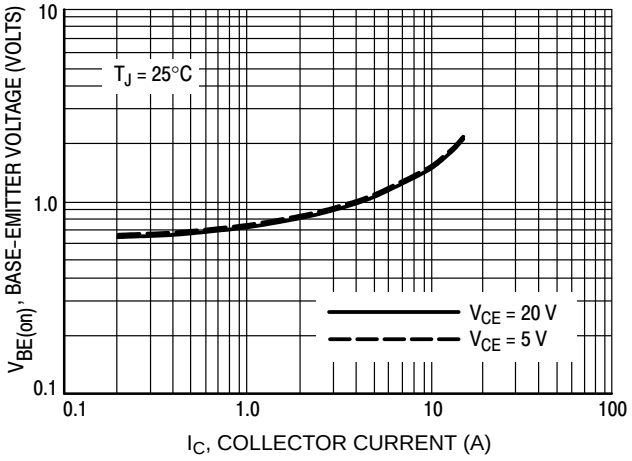



**Figure 11. Typical Base−Emitter Voltage**

**NPN MJL21196**

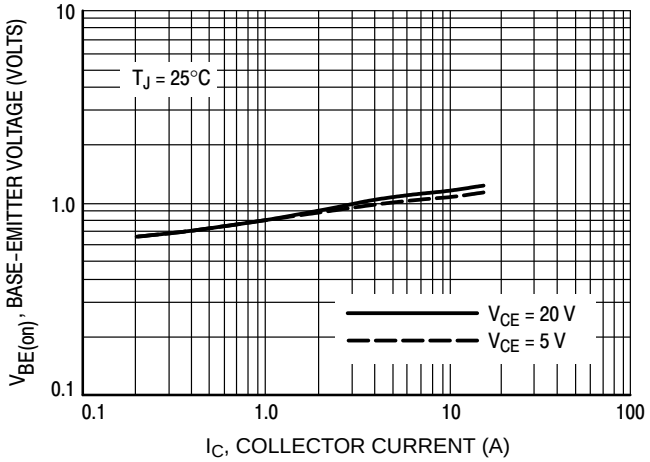



**Figure 12. Typical Base−Emitter Voltage**

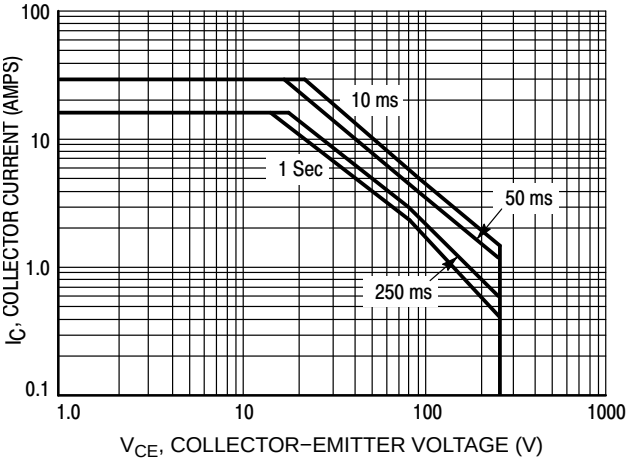



**Figure 13. Active Region Safe Operating Area**

There are two limitations on the power handling ability of a transistor; average junction temperature and secondary breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 13 is based on $T_{J(pk)}$ = 150°C; $T_C$ is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power than can be handled to values less than the limitations imposed by second breakdown.

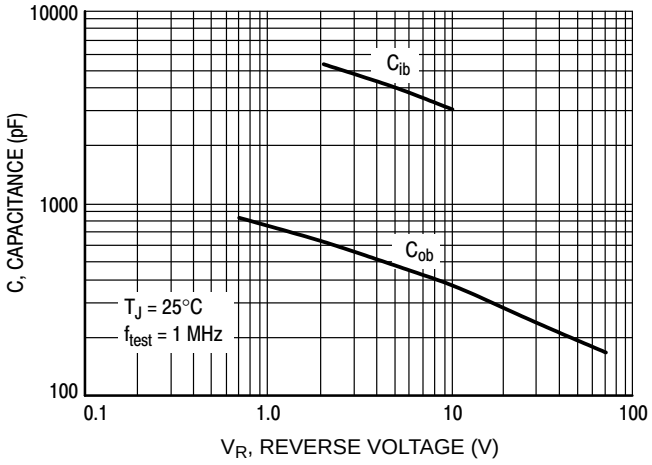



**Figure 14. MJL21195 Typical Capacitance**

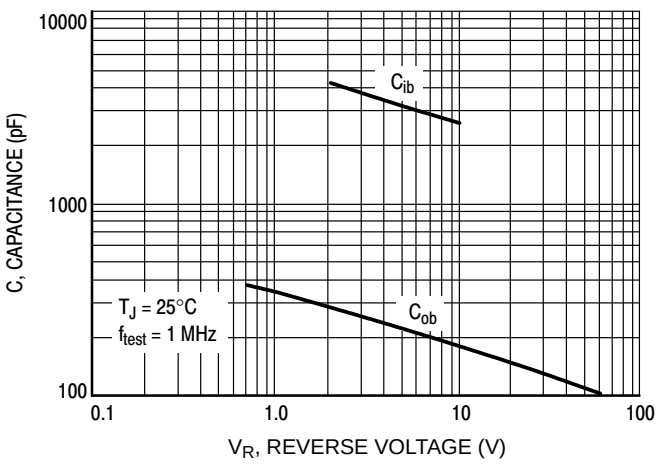



**Figure 15. MJL21196 Typical Capacitance**

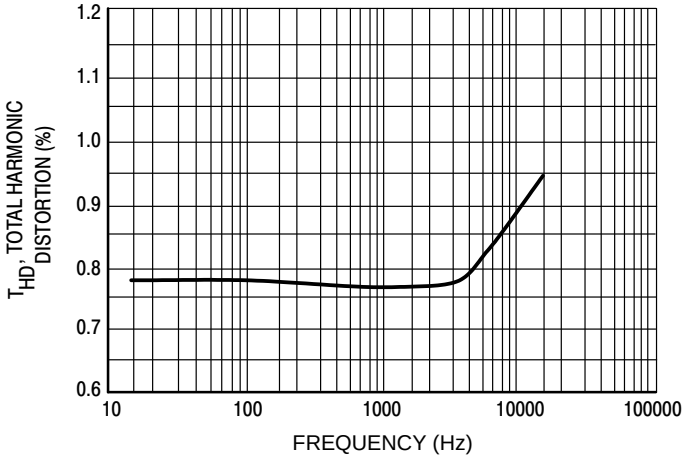



**Figure 16. Typical Total Harmonic Distortion**

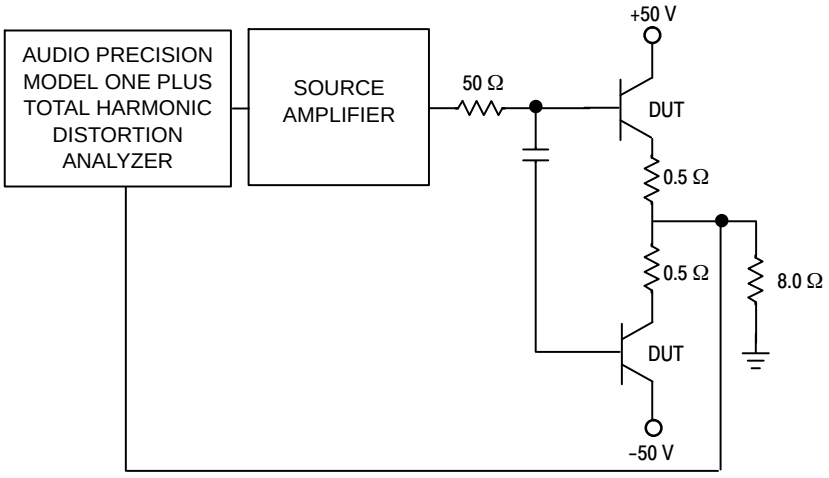
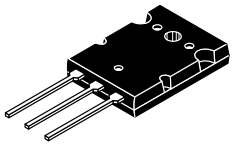



**Figure 17. Total Harmonic Distortion Test Circuit**

# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS

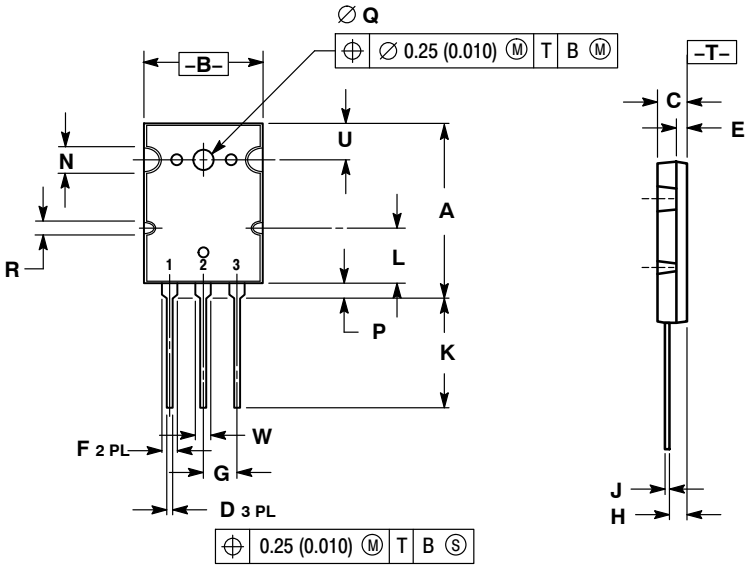
ON Semiconductor®



**TO−3BPL (TO−264)**
CASE 340G−02
ISSUE J

DATE 17 DEC 2004

**SCALE 1:2**




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 28.0 | 29.0 | 1.102 | 1.142 |
| B | 19.3 | 20.3 | 0.760 | 0.800 |
| C | 4.7 | 5.3 | 0.185 | 0.209 |
| D | 0.93 | 1.48 | 0.037 | 0.058 |
| E | 1.9 | 2.1 | 0.075 | 0.083 |
| F | 2.2 | 2.4 | 0.087 | 0.102 |
| G | 5.45 BSC | | 0.215 BSC | |
| H | 2.6 | 3.0 | 0.102 | 0.118 |
| J | 0.43 | 0.78 | 0.017 | 0.031 |
| K | 17.6 | 18.8 | 0.693 | 0.740 |
| L | 11.2 REF | | 0.411 REF | |
| N | 4.35 REF | | 0.172 REF | |
| P | 2.2 | 2.6 | 0.087 | 0.102 |
| Q | 3.1 | 3.5 | 0.122 | 0.137 |
| R | 2.25 REF | | 0.089 REF | |
| U | 6.3 REF | | 0.248 REF | |
| W | 2.8 | 3.2 | 0.110 | 0.125 |

STYLE 1:
PIN 1. GATE
2. DRAIN
3. SOURCE

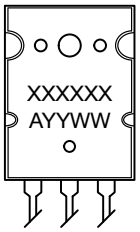
STYLE 2:
PIN 1. BASE
2. COLLECTOR
3. EMITTER

STYLE 3:
PIN 1. GATE
2. SOURCE
3. DRAIN

STYLE 4:
PIN 1. DRAIN
2. SOURCE
3. GATE

STYLE 5:
PIN 1. GATE
2. COLLECTOR
3. EMITTER

### GENERIC MARKING DIAGRAM*




XXXXXX = Specific Device Code
A = Location Code
YY = Year
WW = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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|---|---|---|
| DESCRIPTION: | TO−3BPL (TO−264) | PAGE 1 OF 1 |

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