ADS42B4x EVM

This is the user's guide for the ADS42B4x EVM (Revision A). The ADS42B49 (dual-channel, 14-bit, up to 250 MSPS) is a dual analog-to-digital converter family. This EVM is specifically suited for interfacing with TI's TSW1400 EVM to capture and display waveforms from the ADC. The EVM schematic, Bill of Materials (BOM), and layout files are found in the design package in the ADS42B4x EVM product folder on www.ti.com.

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1 Software Control

1.1 Installation Instructions

- Open folder named: ADS42Bxx_Installer_vxpx (where xpx represents the latest version)
- Double-click: **setup.exe**
- Follow on-screen instructions to complete GUI installation
  - Wait for *ADS42Bxx_Installer* initializing screen to complete
  - Click *Next* to install files in the default destination directory
  - Select *I accept the License Agreement* and click *Next*
  - Select *Next* on the summary page
  - Wait for files to load and then click *Next*
  - Once all files are installed, click *Next*
- If Windows® Logo Message window appears, click *Continue Anyway*.
- Once installed, launch by clicking on the ADS42Bxx_GUI_vxpx program in Start→Texas Instruments ADCs
- When plugging in the USB cable for the first time, you are prompted to install the USB drivers
  - On the *Welcome to the Found New Hardware Wizard* window select *No, not at this time*
  - Select **Install the software automatically** button on the next window
  - Select *Continue Anyway* on the Windows Logo Message window
  - If the computer cannot find the drivers automatically, access them directly in the install directory: C:\Program Files (x86)\Texas Instruments ADCs\ADS42Bxx GUI
  - Click *Finish* once completed

1.2 Software Operation

The software allows full programming control of the ADC device. Figure 1 shows the GUI front panel that has register tabs. The GUI tab provides an interface to the most-used registers.

1.2.1 Top Level

Figure 1 shows the top level tab of the register user interface. Below is a brief explanation of the controls. Please refer to the ADS42B49 datasheet for more detailed explanations of the register functions as needed.

- Reset: Device reset, clicking this switch resets the device
- Powerdown Global: Clicking the Device power down switch on powers down the device
- Data format: Clicking the Device output data format, sets the 2's complement or offset binary format. High Speed Data Converter Pro expects offset binary.
- Output Buffer Selection: Select this box for LVDS or CMOS output format
- Gain ChA: Set this box for gain of channel A. Must enable digital functions first.
- Gain ChB: Set this box for gain of channel B. Must enable digital functions first.
- Test Pattern ChA: Select device test pattern for channel A. Must enable digital functions first.
- Test Pattern ChB: Select device test pattern for channel B. Must enable digital functions first.
- HP[0] High-performance mode bit 0 - set for CMOS outputs
- HP[1:11] High-performance mode bits 1 to 11. Always set this control.
- Digital Function Enable Set this bit to control digital functions, such as gain and test patterns.
- Low Speed Mode En: Low-Speed Mode Enable or Disable
- Low Speed Mode ChA: Low-speed mode for channel A

- Low Speed Mode ChB: Low-speed mode for channel B
- LVDS Data Strength: Set the data strength from this switch
- LVDS Clkout Strength: Set the output clock strength from this switch
- CMOS Clk Strength: Set CMOS output clock strength from this switch
- ClkOut Delay: Programming the delay of CLKOUT
- Offset Correction: Enables or Disables offset correction
- ChA Offset Pedestal: Programming Channel A for different offset pedestals
- ChB Offset Pedestal: Programming Channel B for different offset pedestals

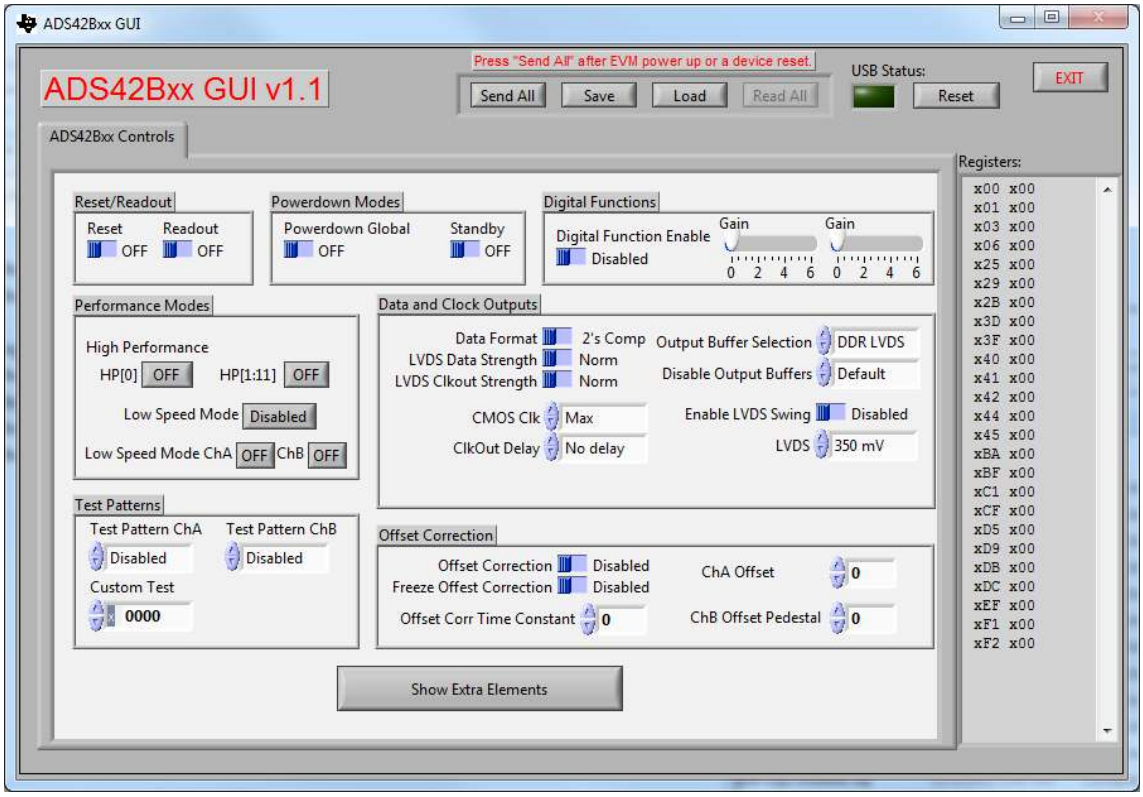

Figure 1. ADS42Bxx_GUI Front Panel – Top Level

1.2.2 Register Control

- Send All: Sends all the register configurations on the panel to the device
- Read All: Not active
- Save: Saves the register configuration to text file
- Load: Loads a register file from a text file. After loading registers, the relative switches and selecting boxes are automatically updated.
  - Select *Load* button
  - Double click on the desired register file
  - Click *Send All* to ensure all of the values are loaded properly

1.2.3 Miscellaneous Settings

- Reset USB: Toggle this button if the USB port is not responding. This generates a new USB handle address. After hitting this, USB Status has to be turned to “Green”.
- Exit: Stops the program

2 Basic Test Procedure

This section outlines the basic test procedure for testing the EVM. Figure 2 shows how to connect the ADS42B4xEVM to TSW1400.

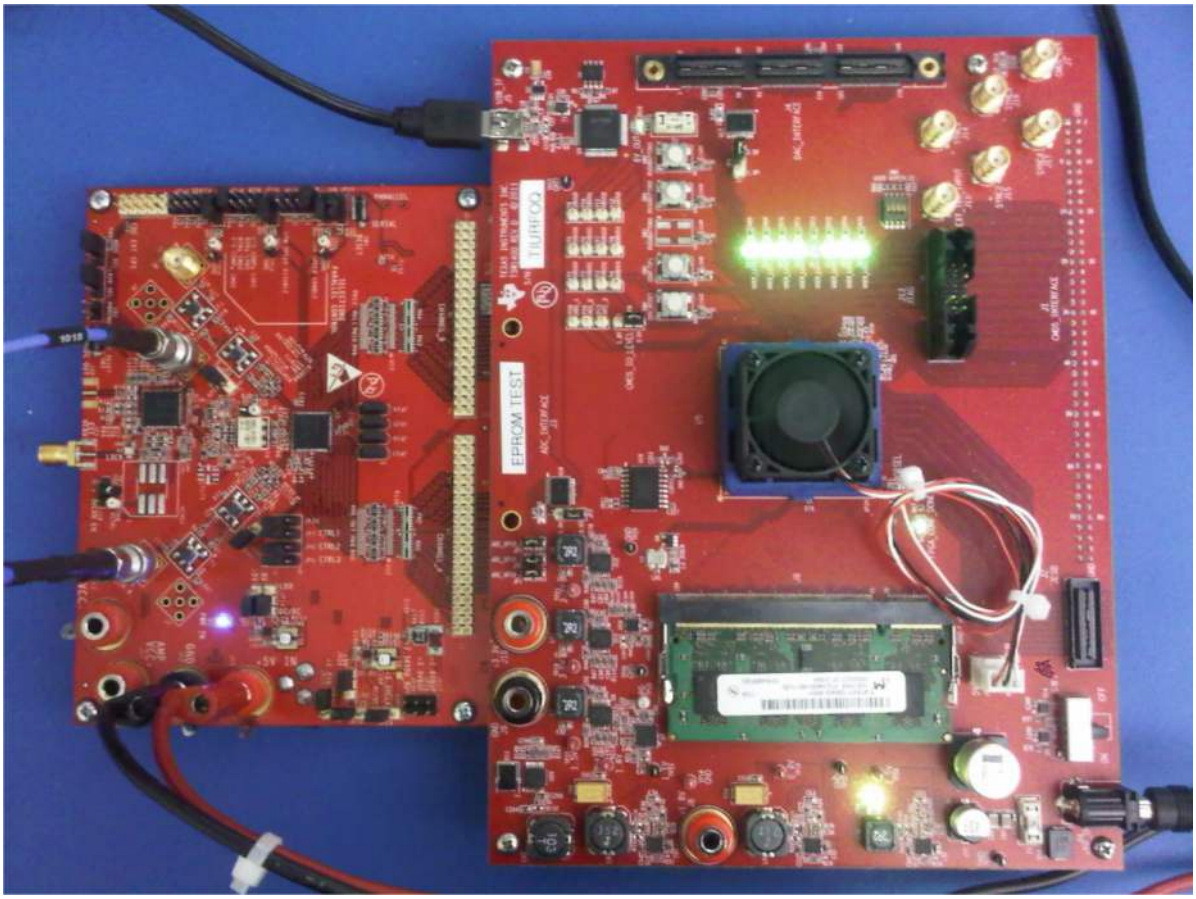

Figure 2. ADS42B4xEVM and TSW1400

2.1 Test Block Diagram

The test set-up for general testing of the ADS42B4x EVM with the TSW1400 capture card is shown in Figure 3.

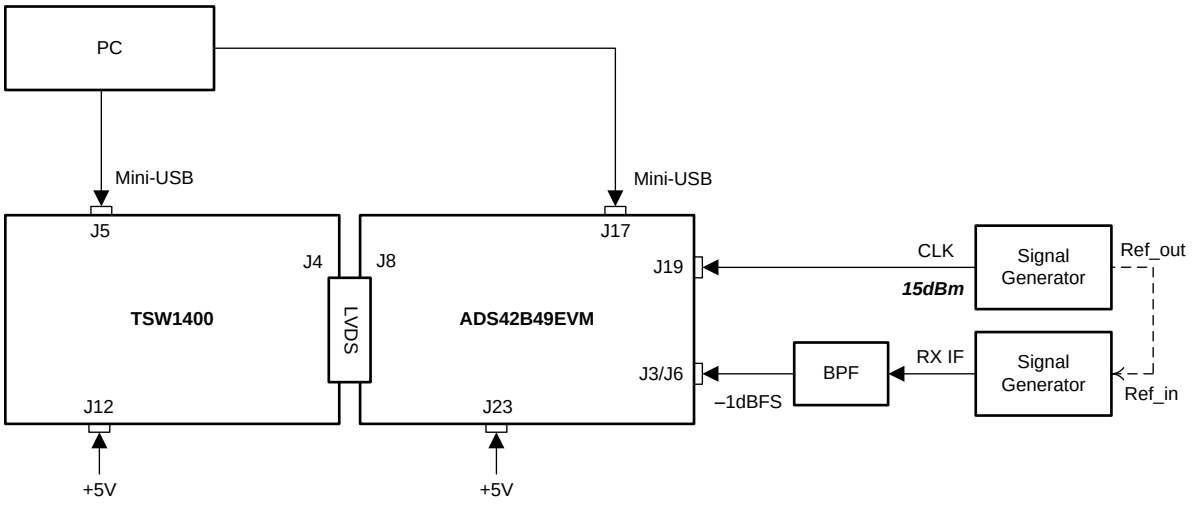

Figure 3. Test Set-Up Block Diagram

2.2 Verify Board Set-up

Verify jumper settings are in the correct position as outlined in Table 1 and Table 2. Parallel configuration is not recommended because the high performance modes cannot be enabled. The high performance modes are required to achieve best performance.

Table 1. Default ADS42Bxx EVM Revision A Jumper Setting for Serial Interface

Jumper	Default position	Function
JP15	Short 1 - 2	DC supply for +1.8VA
JP16	Short 1 - 2	DC supply for +1.8VD
JP17	Short 3 - 2	DC supply, LDO for +5V
JP19	Short 3 - 2	DC supply, LDO for +1.8V
JP28	Short 3 - 2	DC supply, LDO for +5V
JP29	Short 3 - 2	DC supply, LDO for +3.3VCLK
JP26	Open	DC supply for ext buffer
JP27	Open	DC supply for ext buffer
JP3	Short 2 - 3	OPA power down
JP4	Short 2 - 3	OPA power down
JP22	Open	SDOUT to FPGA
JP20	Short 1 - 2	CDC
JP21	Short 1 - 2	CDC
J14	Short 1 - 2	CDC power down
J18	Open	CDC, VCXO
JP8 (1)	Short 3 - 2	ADC SCLK for SPI
JP9	Short 3 - 2	ADC SDATA for SPI
JP10	Short 3 - 2	ADC SEN for SPI
JP11	Short 3 - 2	ADC for SPI, also reset
JP 12	Short 1 - 2	ADC Low speed mode disable
JP 13	Open	

(1) The EVM schematic shows default setting of JP8 to JP11 as parallel interface Table 2) which is for EVM installation. After EVM tested and released these jumpers are set as serial interface (Table 1).

Table 1. Default ADS42Bxx EVM Revision A Jumper Setting for Serial Interface (continued)

Jumper	Default position	Function
JP14	Short 7 - 8	ADC 2's complement, DDR LVDS
JP5	Short 1 - 2	ADC CTRL3, normal operation
JP6	Short 1 - 2	ADC CTRL2, normal operation
JP7	Short 1 - 2	ADC CTRL1, normal operation
JP 18	Short 1 - 2	Ext Buffer
JP 23	Short 1 - 2	Ext Buffer
JP 24	Short 1 - 2	Ext Buffer
JP 25	Short 1 - 2	Ext Buffer
JP30	Short	ADC buffer 3.3-V supply

Table 2. Parallel Interface with Pin Control of ADS58C28 and ADS42Bxx EVM Revision B Jumper Setting

Jumper	Position	Function
JP8	Short 1 - 2	ADC SCLK for parallel control
JP9	Short 1 - 2	ADC SDATA for parallel control
JP10	Short 1 - 2	ADC SEN for parallel control
JP11	Short 1 - 2	ADC parallel control

2.3 Test Set-Up Connections

- Connect the ADS42B4x EVM to TSW1400 EVM
- Connect 5-V power to banana jack at J10; connect ground to J12
- Connect USB cable to programming computer at J17
- Connect USB and power supply jack to TSW1400
- Connect the clock signal through the appropriate BPF to J19
- Connect the input signal through the appropriate BPF to J6/J3

2.4 TSW1400 Quick Start Operation

Reference the TSW1400 User's Guide for more detailed explanation of the TSW1400 set-up and operation. This document assumes that High Speed Data Converter Pro (HSDCPro) is installed and functioning properly. The front panel of HSDCPro is shown in Figure 4. The following configuration needs to be changed from the default settings. Note that HSDCPro version 3.1 or newer is required to properly run the ADS42B4x EVM.

- Select the ADS42B4x device name from the TI ADC Selection pull-down menu
- Select Single Tone for FFT from the Test pull-down menu
- Select the desired channel (that is, Channel A or B) from the Channel Display pull-down menu
- Check the box for *Auto Calculation of Coherent Frequencies.*
- Change the ADC sampling rate to the desired value (that is, 250 MHz)
- Change the input frequency to desired value (that is, 170 MHz or other)
- Verify status display in the lower left has no errors
- Press the **Capture** button to initiate a data capture. The ADS42B4x EVM must be configured before a capture can be made.

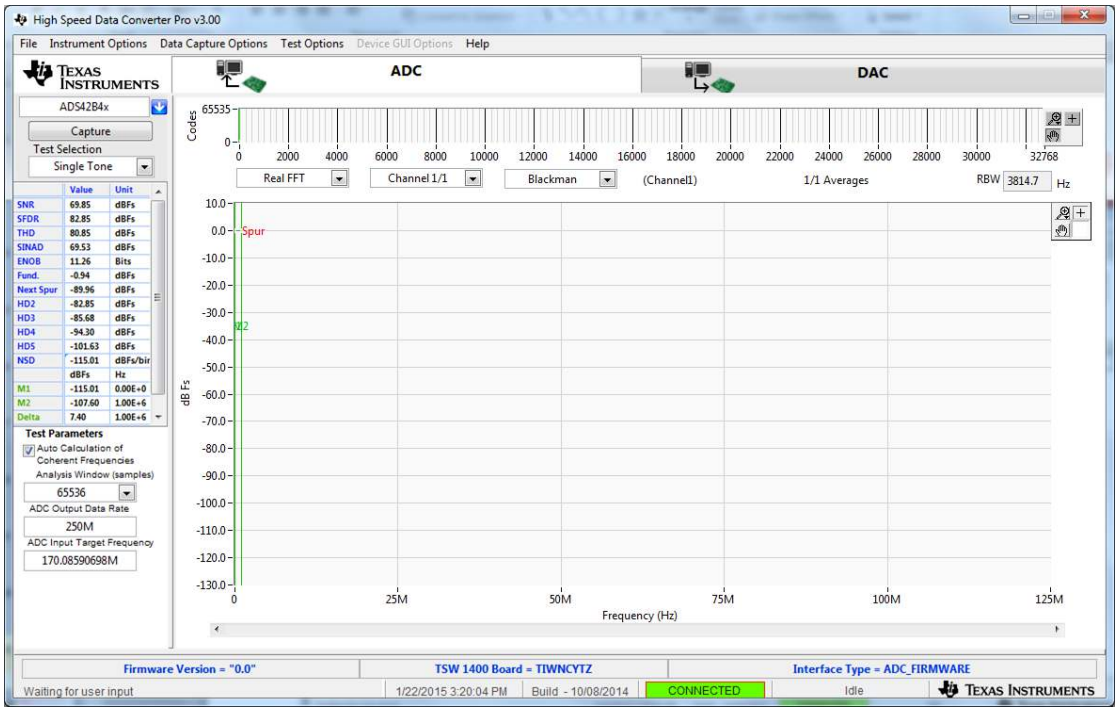

Figure 4. High Speed Data Converter Pro

2.5 ADS42B4x Test Procedure

- Switch on the 5-V power supply for the EVM.
- Connect clock signal at J19 through an appropriate bandpass filter.
  - Set the signal generator to 10 dBm and 250 MHz.
  - Use a high-quality, low phase-noise generator for this input to ensure proper device evaluation.
  - A tight bandpass filter is required to achieve optimal performance.
- Connect the input signal through an appropriate bandpass filter at either J6 or J3 (Channel A or B).
  - Adjust the frequency of the generator to match the coherent frequency displayed in HSDCPro.
  - Select the proper Display Channel in HSDCPro, corresponding to the input connection.
  - Use a high-quality, low phase-noise generator for this input to ensure proper device evaluation.
  - A tight bandpass filter is required to achieve optimal performance.
- Open the ADS42B4x GUI by going to the *Start Menu* and finding *ADS42B4x GUI* in the Texas Instruments folder.
  - Press the *Reset* button.
  - Press the *Data Format* button to choose "Offset Bin"
  - Turn on HP[1:11] to enable the high performance modes.
  - Click *Send All*, see Figure 5.
- Initiate a capture by pressing the **Capture** button in HSDCPro.

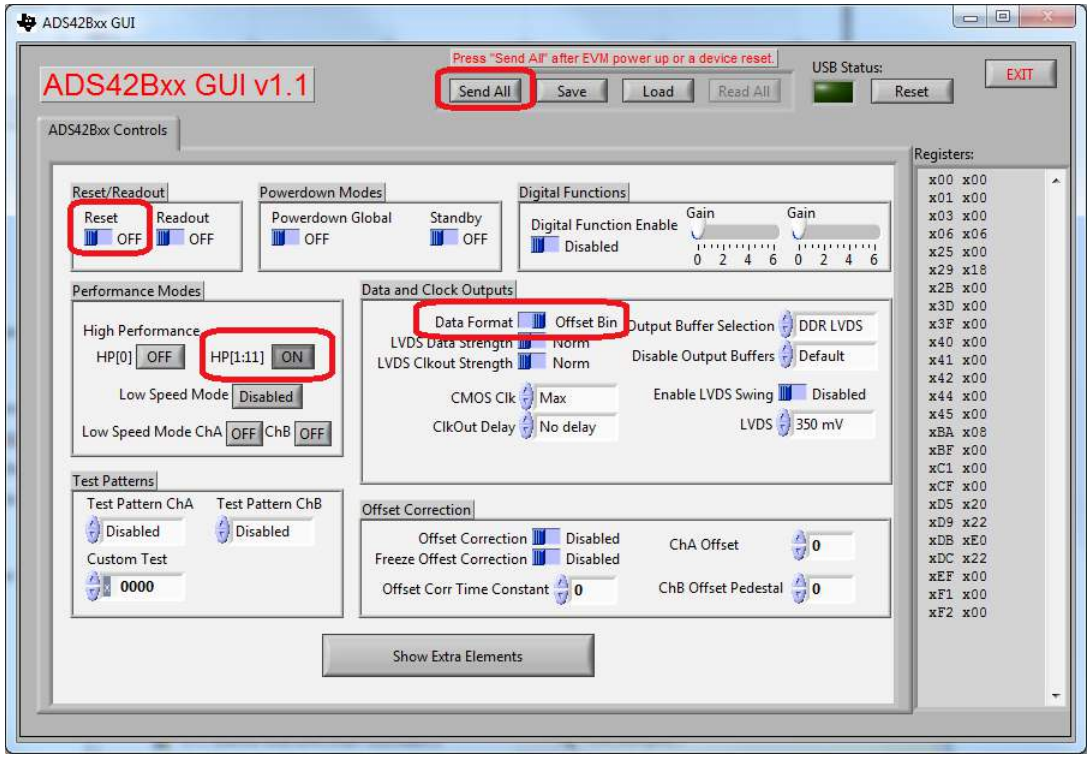

Figure 5. ADS42Bxx GUI

2.6 ADS42B4x Performance Results

Figure 6 shows the performance result at 250-MSPS clock frequency and with a 170-MHz input tone. Figure 6 shows the performance of channel A from ADS42B4xEVM. SNR is 69.85 dBFS and SFDR is 82.85 dBFS.

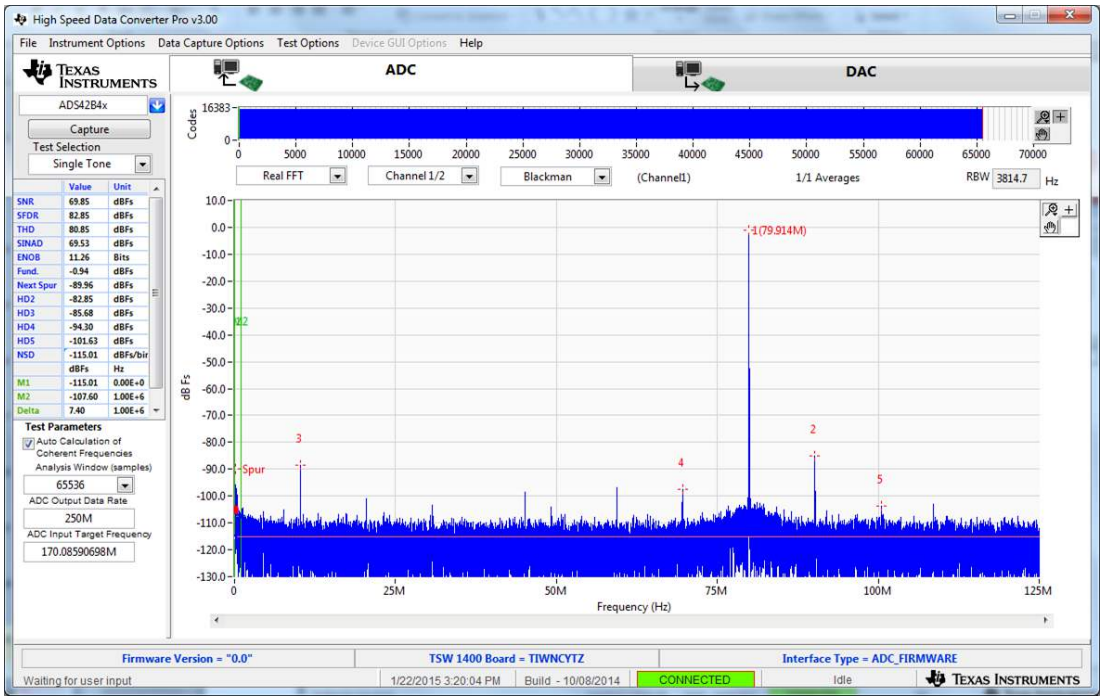

Figure 6. FFT Plot: 250-MHz clock, 170-MHz Input to Channel A

Figure 7 shows the performance of channel B from ADS42B4xEVM. SNR is 69.94 dBFS and SFDR is 84.77 dBFS.

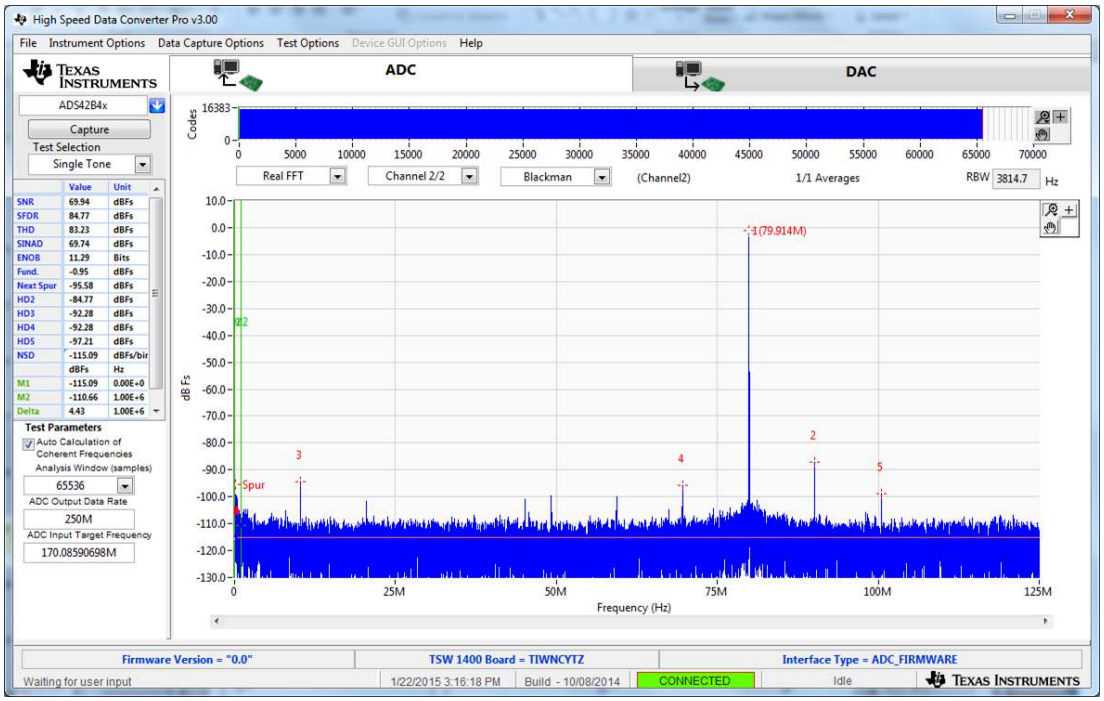

Figure 7. FFT Plot: 250-MHz clock, 170-MHz Input to Channel B

3 Optional Configurations

3.1 THS4509 Input Op-Amp Configuration

The default analog input configuration is transformer coupling through T1 and T2 for channel A, and T3 and T4 for channel B. The optional configuration for analog input is through an Op-Amp THS4509. The changes required to modify the transformer coupled input to the OPA-driven input are shown in Table 3.

Table 3. Jumper Setting for Transformer-coupled or OPA-driven Input

Jumpers or 0 Ω	Transformer-coupled input (default)	OPA-driven input
R119	Install	Do not install
R123	Install	Do not install
R120	Do not install	install
R129	Do not install	install
R143	Install	Do not install
R141	Install	Do not install
R131	Do not install	Install
R132	Do not install	Install
R93	Install	Do not install
R94	Install	Do not install
R95	Do not install	Install
R96	Do not install	Install
R97	Install	Do not install
R98	Install	Do not install
R99	Do not install	Install
R114	Do not install	Install
SJP3	Shunt 2 - 3, default	Shunt 1-2
SJP4	Shunt 2 - 3, default	Shunt 1-2

J11 and J13 are the power supply for the THS4509. An on-board layout option for a LPF or BPF is available between the amplifier and the ADC. By default the filter is bypassed, allowing the flexibility to design according to desired specifications.

3.2 On-Board CDCE72010 Clock

The default clock input configuration is 1:4 transformer coupling through T6. The optional configuration is through clock driver CDCE72010. The changes required to modify the transformer coupled clock input to clock driver input are shown in Table 4.

Table 4. Jumper Setting for Transformer-Coupled or CDCE72010 Input

Jumper	Transformer-coupled (Default)	CDCE72010
J14	shunt	open
JP20	Shunt 1-2	Shunt 1-2
JP21	Shunt 1-2	Shunt 1-2
J18	open	open
R121	0 Ω	DNI
R122	DNI	0 Ω
SJP7	Short 1-2	Short 3-4
SJP6	Short 3-4	Short 5-6

The on-board layout is available for the option of VCXO and crystal BPF. The CDCE72010 comes with a default configuration (please see CDCE72010 data sheet for details about device default configuration). With a 10-MHz primary reference at J19 and a 983.04-MHz VCXO on-board the CDC outputs a LVCMOS clock at U0P (pin7) at 245.76 MHz. With a 491.52-MHz VCXO the CDC outputs a LVCMOS clock at U0P at 122.88 MHz. The clock goes through an on-board crystal BPF (Y0) and is used as the input clock to the ADC through SJP6.

3.3 Parallel CMOS Output

The default ADC output is configured as DDR LVDS output on the EVM. The layout provides an option of 1.8-V parallel CMOS output from the ADC. The changes required to modify from DDR LVDS output to parallel CMOS output are shown in Table 5.

Table 5. Jumper and Component Settings for DDR LVDS Output and Parallel CMOS Output

Jumper/Component	DDR LVDS Output	Parallel CMOS
U12 (SN74AVC16T245)	DNI	Installed
U13 (SN74AVC16T245)	DNI	Installed
RN5 to RN8	Installed	DNI
RN9 to RN12	Installed	DNI
JP26	Open	Shunt
JP27	Open	Shunt

The CMOS output data is output from the EVM board at 40-pin connectors J1 (ch A) and J2 (ch B).

Revision History

Changes from Original (December 2012) to A Revision **Page**

- Changed register information in *Top Level* section. 2
- Changed *ADS42Bxx_GUI Front Panel – Top Level* image. 3
- Changed content in *Miscellaneous Settings* section. 4
- Added JP30 row to the end of the *Default ADS42Bxx EVM Revision A Jumper Setting for Serial Interface* table. 5
- Changed content of the bullets in *TSW1400 Quick Start Operation* section. 7
- Added content in the *ADS42B4x Test Procedure* section. 8
- Added new image in the *ADS42B4x Test Procedure* section. 8
- Changed *FFT Plot: 250-MHz clock, 170-MHz Input to Channel A* image. 9
- Changed *FFT Plot: 250-MHz clock, 170-MHz Input to Channel B* image. 9

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
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