User's Guide

TLV3601EVM User's Guide

ABSTRACT

The TLV3601EVM is an evaluation board designed to evaluate the high-speed TLV3601 and TLV3603 comparators. The PCB footprint for the comparator accommodates either the 5-pin SC70 TLV3601 or the 6-pin SC70 TLV3603 to be soldered on the board.

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Trademarks

1 Introduction

The TLV3601EVM is an evaluation board designed to evaluate the high-speed TLV3601 and TLV3603 comparators. The TLV3601EVM has layout options intended to make it simple to evaluate timing performance with different measurement tools. The output of the TLV3601 allows for direct connection to a 50 Ω terminated oscilloscope input or a high-speed, high impedance FET probe.

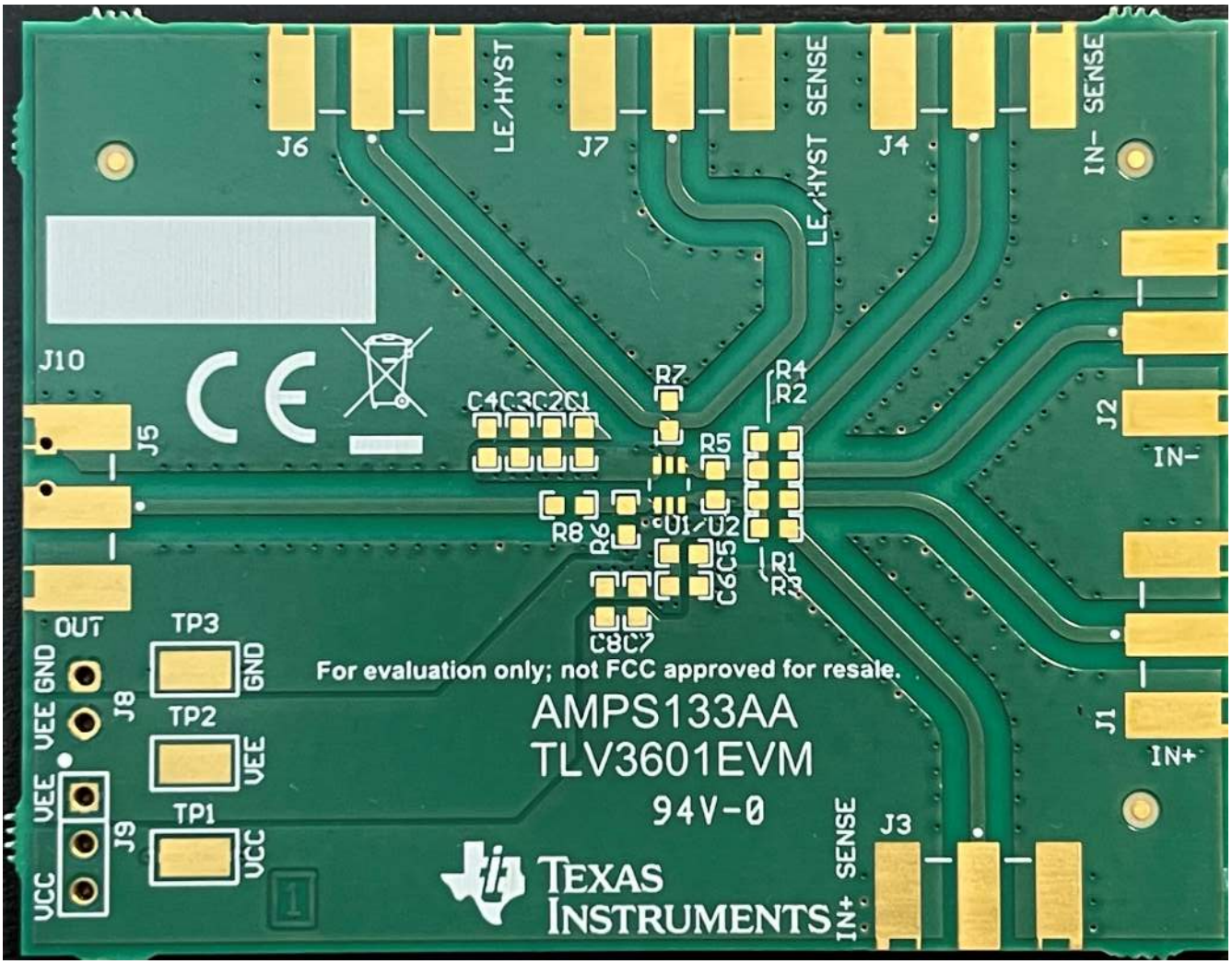

Figure 1-1. TLV3601EVM Board Top View

2 Features

- Low Propagation Delay
- Low Overdrive Dispersion
- High Toggle Frequency
- Narrow Pulse Width Detection Capability
- Single Ended Output Stage Output
- Low Input Offset Voltage
- 5-pin (TLV3601) and 6-pin (TLV3603) SC-70 Package

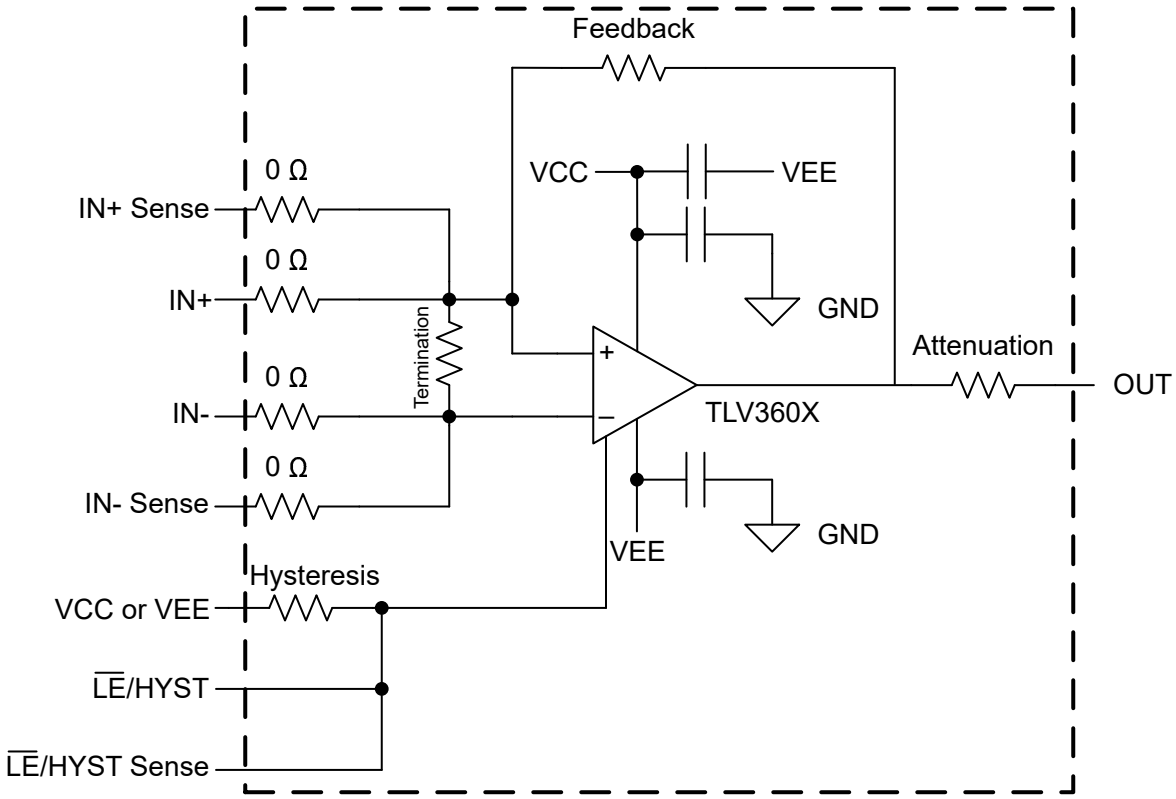

Figure 2-1. Block Diagram

3 EVM Specifications

- Supply Range (VCC - VEE): 2.4 V to 5.5 V
- Input Common Mode Range: (Vee -200 mV) to (VCCI/VCCO + 200 mV)

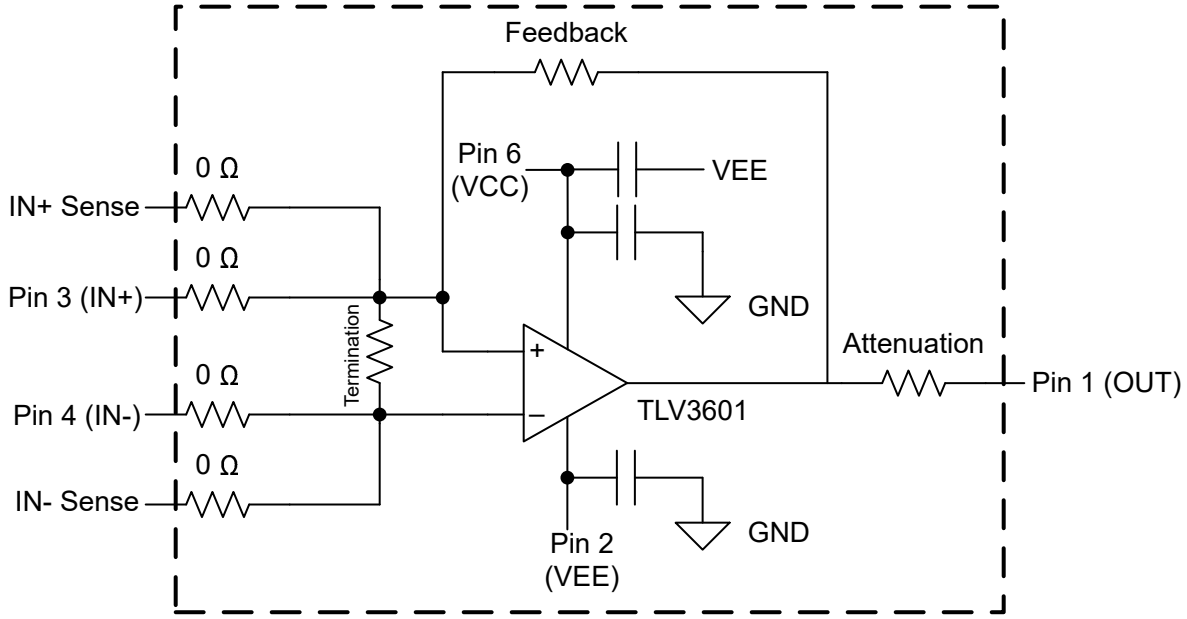

Figure 3-1. EVM Pin Assignments for Evaluating TLV3601

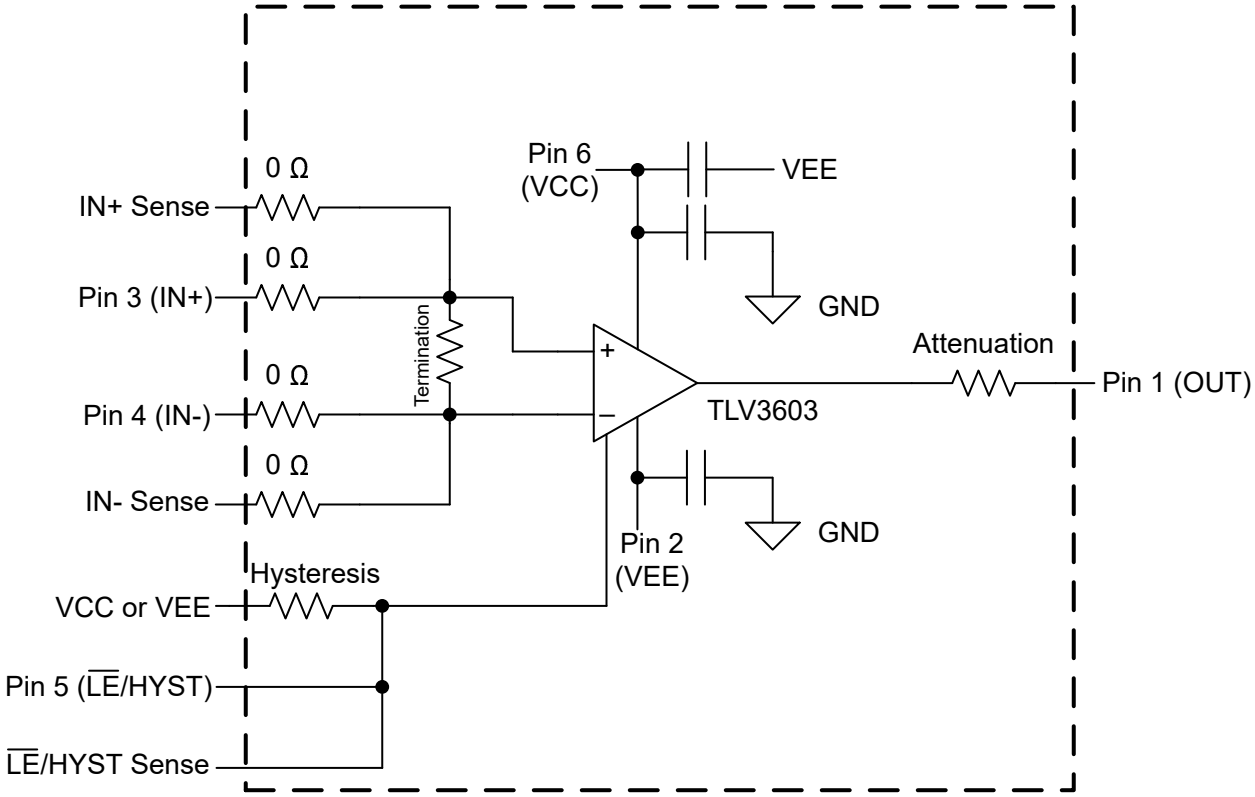

Figure 3-2. EVM Pin Assignments for Evaluating TLV3603

4 Recommended Equipment

- Power Supply
- High Speed Functional Generator
  - Fast rise/fall time recommended (≤ 500ps)
- High Speed Oscilloscope with 50Ω terminations
  - High bandwidth FET probe
- SMA Cables/adapters
  - Be sure to have matched length cables for IN+SENSE, IN-SENSE, and OUT
  - GND Barrel

5 Quick Start Procedure

CAUTION
DO NOT TURN ON POWER SUPPLY UNTIL ALL CONNECTIONS TO THE DEVICE ARE MADE TO THE BOARD.

The following connections are made using a split supply configuration. Split supply configuration is advantageous for measurement purposes. The reference voltage can be set to GND, while the other input can be set to an AC waveform that toggles between negative and positive voltage at a 0 DC offset. Thus, the output will be toggling whenever the AC waveform toggles.

This configuration allows for 2 distinct advantages compared to a single supply input. The first advantage is that the reference voltage is at GND; a non-noisy voltage level. If the reference voltage level needs to be changed in relation to the supplies, the supply voltages can be altered instead. The second advantage being able to zoom into the input as much as possible due to the 0 DC offset of the waveform.

1. Set power supply positive terminal to 2.5 V and negative terminal to -2.5 V. Disable power supply output.
2. Connect positive terminal supply to TP1, negative terminal to TP2, and GND to TP3.
3. Ensure that cables connecting to IN+SENSE and OUT are matched length and impedance. Perform any deskewing if necessary.
4. Set the function generator to produce a square wave output with 100mVpp at 1 MHz, with a DC offset of 0 V. Disable the signal generator output. Connect the output to IN+.
5. Connect IN- to GND through an SMA 50 Ω termination barrel.
6. Connect OUT to a 50Ω terminated scope channel.
7. Connect IN+SENSE to a 50Ω terminated scope channel.
8. Enable the power supply and the signal generator.
9. Verify the supply current is < 60 mA.
10. Monitor and verify the input from IN+SENSE.
11. Monitor and verify OUT.

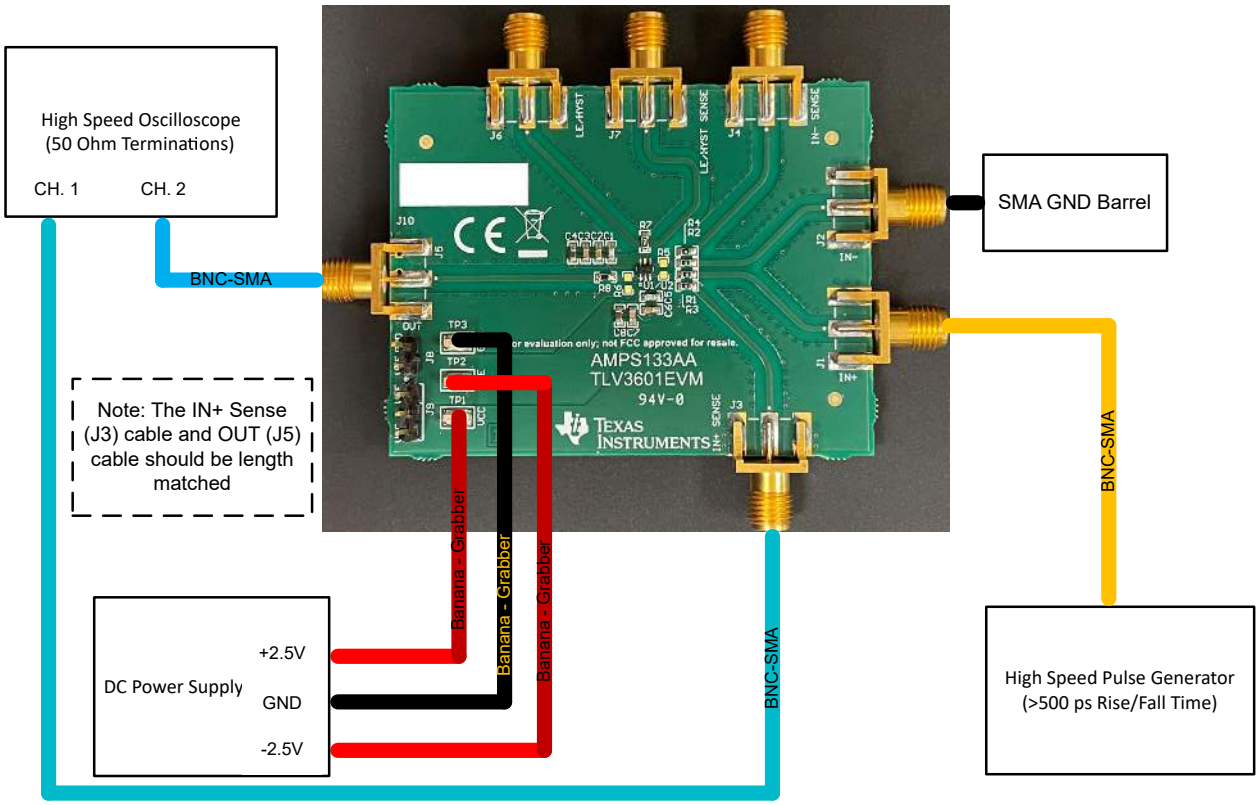

Figure 5-1. TLV3601 EVM Quick Start Setup

Next is a screen capture of the inputs and outputs described in the quick start procedure. Here, the propagation delay between IN+ and OUT is measured by taking the time delta between when IN+ and OUT reach 50% of their respective transitions. The low to high propagation delay in Figure 5-2 was calculated to be 2.184 ns while the high to low propagation delay in Figure 5-3 was measured to be 2.155 ns.

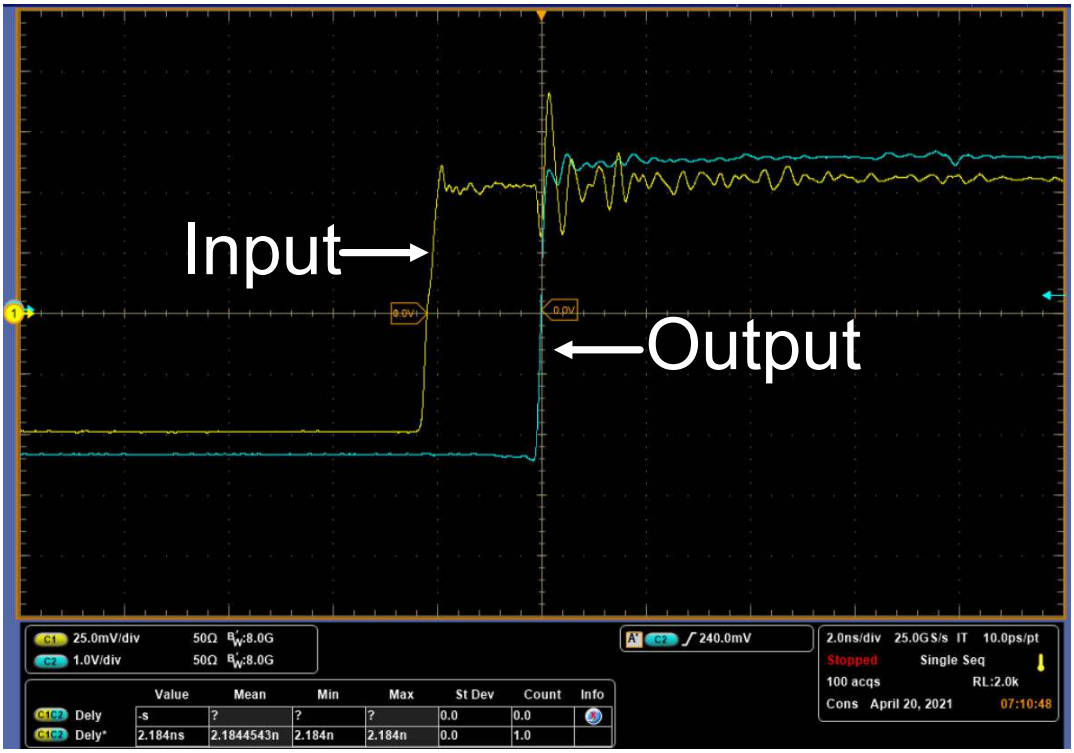

Figure 5-2. Propagation Delay Rise Portion

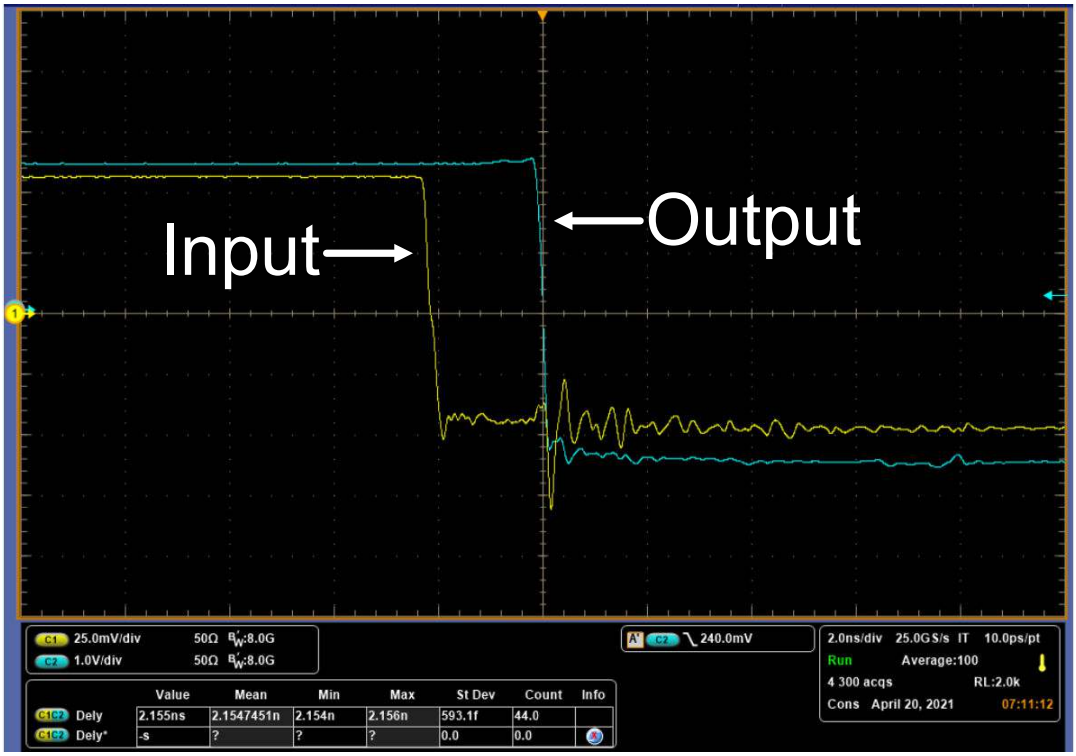

Figure 5-3. Propagation Delay Fall Portion

6 Board Setup

6.1 Supply Voltage

The TLV3601 EVM operates using a V_S (Supply Voltage, or VCC - VEE) from 2.4 V to 5.5 V. Connect VCC to TP1 and connect VEE to TP2. If using single supply configuration, short both pins of J8 together to connect GND and VEE. If dual supply configuration is used, leave J8 pins unconnected and make the VCC and VEE connections previously mentioned, in addition to a GND connection to TP3.

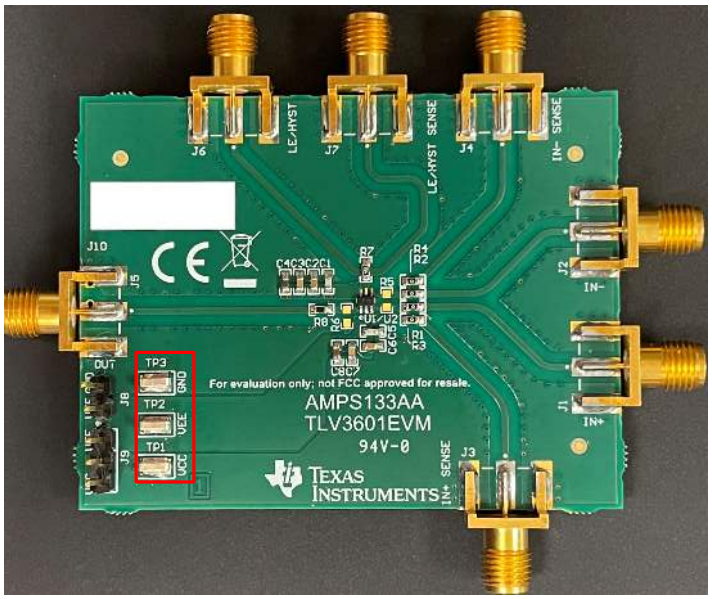

Figure 6-1. TLV3601 EVM Supply Voltage Connection

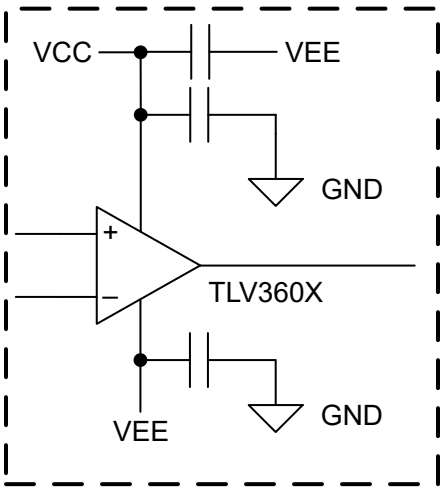

Figure 6-2. TLV3601 EVM Supply Voltage Schematic

6.2 Inputs

Resistors R1, R2, R3, and R4 are all 0 Ω resistor components. The input terminals (IN+ and IN-) have corresponding sense lines so that the inputs to the device can be terminated on the lines with 50 Ω to an oscilloscope. This allows the input signals to be observed with minimal loading and distortion. All input connections are through SMA connectors. If the input signal to the device does not need to be evaluated on an oscilloscope, R3 and R4 can be left uninstalled. However, your input signal may need to be terminated if the oscilloscope's 50 Ω setting is not connected.

The TLV3601EVM has an optional resistor pad on the input (R5) side of the device meant for termination of the input signal. R5 can be populated with a 100 Ω resistor if applying an unterminated LVDS signal to the board.

Alternatively, it can be populated with a 50 Ω resistor if applying a function generator output that needs a 50 Ω termination. One of the inputs would be GND and the board would be operating in split supply in this situation. Otherwise the pad can be left unpopulated.

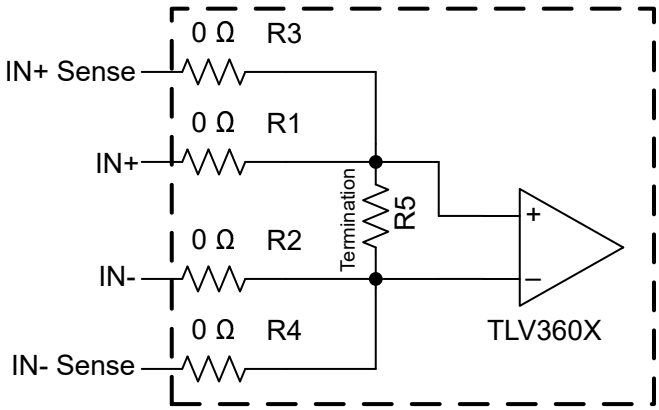

Figure 6-3. Input Side Schematic

6.3 Outputs

R8 is known as the attenuation resistor, and is used to attenuate the output by setting the top half of a voltage divider circuit, with the bottom half supplied by the load, such as an oscilloscope's internal termination. It is not advisable to populate with a low value resistor as the TLV3601 output cannot drive such a load as the amount of current sourced would be significant. A 1 kΩ resistor is recommended for this footprint which, coupled with a scope's internal 50 Ω termination creates an attenuation factor of 1:21 which can be rectified using oscilloscope settings. A high speed probe may be used for measurement of the output, but rise and fall times may be limited.

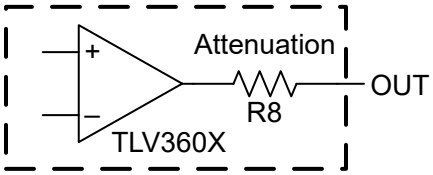

Figure 6-4. Output Side Block Diagram

Two types of output connections are supplied depending on the needed configuration. J5, an SMA connector, can be populated or J10, a two-pin jumper, can be populated if using an active probe. If measuring the output and input (via input sense connections J3 and J4), it is recommended to use length matched cables on the output and sense lines to minimize distortion issues.

6.4 Hysteresis

The TLV3601 EVM is able to support both the TLV3601 and TLV3603 devices. A key difference between devices is the way hysteresis is able to be applied.

The TLV3601 needs hysteresis applied through external components R6, a feedback resistor, and R1, a series resistor for IN+. Necessary calculations for the hysteric window must be made to figure out the value of both resistors.

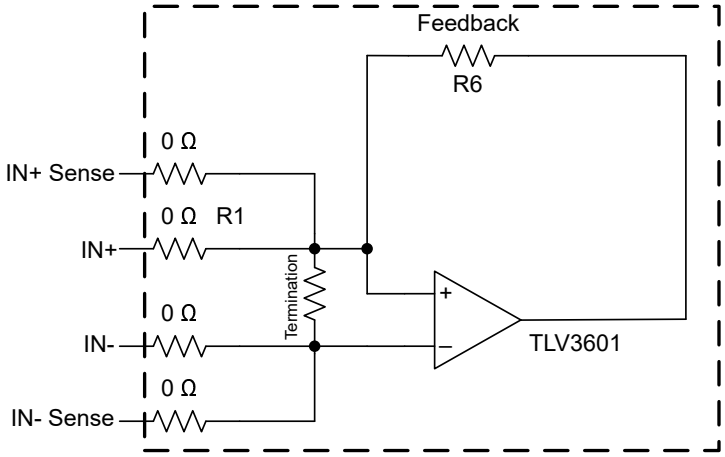

Figure 6-5. TLV3601 Hysteresis Schematic

The TLV3603 utilizes an extra pin not available on the TLV3601, called LE/HYST. This pin is able to adjust the internal hysteresis of the device, through the attachment of an external resistor (R7) connecting to VEE. To understand the relationship between the resistor value of R7 and the amount of hysteresis created, see TLV3603 data sheet.

Alternatively, the pin also functions as an inverting Latch Enable. If the pin is connected to VEE, the device will hold the output state for as long as the pin remains connected to that voltage. If the pin is connected to VCC, the device will function normally with no hysteresis. Connections for VCC and VEE are supplied through J9 with R7 being populated with a 0 Ω resistor. However, if it is necessary to control when the device latches, a pulsing signal can be applied to SMA connector J6, with SMA connector J7 being the corresponding sense line for that input.

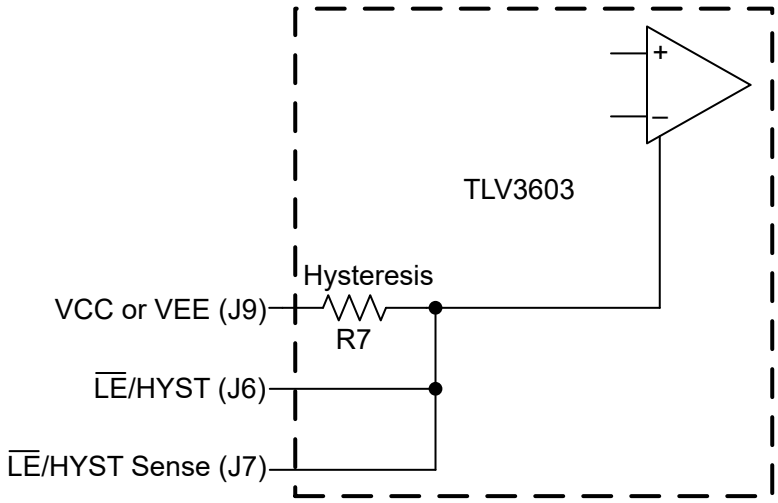

Figure 6-6. TLV3603 Hysteresis Schematic

7 Layout Guidelines

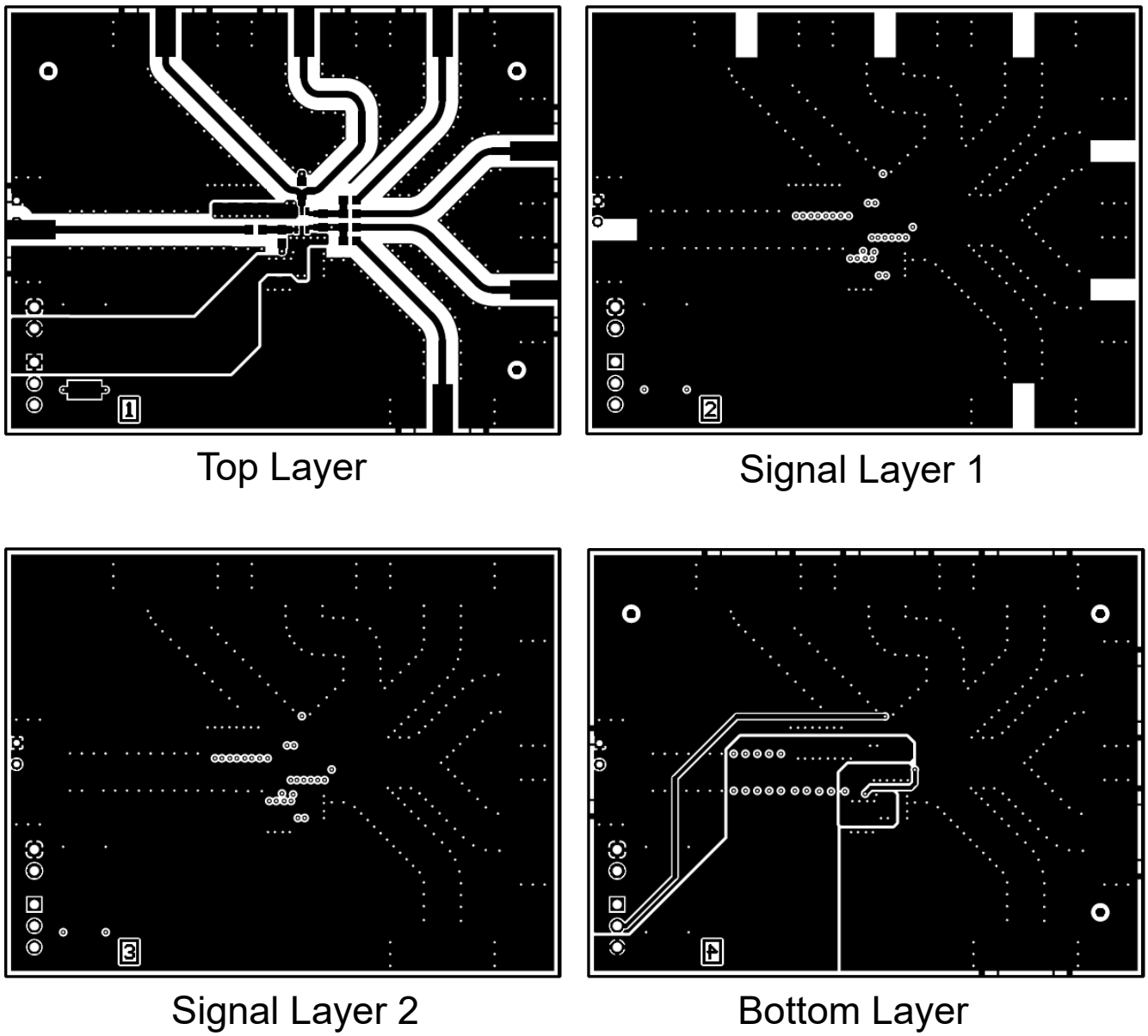

Figure 7-1. Layers

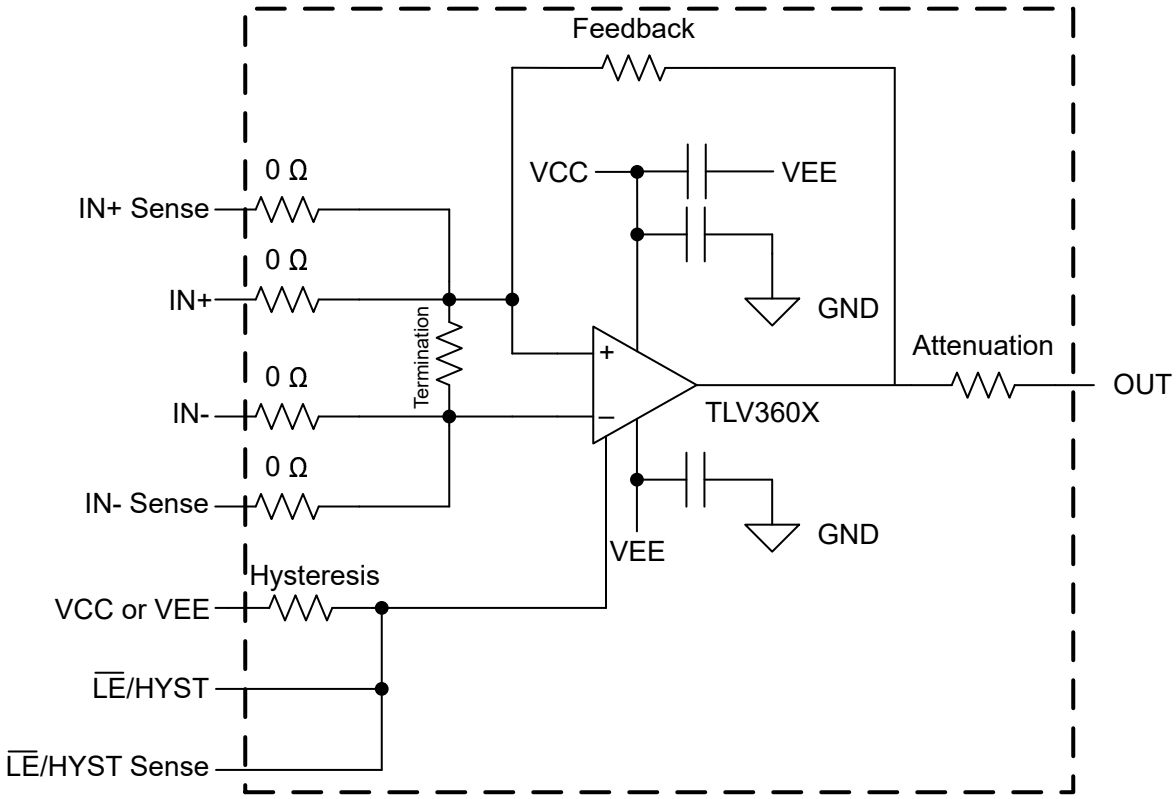

Figure 7-2. Block Diagram

8 Schematic

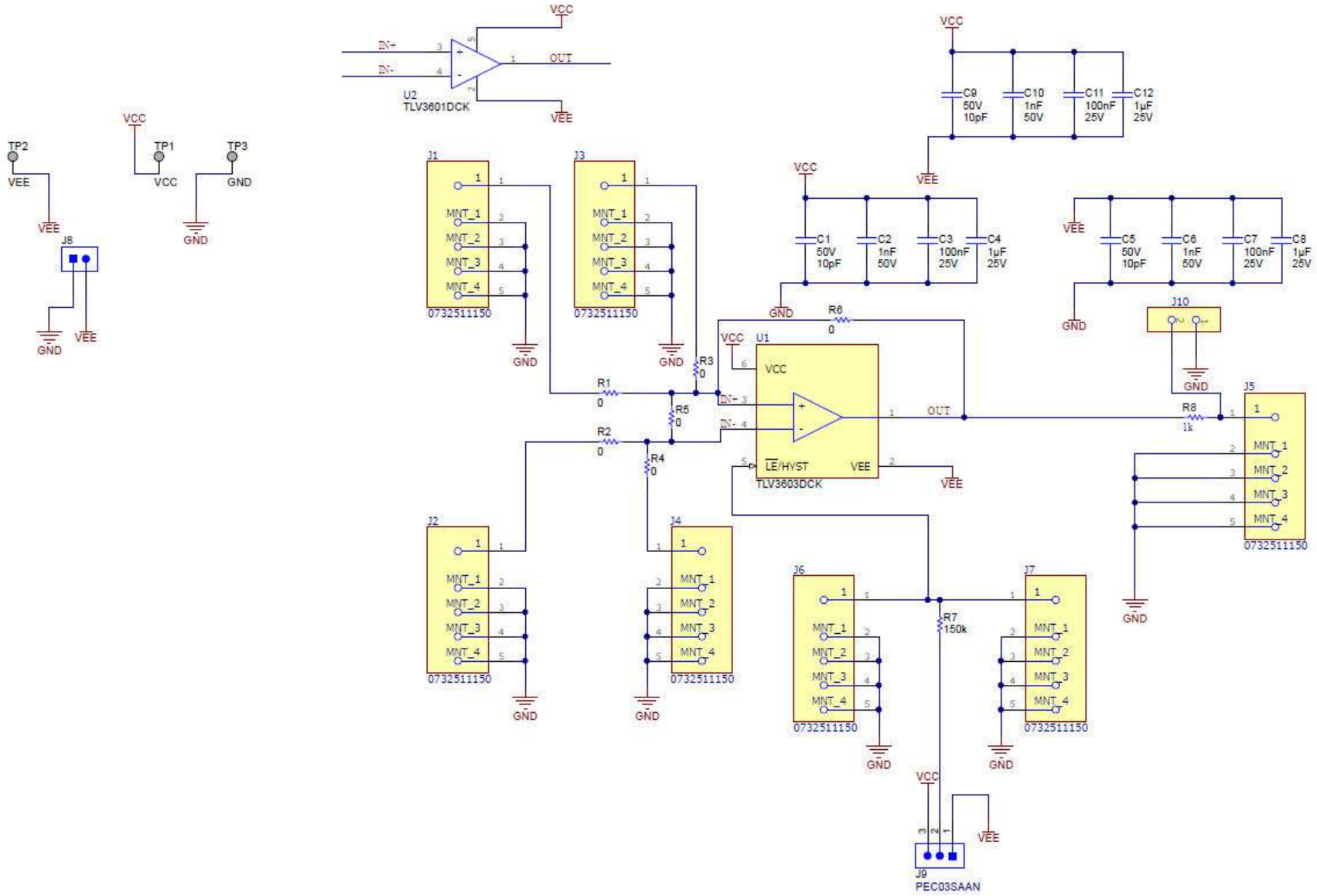

Figure 8-1. TLV3601 EVM Schematic

9 Bill of Materials

Table 9-1. TLV360xEVM Bill of Materials

Designator	QTY	Value	Description	Package Reference	Part Number	Manufacturer
C1, C5, C9	0	10pF	CAP, CERM, 10 pF, 50 V, +/- 5%, C0G/NP0, AEC-Q200 Grade 1, 0603	0603	CGA3E2C0G1H100D080AA	TDK
C2, C6, C10	0	1000pF	CAP, CERM, 1000 pF, 50 V, +/- 5%, X7R, 0603	0603	CL10C102JB8NNNC	Samsung Electro-Mechanics
C3, C7, C11	0	0.1uF	CAP, CERM, 0.1 uF, 25 V, +/- 5%, X7R, 0603	0603	C0603C104J3RACTU	Kemet
C4, C8, C12	0	1uF	CAP, CERM, 1 uF, 25 V, +/- 10%, X7R, 0603	0603	C0603C105K3RACTU	Kemet
FID1, FID2, FID3, FID4, FID5, FID6	0		Fiducial mark. There is nothing to buy or mount.	N/A	N/A	N/A
H1, H2, H3, H4	0		Bumpon, Hemisphere, 0.44 X 0.20, Clear	Transparent Bumpon	SJ-5303 (CLEAR)	3M
J1, J2, J3, J4, J5, J6, J7	0		SMA Connector Receptacle, Female Socket 50Ohm Board Edge, End Launch Solder		0732511150	Molex Inc
J8	0		Header, 100mil, 2x1, Gold, TH	2x1 Header	TSW-102-07-G-S	Samtec
J9	0		Header, 100mil, 3x1, Tin, TH	Header, 3 PIN, 100mil, Tin	PEC03SAAN	Sullins Connector Solutions
J10	0		STANDRD SOLDER TAIL SIP SOCKET; 02 Pins; Tin (matte) over Nickel	HDR2	399-43-102-10-003000	Mill-Max
R1, R2, R3, R4, R5, R6	0	0	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW06030000Z0EA	Vishay-Dale
R7	0	150k	RES, 150 k, 5%, 0.1 W, 0603	0603	CRCW0603150KJNEA	Vishay-Dale
R8	0	1k	RES, 1 k, 1%, 0.1 W, 0603	0603	RC0603FR-071KL	Yageo America
TP1, TP2, TP3	0		Test Point, Miniature, SMT	Test Point, Miniature, SMT	5019	Keystone
U1	0		2.5ns High-Speed Comparator with Push Pull Output	SC70-6	TLV3603DCK	Texas Instruments
U2	0		2.5ns High-Speed Comparator with Push Pull Output, SC70-5	SC70-6	TLV3601DCK	Texas Instruments

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