19-3592; Rev 0; 2/05

526ksps, Single-Channel, 14-Bit, Parallel-Interface ADCs

General Description

The MAX1319/MAX1323/MAX1327 are single-channel, 14-bit, 526ksps analog-to-digital converters (ADCs) with ±2 LSB INL and ±1 LSB DNL with no missing codes. The MAX1323 has a ±5V input range with ±16.5V fault-tolerant inputs. The MAX1327 has a ±10V input range with ±16.5V fault-tolerant inputs and the MAX1319 has a 0 to +5V input range with ±6.0V fault-tolerant inputs. Other features include a 10MHz track/hold (T/H) input bandwidth, internal clock, internal (+2.5V) or external (+2.0V to +3.0V) reference, and shutdown mode.

A 16.6MHz, 14-bit, parallel interface provides the conversion results and accepts digital configuration inputs.

These devices operate from a +4.75V to +5.25V analog supply and a separate +2.7V to +5.25V digital supply, and consume less than 35mA total supply current. For multichannel applications, refer to the MAX1316–MAX1318/MAX1320–MAX1322/MAX1324–MAX1326 data sheet.

These devices come in a 48-pin TQFP package and operate over the extended -40°C to +85°C temperature range.

Applications

Vibration and Waveform Analysis

Data-Acquisition Systems

Industrial Process Control and Automation

Ordering Information/ Selector Guide

PART	PIN-PACKAGE	INPUT RANGE (V)	PKG CODE
MAX1319ECM	48 TQFP	0 to +5	C48-6
MAX1323ECM	48 TQFP	±5	C48-6
MAX1327ECM	48 TQFP	±10	C48-6

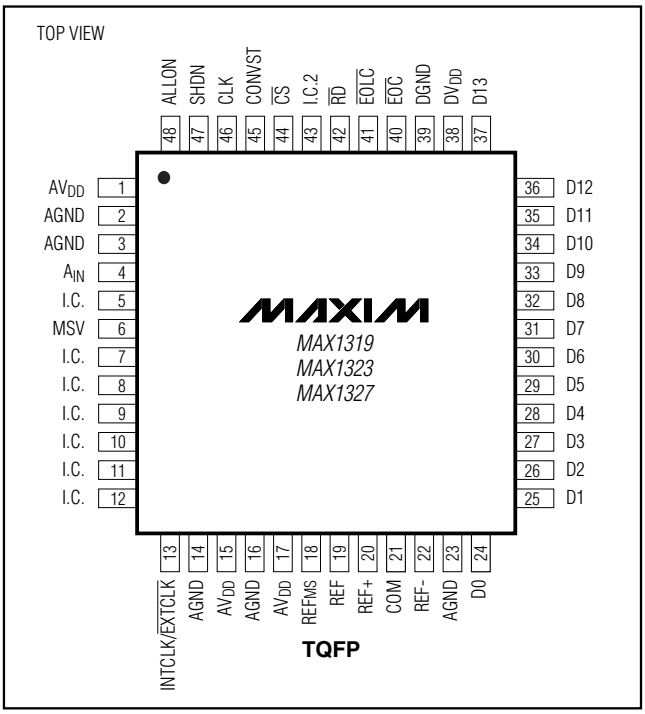
Note: All devices operate over the -40°C to +85°C temperature range.

Typical Operating Circuits appear at end of data sheet.

Features

- ♦ **14-Bit ADCs**
  526ksps
  ±2 LSB INL, ±1 LSB DNL, No Missing Codes
  90dBc SFDR, -86dBc THD, 76.5dB SINAD, 77dB SNR at 100kHz Input
- ♦ **Fast 1.6µs Conversion Time**
- ♦ **Flexible Input Ranges**
  0 to +5V (MAX1319)
  ±5V (MAX1323)
  ±10V (MAX1327)
- ♦ **No Calibration Needed**
- ♦ **14-Bit High-Speed Parallel Interface**
- ♦ **Internal or External Clock**
- ♦ **+2.5V Internal Reference or +2.0V to +3.0V External Reference**
- ♦ **+5V Analog Supply, +3V to +5V Digital Supply**
  32mA Analog Supply Current (typ)
  550µA Digital Supply Current (typ)
  Shutdown and Power-Saving Modes
- ♦ **48-Pin TQFP Package (7mm x 7mm Footprint)**

Pin Configuration



526ksps, Single-Channel, 14-Bit, Parallel-Interface ADCs

ABSOLUTE MAXIMUM RATINGS

AV_{DD} to AGND .....-0.3V to +6V
DV_{DD} to DGND.....-0.3V to +6V
AGND to DGND.....-0.3V to +0.3V
CH0, I.C. to AGND (MAX1319).....±6.0V
CH0, I.C. to AGND (MAX1323/MAX1327).....±16.5V
INTCLK/$\overline{EXTCLK}$ to AGND.....-0.3V to (AV_{DD} + 0.3V)
$\overline{EOC}$, $\overline{EOLC}$, $\overline{WR}$, I.C.2, $\overline{RD}$, $\overline{CS}$ to DGND.....-0.3V to (DV_{DD} + 0.3V)
CONVST, CLK, SHDN, ALLON to DGND.....-0.3V to (DV_{DD} + 0.3V)
MSV, REF_{MS}, REF to AGND.....-0.3V to (AV_{DD} + 0.3V)
REF+, COM, REF- to AGND.....-0.3V to (AV_{DD} + 0.3V)
D0–D13 to DGND .....-0.3V to (DV_{DD} + 0.3V)
Maximum Current into Any Pin Except AV_{DD}, DV_{DD}, AGND, DGND .....±50mA
Continuous Power Dissipation (T_A = +70°C)
TQFP (derate 22.7mW/°C above +70°C).....1818mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(AV_{DD} = +5V, DV_{DD} = +3V, AGND = DGND = 0V, V_{REF} = V_{REFMS} = +2.5V (external reference), C_{REF} = C_{REFMS} = 0.1µF, C_{REF+} = C_{REF-} = 0.1µF, $C_{REF+-to-REF-}$ = 2.2µF || 0.1µF, C_{COM} = 2.2µF || 0.1µF, C_{MSV} = 2.2µF || 0.1µF (MAX1319; unipolar device), MSV = AGND (MAX1323/MAX1327; bipolar devices), f_{CLK} = 10MHz 50% duty, t_{ACQ} = 200ns, t_{QUIET} = 10ns, INTCLK/$\overline{EXTCLK}$ = AGND (external clock), SHDN = DGND, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC PERFORMANCE (Note 1)						
Resolution	N		14			Bits
Integral Nonlinearity	INL	(Note 2)		±0.8	±2	LSB
Differential Nonlinearity	DNL	No missing codes		±0.5	±1	LSB
Offset Error		Unipolar device			±33	LSB
		Bipolar devices			±33	
Offset Drift		Unipolar device		4		ppm/°C
		Bipolar devices		4		
Gain Error		(Note 3)		±10	±49	LSB
Gain Temperature Coefficient				3		ppm/°C
DYNAMIC PERFORMANCE (at f_{IN} = 100kHz, -0.4dBFS)						
Signal-to-Noise Ratio	SNR	Unipolar	74.5	76		dB
		Bipolar	75	76.5		
Signal-to-Noise and Distortion Ratio	SINAD	Unipolar	74.5	76.0		dB
		Bipolar	75	76.5		
Spurious Free Dynamic Range	SFDR		83	93		dBc
Total Harmonic Distortion	THD			-90	-83	dBc
ANALOG INPUTS (CH0–CH7)						
Input Voltage Range		MAX1319	0		+5	V
		MAX1323	-5		+5	
		MAX1327	-10		+10	

ELECTRICAL CHARACTERISTICS (continued)

(AV_{DD} = +5V, DV_{DD} = +3V, AGND = DGND = 0V, V_{REF} = V_{REFMS} = +2.5V (external reference), C_{REF} = C_{REFMS} = 0.1µF, C_{REF+} = C_{REF-} = 0.1µF, $C_{REF+-to-REF-}$ = 2.2µF ll 0.1µF, C_{COM} = 2.2µF ll 0.1µF, C_{MSV} = 2.2µF ll 0.1µF (MAX1319; unipolar device), MSV = AGND (MAX1323/MAX1327; bipolar devices), f_{CLK} = 10MHz 50% duty, t_{ACQ} = 200ns, t_{QUIET} = 10ns, INTCLK/$\overline{EXTCLK}$ = AGND (external clock), SHDN = DGND, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Current		MAX1319	V_{IN} = +5V		0.54	0.72	mA
			V_{IN} = 0V	-0.157	-0.12		
		MAX1323	V_{IN} = +5V		0.29	0.39	
			V_{IN} = -5V	-1.16	-0.87		
		MAX1327	V_{IN} = +10V		0.56	0.74	
			V_{IN} = -10V	-1.13	-0.85		
Input Resistance		MAX1319			7.58		kΩ
		MAX1323			8.66		
		MAX1327			14.26		
Input Capacitance					15		pF
TRACK/HOLD							
External Clock Throughput Rate					526		ksps
Internal Clock Throughput Rate					526		ksps
Small-Signal Bandwidth					10		MHz
Full-Power Bandwidth					10		MHz
Aperture Delay					16		ns
Aperture Jitter					50		ps_{RMS}
INTERNAL REFERENCE							
REF_{MS} Voltage	V_{REFMS}			2.475	2.500	2.525	V
REF Voltage	V_{REF}			2.475	2.500	2.525	V
REF Temperature Coefficient					30		ppm/°C
EXTERNAL REFERENCE (REF_{MS} and REF externally driven)							
Input Current				-250		+250	µA
REF_{MS} Input Voltage Range	V_{REFMS}	Unipolar device		2.0	2.5	3.0	V
REF Input Voltage Range	V_{REF}			2.0	2.5	3.0	V
REF Input Capacitance					15		pF
REF_{MS} Input Capacitance					15		pF

526ksps, Single-Channel, 14-Bit, Parallel-Interface ADCs

ELECTRICAL CHARACTERISTICS (continued)

(AV_{DD} = +5V, DV_{DD} = +3V, AGND = DGND = 0V, V_{REF} = V_{REFMS} = +2.5V (external reference), C_{REF} = C_{REFMS} = 0.1µF, C_{REF+} = C_{REF-} = 0.1µF, $C_{REF+-to-REF-}$ = 2.2µF ll 0.1µF, C_{COM} = 2.2µF ll 0.1µF, C_{MSV} = 2.2µF ll 0.1µF (MAX1319; unipolar device), MSV = AGND (MAX1323/MAX1327; bipolar devices), f_{CLK} = 10MHz 50% duty, t_{ACQ} = 200ns, t_{QUIET} = 10ns, INTCLK/$\overline{EXTCLK}$ = AGND (external clock), SHDN = DGND, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL INPUTS (D0–D7, $\overline{RD}$, $\overline{CS}$, CLK, SHDN, CONVST)						
Input-Voltage High	V_{IH}		0.7 x DV_{DD}			V
Input-Voltage Low	V_{IL}				0.3 x DV_{DD}	V
Input Hysteresis				15		mV
Input Capacitance	C_{IN}			15		pF
Input Current	I_{IN}	V_{IN} = 0V or DV_{DD}			±1	µA
CLOCK-SELECT INPUT (INTCLK/$\overline{EXTCLK}$)						
Input-Voltage High			0.7 x AV_{DD}			V
Input-Voltage Low					0.3 x AV_{DD}	V
DIGITAL OUTPUTS (D0–D13, $\overline{EOC}$, $\overline{EOLC}$)						
Output-Voltage High	V_{OH}	I_{SOURCE} = 0.8mA	DV_{DD} - 0.6			V
Output-Voltage Low	V_{OL}	I_{SINK} = 1.6mA			0.4	V
Tri-State Leakage Current		$\overline{RD}$ ≥ V_{IH} or $\overline{CS}$ ≥ V_{IH}		0.06	1	µA
Tri-State Output Capacitance		$\overline{RD}$ ≥ V_{IH} or $\overline{CS}$ ≥ V_{IH}		15		pF
POWER SUPPLIES						
Analog Supply Voltage	AV_{DD}		4.75		5.25	V
Digital Supply Voltage	DV_{DD}		2.70		5.25	V
Analog Supply Current	I_{AVDD}	MAX1319		32	36	mA
		MAX1323/MAX1327		28	32	
Digital Supply Current	I_{DVDD}				700	µA
Shutdown Current		V_{SHDN} = DV_{DD}			10	µA
		$V_{\overline{RD}}$ = DV_{DD}, V_{SHDN} = DV_{DD}		0.1	2	µA
Power-Supply Rejection Ratio	PSRR	AV_{DD} = +4.75V to +5.75V (Note 5)		50		dB

TIMING CHARACTERISTICS (Figures 3, 4, 5, and 6) (Tables 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Conversion Time	t_{CONV}	Internal clock		1.6	1.8	ns
		External clock (Figure 4)		16		Clock cycles
CONVST Pulse-Width Low (Acquisition Time)	t_{ACQ}	(Note 4)	0.16		100	µs
$\overline{CS}$ Pulse Width	t_2		30			ns
$\overline{RD}$ Pulse-Width Low	t_3		30			ns
$\overline{CS}$ to $\overline{RD}$ Setup Time	t_8		0			ns
$\overline{RD}$ to $\overline{CS}$ Hold Time	t_9		0			ns
Data Access Time ($\overline{RD}$ Low to Valid Data)	t_{10}				30	ns
Bus Relinquish Time ($\overline{RD}$ High)	t_{11}				30	ns
$\overline{EOC}$ Pulse Width	t_{12}	Internal clock	80			ns
		External clock (Figure 4)		1		Clock cycle
External CLK Period	t_{16}		90			ns
External CLK High Period	t_{17}	Logic sensitive to rising edges	20			ns
External CLK Low Period	t_{18}	Logic sensitive to rising edges	20			ns
External Clock Frequency		(Note 6)	0.1		12.5	MHz
Internal Clock Frequency				10		MHz
CONVST High to CLK Edge	t_{19}	(Note 7)	20			ns
$\overline{EOC}$ Low to $\overline{RD}$	t_{20}		0			ns

Note 1: For the MAX1319, V_{IN} = 0 to +5V. For the MAX1323, V_{IN} = -5V to +5V. For the MAX1327, V_{IN} = -10V to +10V.

Note 2: INL is defined as the deviation of the analog value at any code from its theoretical value after offset and gain errors have been removed.

Note 3: Offset nulled.

Note 4: CONVST must remain low for at least the acquisition period.

Note 5: Defined as the change in positive full scale caused by a ±5% variation in the nominal supply voltage.

Note 6: Minimum clock frequency is limited only by the internal T/H droop rate. Limit the time between the falling edge of CONVST to the falling edge of EOLC to a maximum of 0.25ms.

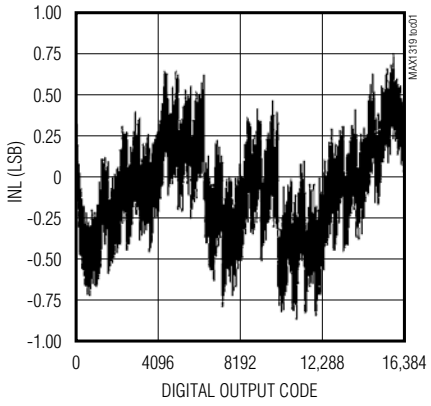
Note 7: To avoid T/H droop degrading the sampled analog input signals, the first clock pulse should occur within 10µs of the rising edge of CONVST and have a minimum clock frequency of 100kHz.

526ksps, Single-Channel, 14-Bit, Parallel-Interface ADCs

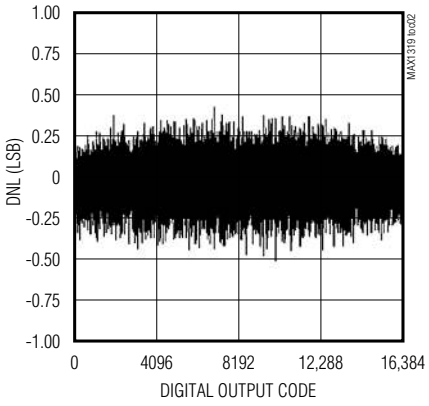
Typical Operating Characteristics

(AV_{DD} = +5V, DV_{DD} = +3V, AGND = DGND = 0V, V_{REF} = V_{REFMS} = +2.5V (external reference), see the *Typical Operating Circuits*, f_{CLK} = 10MHz 50% duty, INTCLK/$\overline{EXTCLK}$ = AGND (external clock), SHDN = DGND, T_A = +25°C.)

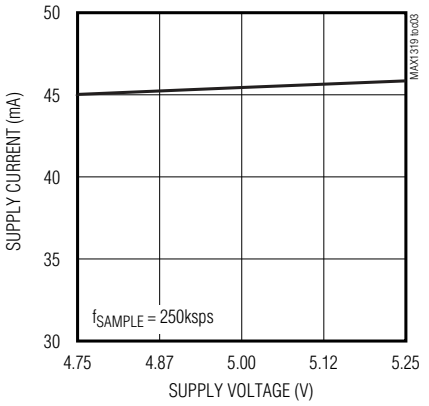
INTEGRAL NONLINEARITY vs. DIGITAL OUTPUT CODE



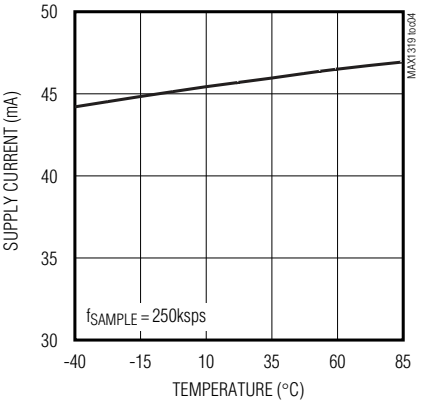
DIFFERENTIAL NONLINEARITY vs. DIGITAL OUTPUT CODE



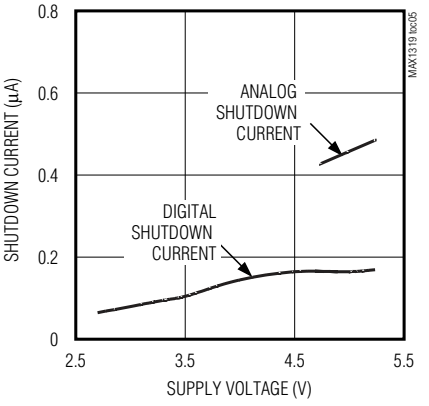
ANALOG SUPPLY CURRENT vs. SUPPLY VOLTAGE



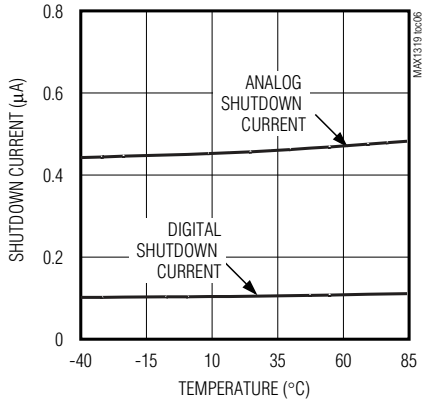
ANALOG SUPPLY CURRENT vs. TEMPERATURE



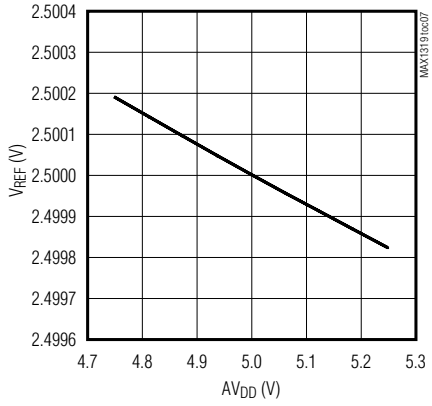
SHUTDOWN CURRENT vs. SUPPLY VOLTAGE



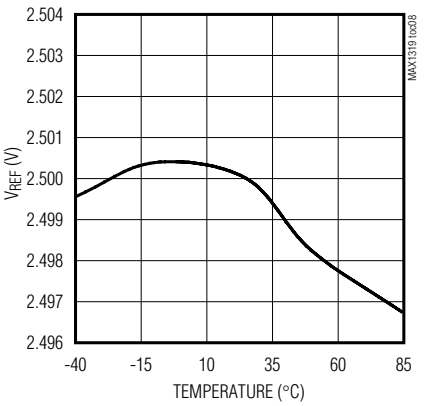
SHUTDOWN CURRENT vs. TEMPERATURE



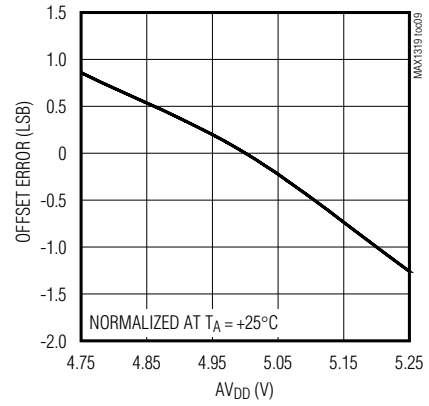
INTERNAL REFERENCE VOLTAGE vs. ANALOG SUPPLY VOLTAGE



INTERNAL REFERENCE VOLTAGE vs. TEMPERATURE



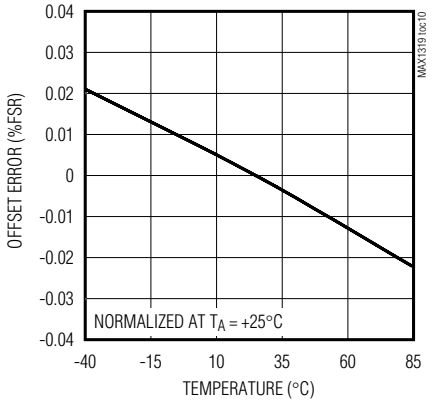
OFFSET ERROR vs. SUPPLY VOLTAGE



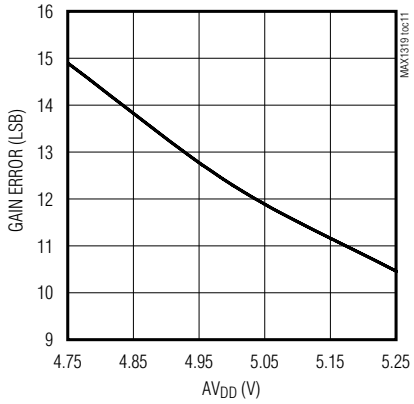
Typical Operating Characteristics (continued)

(AV_{DD} = +5V, DV_{DD} = +3V, AGND = DGND = 0V, V_{REF} = V_{REFMS} = +2.5V (external reference), see the *Typical Operating Circuits*, f_{CLK} = 10MHz 50% duty, INTCLK/$\overline{EXTCLK}$ = AGND (external clock), SHDN = DGND, T_A = +25°C.)

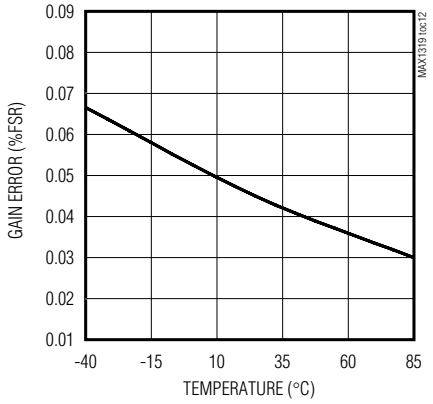
OFFSET ERROR vs. TEMPERATURE



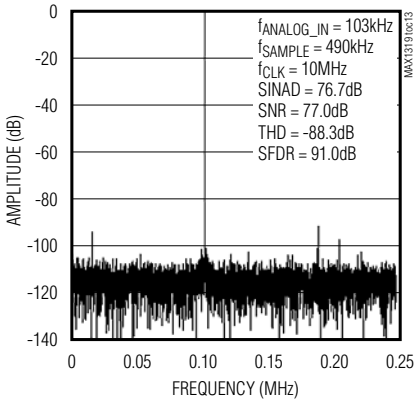
GAIN ERROR vs. SUPPLY VOLTAGE



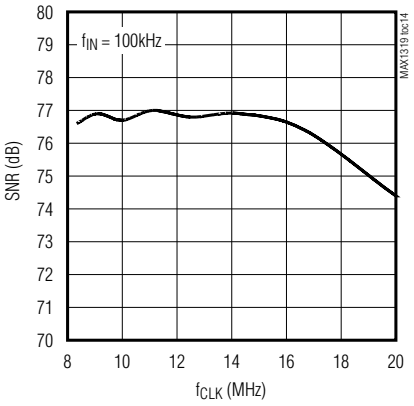
GAIN ERROR vs. TEMPERATURE



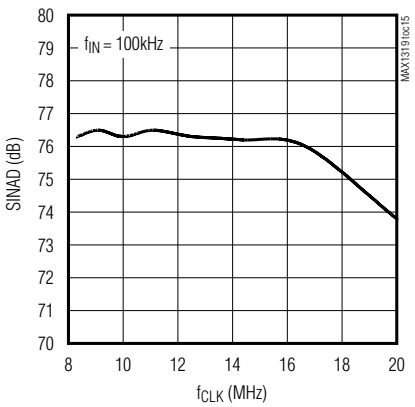
FFT



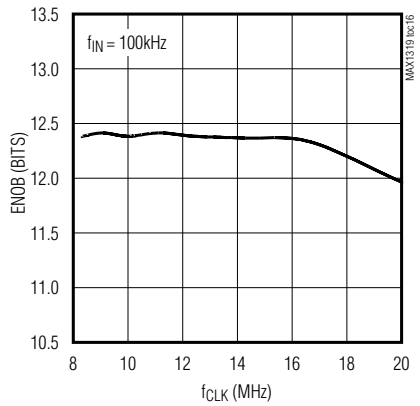
SIGNAL-TO-NOISE RATIO vs. CLOCK FREQUENCY



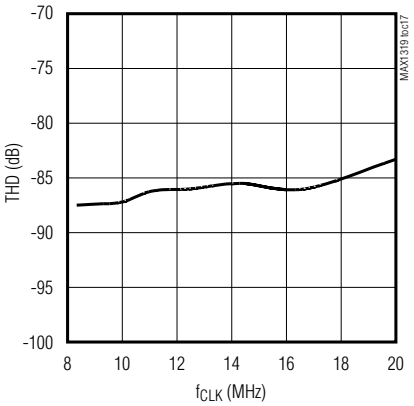
SIGNAL-TO-NOISE PLUS DISTORTION vs. CLOCK FREQUENCY



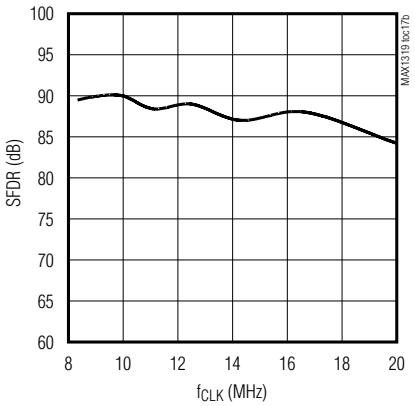
EFFECTIVE NUMBER OF BITS vs. CLOCK FREQUENCY



TOTAL HARMONIC DISTORTION vs. CLOCK FREQUENCY



SPURIOUS-FREE DYNAMIC RANGE vs. CLOCK FREQUENCY

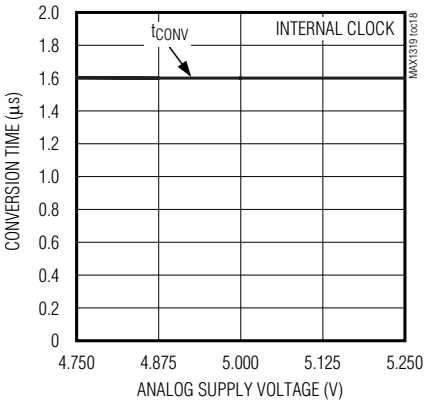


526ksps, Single-Channel, 14-Bit, Parallel-Interface ADCs

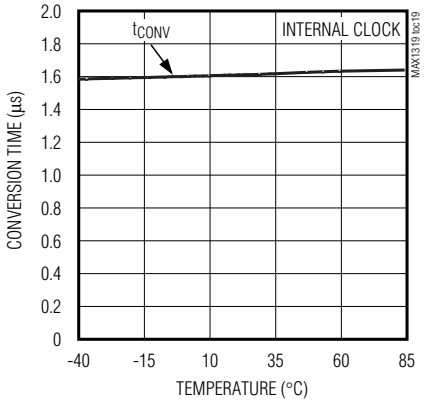
Typical Operating Characteristics (continued)

(AV_{DD} = +5V, DV_{DD} = +3V, AGND = DGND = 0V, V_{REF} = V_{REFMS} = +2.5V (external reference), see the *Typical Operating Circuits*, f_{CLK} = 10MHz 50% duty, INTCLK/$\overline{EXTCLK}$ = AGND (external clock), SHDN = DGND, T_A = +25°C.)

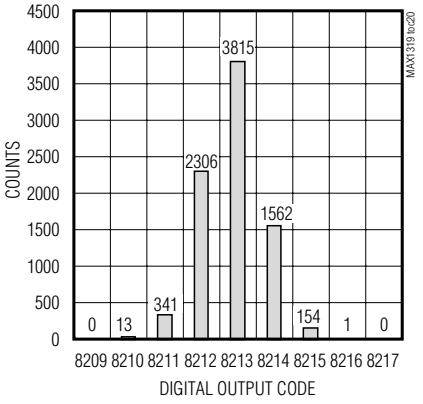
CONVERSION TIME vs. ANALOG SUPPLY VOLTAGE



CONVERSION TIME vs. TEMPERATURE



OUTPUT HISTOGRAM (DC INPUT)



Pin Description

PIN	NAME	FUNCTION
1, 15, 17	AV_{DD}	Analog Supply Input. AV_{DD} is the power input for the analog section of the converter. Apply +5V to AV_{DD}. Bypass AV_{DD} to AGND with a 0.1µF capacitor at each AV_{DD} input.
2, 3, 14, 16, 23	AGND	Analog Ground. AGND is the power return for AV_{DD}. Connect all AGNDs together.
4	A_{IN}	Analog Input
5, 7–12	I.C.	Internally Connected. Connect I.C. to AGND.
6	MSV	Midscale Voltage Bypass. For the MAX1319, connect a 2.2µF and a 0.1µF capacitor from MSV to AGND. For the MAX1323/MAX1327, connect MSV directly to AGND.
13	INTCLK/$\overline{EXTCLK}$	Clock-Mode Select Input. Use INTCLK/$\overline{EXTCLK}$ to select the internal or external conversion clock. Connect INTCLK/$\overline{EXTCLK}$ to AV_{DD} to select the internal clock. Connect INTCLK/$\overline{EXTCLK}$ to AGND to use an external clock connected to CLK.
18	REF_{MS}	Midscale Reference Bypass or Input. REF_{MS} is the bypass point for an internally generated reference voltage. For the MAX1319, connect a 0.1µF capacitor from REF_{MS} to AGND. For the MAX1323/MAX1327, connect REF_{MS} directly to REF and bypass with a 0.1µF capacitor from REF_{MS} to AGND.
19	REF	ADC Reference Bypass or Input. REF is the bypass point for an internally generated reference voltage. Bypass REF with a 0.01µF capacitor to AGND. REF can be driven externally by a precision external voltage reference.
20	REF+	Positive Reference Bypass. REF+ is the bypass point for an internally generated reference voltage. Bypass REF+ with a 0.1µF capacitor to AGND. Also bypass REF+ to REF- with a 2.2µF and a 0.1µF capacitor.
21	COM	Reference Common Bypass. COM is the bypass point for an internally generated reference voltage. Bypass COM to AGND with a 2.2µF and a 0.1µF capacitor.

Pin Description (continued)

PIN	NAME	FUNCTION
22	REF-	Negative Reference Bypass. REF- is the bypass point for an internally generated reference voltage. Bypass REF- with a 0.1µF capacitor to AGND. Also bypass REF- to REF+ with a 2.2µF and a 0.1µF capacitor.
24	D0	Digital Out Bit 0 of 14-Bit Parallel Data Bus. High impedance when $\overline{RD}$ = 1 or $\overline{CS}$ = 1.
25	D1	Digital Out Bit 1 of 14-Bit Parallel Data Bus. High impedance when $\overline{RD}$ = 1 or $\overline{CS}$ = 1.
26	D2	Digital Out Bit 2 of 14-Bit Parallel Data Bus. High impedance when $\overline{RD}$ = 1 or $\overline{CS}$ = 1.
27	D3	Digital Out Bit 3 of 14-Bit Parallel Data Bus. High impedance when $\overline{RD}$ = 1 or $\overline{CS}$ = 1.
28	D4	Digital Out Bit 4 of 14-Bit Parallel Data Bus. High impedance when $\overline{RD}$ = 1 or $\overline{CS}$ = 1.
29	D5	Digital Out Bit 5 of 14-Bit Parallel Data Bus. High impedance when $\overline{RD}$ = 1 or $\overline{CS}$ = 1.
30	D6	Digital Out Bit 6 of 14-Bit Parallel Data Bus. High impedance when $\overline{RD}$ = 1 or $\overline{CS}$ = 1.
31	D7	Digital Out Bit 7 of 14-Bit Parallel Data Bus. High impedance when $\overline{RD}$ = 1 or $\overline{CS}$ = 1.
32	D8	Digital Out Bit 8 of 14-Bit Parallel Data Bus. High impedance when $\overline{RD}$ = 1 or $\overline{CS}$ = 1.
33	D9	Digital Out Bit 9 of 14-Bit Parallel Data Bus. High impedance when $\overline{RD}$ = 1 or $\overline{CS}$ = 1.
34	D10	Digital Out Bit 10 of 14-Bit Parallel Data Bus. High impedance when $\overline{RD}$ = 1 or $\overline{CS}$ = 1.
35	D11	Digital Out Bit 11 of 14-Bit Parallel Data Bus. High impedance when $\overline{RD}$ = 1 or $\overline{CS}$ = 1.
36	D12	Digital Out Bit 12 of 14-Bit Parallel Data Bus. High impedance when $\overline{RD}$ = 1 or $\overline{CS}$ = 1.
37	D13	Digital Out Bit 13 of 14-Bit Parallel Data Bus. High impedance when $\overline{RD}$ = 1 or $\overline{CS}$ = 1.
38	DV_{DD}	Digital Supply Input. Apply +2.7V to +5.25V to DV_{DD}. Bypass DV_{DD} to DGND with a 0.1µF capacitor.
39	DGND	Digital Supply GND. DGND is the power return for DV_{DD}. Connect DGND to AGND at only one point (see the *Layout, Grounding, and Bypassing* section).
40	$\overline{EOC}$	End-of-Conversion Output. $\overline{EOC}$ goes low to indicate the end of a conversion. $\overline{EOC}$ returns high after one clock period.
41	$\overline{EOLC}$	End-of-Last-Conversion Output. $\overline{EOLC}$ goes low to indicate the end of the last conversion. $\overline{EOLC}$ returns high when CONVST goes low for the next conversion sequence. For the MAX1319/MAX1323/MAX1327, $\overline{EOLC}$ gives the same information as $\overline{EOC}$.
42	$\overline{RD}$	Read Input. Pulling $\overline{RD}$ low initiates a read command of the parallel data buses, D0–D13. D0–D13 are high impedance while either $\overline{RD}$ or $\overline{CS}$ is high.
43	I.C.2	Internally Connected 2. Connect I.C.2 to DV_{DD}.
44	$\overline{CS}$	Chip-Select Input. Pulling $\overline{CS}$ low activates the digital interface. D0–D13 are high impedance while either $\overline{CS}$ or $\overline{RD}$ is high.
45	CONVST	Convert-Start Input. Driving CONVST high places the device in hold mode and initiates the conversion process. The analog inputs are sampled on the rising edge of CONVST. When CONVST is low the analog inputs are tracked.
46	CLK	External-Clock Input. CLK accepts an external clock signal up to 15MHz. Connect CLK to DGND for internally clocked conversions. To select external clock mode, set INTCLK/$\overline{EXTCLK}$ = 0.
47	SHDN	Shutdown Input. Set SHDN = 0 for normal operation. Set SHDN = 1 for shutdown mode.
48	ALLON	ALLON is not implemented. Connect ALLON to DGND.

526ksps, Single-Channel, 14-Bit, Parallel-Interface ADCs

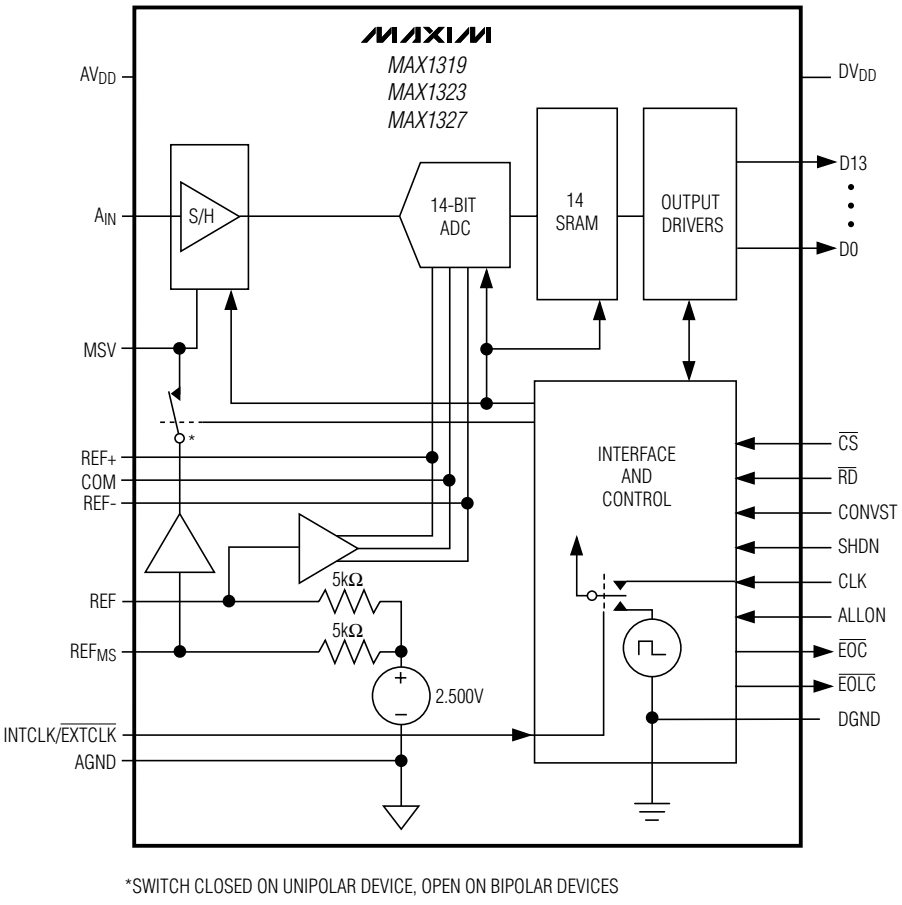


Figure 1. Functional Diagram

Detailed Description

The MAX1319/MAX1323/MAX1327 are 14-bit, 526ksps, 1.6µs conversion-time ADCs. These devices are available with 0 to +5V, ±5V, and ±10V input ranges. The 0 to +5V device features ±6V fault-tolerant inputs (see the *Typical Operating Circuits*). The ±5V and ±10V devices feature ±16.5V fault-tolerant inputs (see the *Typical Operating Circuits*). Internal or external reference, and clock capability offer great flexibility and ease of use. A 16.6MHz, 14-bit, parallel data bus outputs the conversion result. Figure 1 shows the functional diagram of these devices.

Analog Inputs

T/H

The time required for the T/H to acquire an input signal depends on the input source impedance. If the input signal's source impedance is high, the acquisition time lengthens and more time must be allowed between conversions. The acquisition time (t_{ACQ}) is the maximum time the device takes to acquire the signal. Use the following formula to calculate the acquisition time:

$$t_{ACQ} = 10 (R_S + R_{IN}) \times 6pF$$

where R_{IN} = 2.2kΩ, R_S = the input signal's source impedance, and t_{ACQ} is never less than 180ns. A source impedance of less than 100Ω does not significantly affect the ADC's performance.

To improve the input signal bandwidth under AC conditions, drive the input with a wideband buffer (>50MHz) that can drive the ADC's input capacitance and settle quickly. For example, the MAX4265 can be used for +5V unipolar devices, or the MAX4350 can be used for ±5V bipolar inputs.

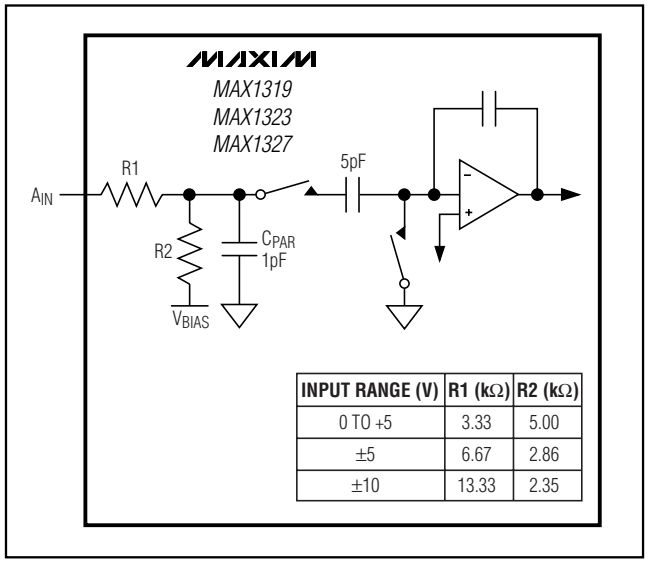
The T/H aperture delay is typically 13ns. Figure 2 shows a simplified equivalent input circuit, illustrating the ADC's sampling architecture.

Input Bandwidth

The input tracking circuitry has a 10MHz small-signal bandwidth, making it possible to digitize high-speed transient events and measure periodic signals with bandwidths exceeding the ADC's sampling rate by using undersampling techniques. To avoid high frequency signals being aliased into the frequency band of interest, anti-alias filtering is recommended.

Input Range and Protection

These devices provide ±10V, ±5V or 0 to +5V analog input voltage ranges. Figure 2 shows the typical input circuit. Overvoltage protection circuitry at the analog input provides ±16.5V fault protection for the bipolar input devices and ±6.0V fault protection for the unipolar input device. This fault protection circuit limits the current going into or out of the device to less than 50mA, providing an added layer of protection from momentary overvoltage or undervoltage conditions at the analog input.



INPUT RANGE (V)	R1 (kΩ)	R2 (kΩ)
0 TO +5	3.33	5.00
±5	6.67	2.86
±10	13.33	2.35

Figure 2. Typical Input Circuit

Power-Saving Modes

Shutdown Mode

During shutdown, the analog and digital circuits in the device power down and the device draws less than 100µA from AV_{DD}, and less than 100µA from DV_{DD}. Select shutdown mode using the SHDN input. Set SHDN high to enter shutdown mode. After coming out of shutdown, allow the 1ms wake-up before making the first conversion. When using an external clock, apply at least 20 clock cycles with CONVST high before making the first conversion. When using internal clock mode, wait at least 2µs before making the first conversion.

Clock Modes

These devices provide an internal clock of 10MHz (typ). Alternatively, an external clock can be used.

Internal Clock

Internal clock mode frees the microprocessor from the burden of running the ADC conversion clock. For internal clock operation, connect INTCLK/$\overline{\text{EXTCLK}}$ to AV_{DD} and connect CLK to DGND.

External Clock

For external clock operation, connect INTCLK/$\overline{\text{EXTCLK}}$ to AGND and connect an external clock source to CLK. Note that INTCLK/$\overline{\text{EXTCLK}}$ is referenced to the analog power supply, AV_{DD}. The external clock frequency can be up to 15MHz, with a duty cycle between 30% and 70%. Clock frequencies of 100kHz and lower can be used, but the droop in the T/H circuits reduces linearity.

Selecting an Input Buffer

Most applications require an input buffer to achieve 14-bit accuracy. Although slew rate and bandwidth are important, the most critical specification is settling time. The sampling requires a relatively brief sampling interval of 150ns. At the beginning of the acquisition, the internal sampling capacitor array connects to the amplifier output, causing some output disturbance. Ensure the amplifier is capable of settling to at least 14-bit accuracy during this interval. Use a low-noise, low-distortion, wideband amplifier (such as the MAX4330 or MAX4265), which settles quickly and is stable with the ADC's capacitive load (in parallel with any bypass capacitors on the analog inputs).

526ksps, Single-Channel, 14-Bit, Parallel-Interface ADCs

Applications Information

Digital Interface

The parallel digital interface outputs the 14-bit conversion result. The interface includes the following control signals: chip select ($\overline{CS}$), read ($\overline{RD}$), end of conversion ($\overline{EOC}$), end of last conversion ($\overline{EOLC}$), convert start (CONVST), shutdown (SHDN), all on (ALLON), internal clock select (INTCLK /$\overline{EXTCLK}$), and external clock input (CLK). Figures 3 and 4, Table 1, and the *Timing Characteristics* table show the operation of the interface. The parallel interface goes high impedance when $\overline{RD}$ = 1 or $\overline{CS}$ = 1.

Starting a Conversion

To start a conversion using internal clock mode, pull CONVST low for at least the acquisition time (t_{ACQ}). The T/H acquires the signal while CONVST is low, and conversion begins on the rising edge of CONVST. The end-of-conversion signal ($\overline{EOC}$) or the end-of-last-conversion signal ($\overline{EOLC}$) pulses low when the conversion result is available (Figure 3).

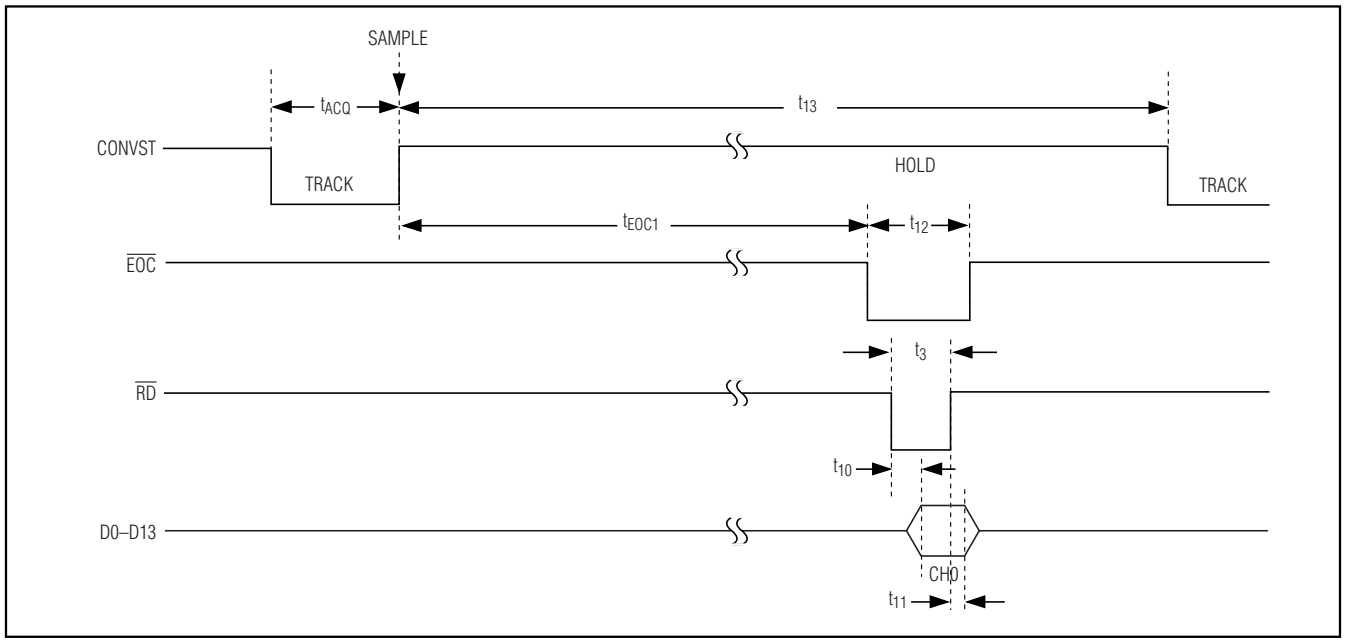


Figure 3. Reading a Conversion—Internal Clock

Table 1. Reference Bypass Capacitors

LOCATION	INPUT VOLTAGE RANGE	
	UNIPOLAR (µF)	BIPOLAR (µF)
MSV Bypass Capacitor to AGND	2.2 ll 0.1	NA
REF_{MS} Bypass Capacitor to AGND	0.01	0.01
REF Bypass Capacitor to AGND	0.01	0.01
REF+ Bypass Capacitor to AGND	0.1	0.1
REF+ to REF- Capacitor	2.2 ll 0.1	2.2 ll 0.1
REF- Bypass Capacitor to AGND	0.1	0.1
COM Bypass Capacitor to AGND	2.2 ll 0.1	2.2 ll 0.1

NA = Not applicable (connect MSV directly to AGND).

To start a conversion using external clock mode, pull CONVST low for at least the acquisition time (t_{ACQ}). The T/H acquires the signal while CONVST is low, and conversion begins on the rising edge of CONVST. Apply an external clock to the CLK pin. To avoid T/H droop degrading the sampled analog input signals, the first clock pulse should occur within 10µs from the rising edge of CONVST, and have a minimum clock frequency of 100kHz. The conversion result is available for read on the rising edge of the 17th clock cycle (Figure 4).

In both internal and external clock modes, CONVST must be held high until the last conversion result is read. For best operation, the rising edge of CONVST must be a clean, high-speed, low-jitter digital signal.

It is necessary to have a period of inactivity on the digital bus during signal aquisition. t_{QUIET} is the period between the $\overline{RD}$ rising edge and the falling edge of CONVST shown in Figure 4. Allow a minimum of 50ns for t_{QUIET}.

Reading a Conversion Result

Reading During a Conversion

Figures 3 and 4 show the interface signals for initiating a read operation during a conversion cycle. $\overline{CS}$ can be low at all times; it can be low during the $\overline{RD}$ cycles, or it can be the same as $\overline{RD}$.

After initiating a conversion by bringing CONVST high, wait for $\overline{EOC}$ or $\overline{EOLC}$ to go low (about 1.6µs in internal clock mode or 17 clock cycles in external clock mode) before reading the first conversion result. Read the conversion result by bringing $\overline{RD}$ low and latching the data to the parallel digital-output bus. Bring $\overline{RD}$ high to release the digital bus.

Power-Up Reset

After applying power, allow the 1.0ms wake-up time to elapse before initiating the first conversion. If using an external clock, apply 20 clock pulses to CLK with CONVST high before initiating the first conversion. If using an internal clock, hold CONVST high for at least 2.0µs after the wake-up time is complete.

Reference

Internal Reference

The internal reference circuits provide for analog input voltages of 0 to +5V unipolar (MAX1319), ±5V bipolar (MAX1323) or ±10V bipolar (MAX1327). Install external capacitors for reference stability, as indicated in Table 1, and as shown in the *Typical Operating Circuits*.

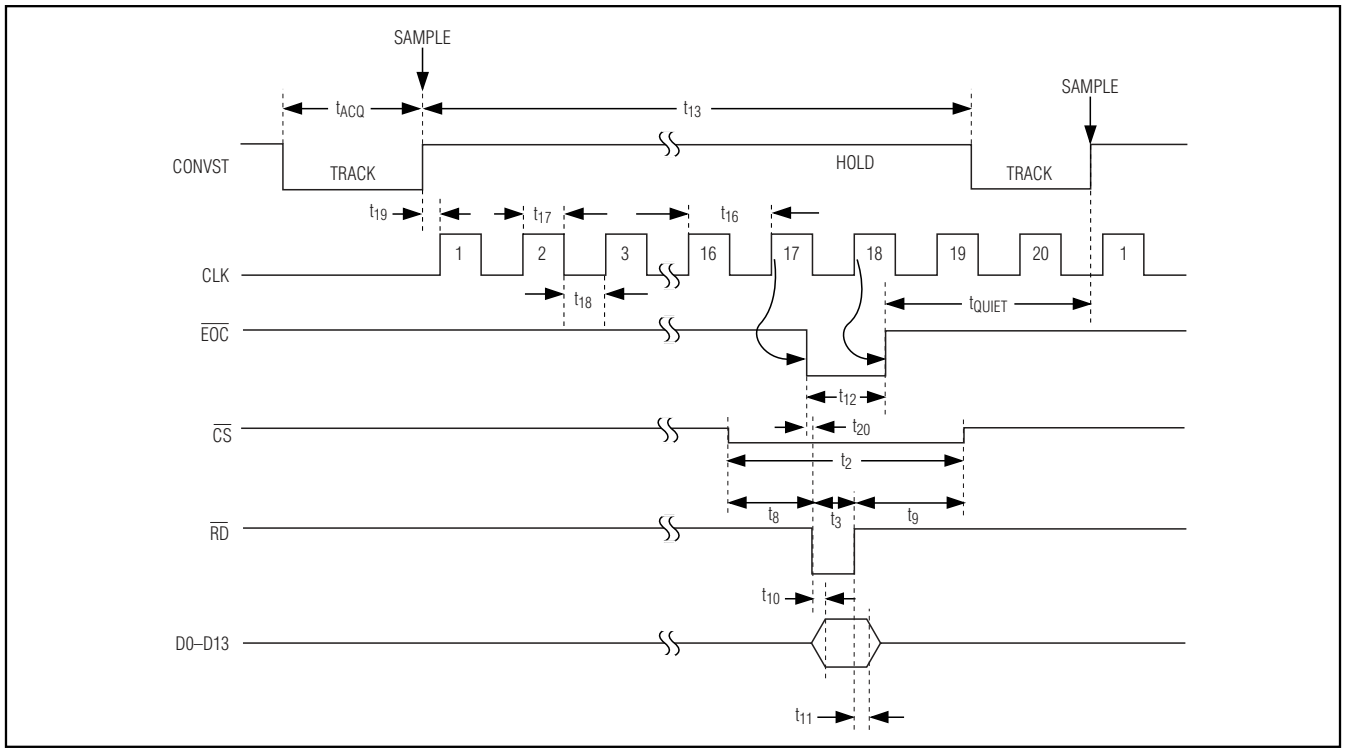


Figure 4. Reading a Conversion—External Clock

526ksps, Single-Channel, 14-Bit, Parallel-Interface ADCs

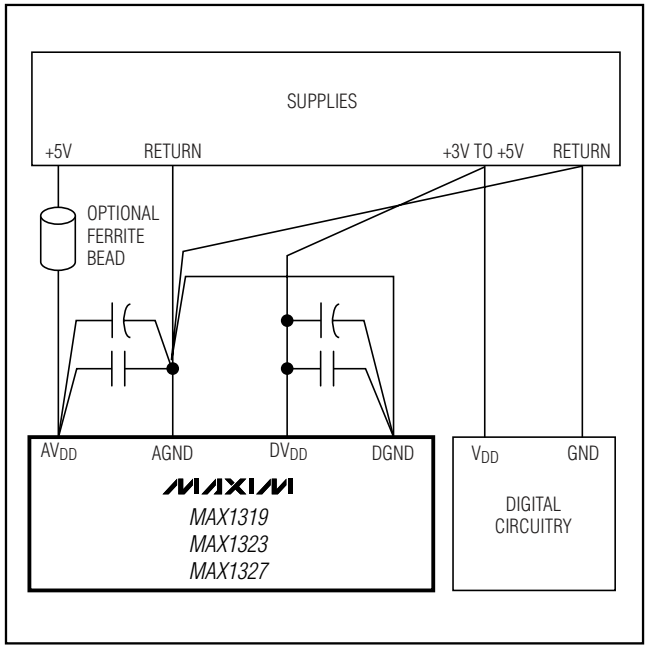


Figure 5. Power-Supply Grounding and Bypassing

External Reference

Connect a +2.0V to +3.0V external reference at REF_{MS} and/or REF. When connecting an external reference, the input impedance is typically 5kΩ. The external reference must be able to drive 200µA of current and be less than 3Ω output impedance. For more information about using external references see the *Transfer Functions* section.

Layout, Grounding, and Bypassing

For best performance use PC boards. Board layout should ensure that digital and analog signal lines are separated from each other. Do not run analog and digital lines parallel to one another (especially clock lines), or do not run digital lines underneath the ADC package. Figure 5 shows the recommended system ground connections. A single-point analog ground (star ground point) should be established at AGND, separate from the logic ground. All other analog grounds and DGND should be connected to this ground. No other digital system ground should be connected to this single-point analog ground. The ground return to the power supply for this ground should be low impedance and as short as possible for noise-free operation. High-frequency noise in the V_{DD} power supply may affect the high-speed comparator in the ADC. Bypass these supplies to the single-point analog ground with 0.1µF and 2.2µF bypass capacitors close to the device. If the +5V power supply is very noisy, a ferrite bead can be connected as a lowpass filter, as shown in Figure 5.

Transfer Functions

Bipolar ±10V Device

Table 2 and Figure 6 show the two's complement transfer function for the MAX1327 with a ±10V input range. The full-scale input range (FSR) is eight times the voltage at REF. The internal +2.500V reference gives a +20V FSR, while an external +2V to +3V reference allows an FSR of +16V to +24V, respectively. Calculate the LSB size using the following equation:

$$1\ LSB = \frac{8 \times V_{REFADC}}{2^{14}}$$

This equals 1.2207mV with a +2.5V internal reference.

The input range is centered about V_{MSV}. Normally, MSV = AGND, and the input is symmetrical at about zero. For a custom midscale voltage, drive MSV with an external voltage source. Noise present on MSV directly couples into the ADC result. Use a precision, low-drift voltage reference with adequate bypassing to prevent MSV from degrading ADC performance. For maximum full-scale range, be careful not to violate the absolute maximum voltage ratings of the analog inputs when choosing MSV.

Determine the input voltage as a function of V_{REF}, V_{MSV}, and the output code in decimal using the following equation:

$$V_{CH\_} = LSB \times CODE_{10} + V_{MSV}$$

Bipolar ±5V Device

Table 3 and Figure 7 show the two's complement transfer function for the MAX1323 with a ±5V input range. The FSR is four times the voltage at REF. The internal +2.500V reference gives a +10V FSR, while an external +2V to +3V reference allows an FSR of +8V to +12V, respectively. Calculate the LSB size using the following equation:

$$1\ LSB = \frac{4 \times V_{REFADC}}{2^{14}}$$

This equals 0.6104mV when using the internal reference.

The input range is centered about V_{MSV}. Normally, MSV = AGND, and the input is symmetrical at about zero. For a custom midscale voltage, drive MSV with an external voltage source. Noise present on MSV directly couples into the ADC result. Use a precision, low-drift voltage reference with adequate bypassing to prevent MSV from degrading ADC performance. For maximum full-scale range, be careful not to violate the absolute

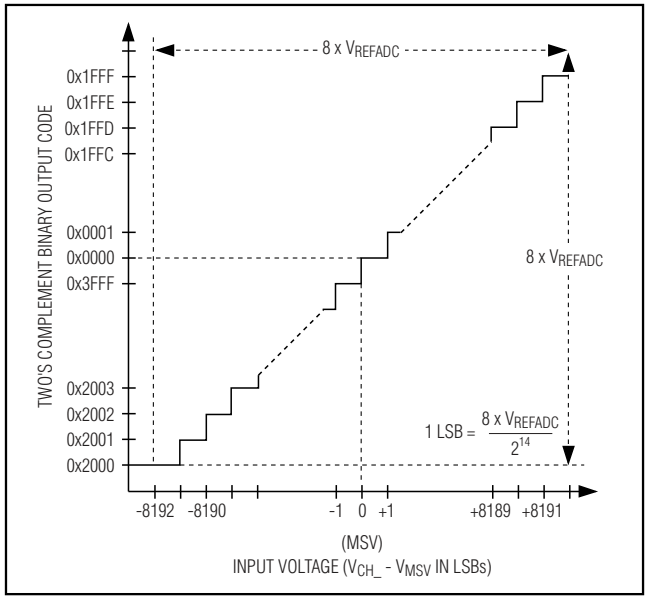


Figure 6. ±10V Bipolar Transfer Function

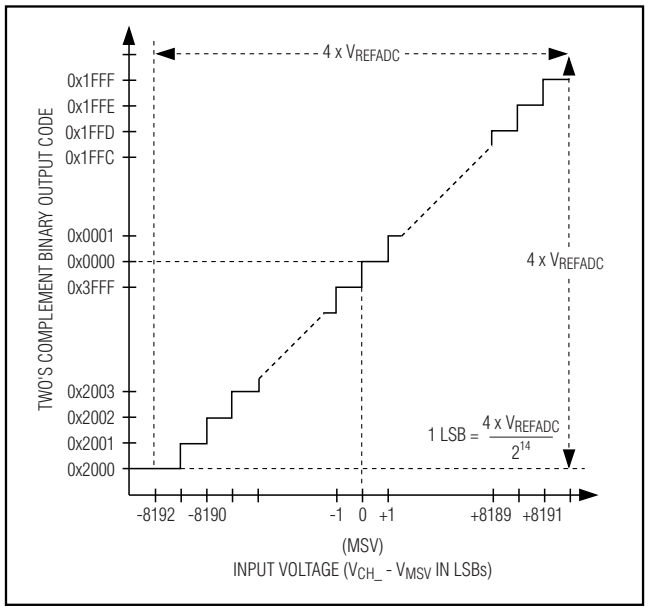


Figure 7. ±5V Bipolar Transfer Function

maximum voltage ratings of the analog inputs when choosing MSV. Determine the input voltage as a function of V_{REF}, V_{MSV}, and the output code in decimal using the following equation:

$$V_{CH\_} = LSB \times CODE_{10} + V_{MSV}$$

Table 2. ±10V Bipolar Code Table

TWO'S COMPLEMENT BINARY OUTPUT CODE	DECIMAL EQUIVALENT OUTPUT ($CODE_{10}$)	INPUT VOLTAGE (V) (V_{REF} = 2.5V, V_{MSV} = 0V)
01 1111 1111 1111 → 0x1FFF	8191	9.9988
01 1111 1111 1110 → 0x1FFE	8190	9.9976
00 0000 0000 0001 → 0x0001	1	0.0012
00 0000 0000 0000 → 0x0000	0	0
11 1111 1111 1111 → 0x3FFF	-1	-0.0012
10 0000 0000 0001 → 0x2001	-8191	-9.9988
10 0000 0000 0000 → 0x2000	-8192	-10.0000

Table 3. ±5V Bipolar Code Table

TWO'S COMPLEMENT BINARY OUTPUT CODE	DECIMAL EQUIVALENT OUTPUT ($CODE_{10}$)	INPUT VOLTAGE (V) (V_{REF} = 2.5V, V_{MSV} = 0V)
01 1111 1111 1111 → 0x1FFF	8191	4.9994
01 1111 1111 1110 → 0x1FFE	8190	4.9988
00 0000 0000 0001 → 0x0001	1	0.0006
00 0000 0000 0000 → 0x0000	0	0
11 1111 1111 1111 → 0x3FFF	-1	-0.0006
10 0000 0000 0001 → 0x2001	-8191	-4.9994
10 0000 0000 0000 → 0x2000	-8192	-5.0000

Table 4. 0 to +5V Unipolar Code Table

BINARY OUTPUT CODE	DECIMAL EQUIVALENT OUTPUT ($CODE_{10}$)	INPUT VOLTAGE (V) (V_{REF} = V_{REFMS} = 2.5V)
11 1111 1111 1111 → 0x3FFF	16383	4.9997
11 1111 1111 1110 → 0x3FFE	16382	4.9994
10 0000 0000 0001 → 0x2001	8193	2.5003
10 0000 0000 0000 → 0x2000	8192	2.5000
01 1111 1111 1111 → 0x1FFF	8191	2.4997
00 0000 0000 0001 → 0x0001	1	0.0003
00 0000 0000 0000 → 0x0000	0	0

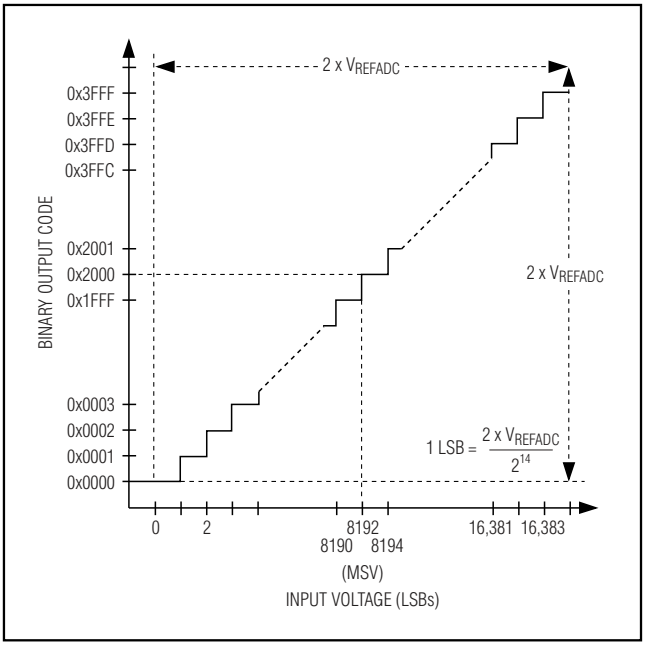


Figure 8. 0 to +5V Unipolar Transfer Function

Unipolar 0 to +5V Device

Table 4 and Figure 8 show the offset binary transfer function for the MAX1319 with a 0 to +5V input range. The FSR is two times the voltage at REF. The internal +2.500V reference gives a +5V FSR, while an external +2V to +3V reference allows an FSR of +4V to +6V, respectively. Calculate the LSB size using the following equation:

$$1\ LSB = \frac{2 \times V_{REFADC}}{2^{14}}$$

This equals 0.3052mV when using the internal reference.

The input range is centered about V_{MSV}, which is internally set to +2.500V. For a custom midscale voltage, drive REF_{MS} with an external voltage source and MSV will follow REF_{MS}. Noise present on MSV or REF_{MS} directly couples into the ADC result. Use a precision, low-drift voltage reference with adequate bypassing to prevent MSV from degrading ADC performance. For maximum full-scale range, be careful not to violate the absolute maximum voltage ratings of the analog inputs when choosing MSV. Determine the input voltage as a function of V_{REF}, V_{MSV}, and the output code in decimal using the following equation:

$$V_{CH\_} = LSB \times CODE_{10} + (V_{MSV} - 2.500V)$$

Definitions

Integral Nonlinearity (INL)

Integral nonlinearity is the deviation of the values on an actual transfer function from a straight line. For these devices this straight line is a line drawn between the endpoints of the transfer function, once offset and gain errors have been nullified.

Differential Nonlinearity (DNL)

Differential nonlinearity is the difference between an actual step width and the ideal value of 1 LSB. For these devices, the DNL of each digital output code is measured and the worst-case value is reported in the *Electrical Characteristics* table. A DNL error specification of less than ±1 LSB guarantees no missing codes and a monotonic transfer function.

Unipolar Offset Error

For the unipolar MAX1319, the ideal midscale transition from 0x1FFF to 0x2000 occurs at MSV (see Figure 8). The unipolar offset error is the amount of deviation between the measured midscale transition point and the ideal midscale transition point.

Bipolar Offset Error

For the bipolar MAX1323/MAX1327, the ideal zero-point transition from 0x3FFF to 0x0000 occurs at MSV, which is usually connected to ground (see Figures 6 and 7). The bipolar offset error is the amount of deviation between the measured zero-point transition and the ideal zero-point transition.

Gain Error

The ideal full-scale transition from 0x1FFE to 0x1FFF occurs at 1 LSB below full scale (see the *Transfer Functions* section). The gain error is the amount of deviation between the measured full-scale transition point and the ideal full-scale transition point, once offset error has been nullified.

Signal-to-Noise Ratio

For a waveform perfectly reconstructed from digital samples, signal-to-noise ratio (SNR) is the ratio of the full-scale analog input (RMS value) to the RMS quantization error (residual error). The ideal, theoretical minimum analog-to-digital noise is caused by quantization noise error only and results directly from the ADC's resolution (N bits):

$$SNR = (6.02 \times N + 1.76)dB$$

where N = 14 bits.

In reality, there are other noise sources besides quantization noise; thermal noise, reference noise, clock jitter, etc. SNR is computed by taking the ratio of the RMS signal to the RMS noise, which includes all spectral components minus the fundamental, the first five harmonics, and the DC offset.

Signal-to-Noise Plus Distortion

Signal-to-noise plus distortion (SINAD) is the ratio of the fundamental input frequency's RMS amplitude to the RMS equivalent of all the other ADC output signals.

$$SINAD(dB) = 20 \times \log\left[\frac{Signal_{RMS}}{(Noise + Distortion)_{RMS}}\right]$$

Effective Number of Bits

Effective number of bits (ENOB) indicates the global accuracy of an ADC at a specific input frequency and sampling rate. An ideal ADC's error consists of quantization noise only. With an input range equal to the full-scale range of the ADC, calculate the ENOB as follows:

$$ENOB = \frac{SINAD - 1.76}{6.02}$$

Total Harmonic Distortion

Total harmonic distortion (THD) is the ratio of the RMS sum of the first five harmonics of the input signal to the fundamental itself. This is expressed as:

$$THD = 20 \times \log\left[\frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2}}{V_1}\right]$$

where V_1 is the fundamental amplitude and V_2 through V_5 are the 2nd- through 5th-order harmonics.

Spurious-Free Dynamic Range

Spurious-free dynamic range (SFDR) is the ratio of the RMS amplitude of the fundamental (maximum signal component) to the RMS value of the next largest frequency component.

Aperature Delay

Aperture delay (t_{AD}) is the time delay from the sampling clock edge to the instant when an actual sample is taken.

Aperture Jitter

Aperture Jitter (t_{AJ}) is the sample-to-sample variation in aperture delay.

Small-Signal Bandwidth

A small -20dBFS analog input signal is applied to an ADC in a manner that ensures that the signal's slew rate does not limit the ADC's performance. The input frequency is then swept up to the point where the amplitude of the digitized conversion result has decreased by -3dB.

Full-Power Bandwidth

A large -0.5dBFS analog input signal is applied to an ADC, and the input frequency is swept up to the point where the amplitude of the digitized conversion result has decreased by -3dB. This point is defined as full-power input bandwidth frequency.

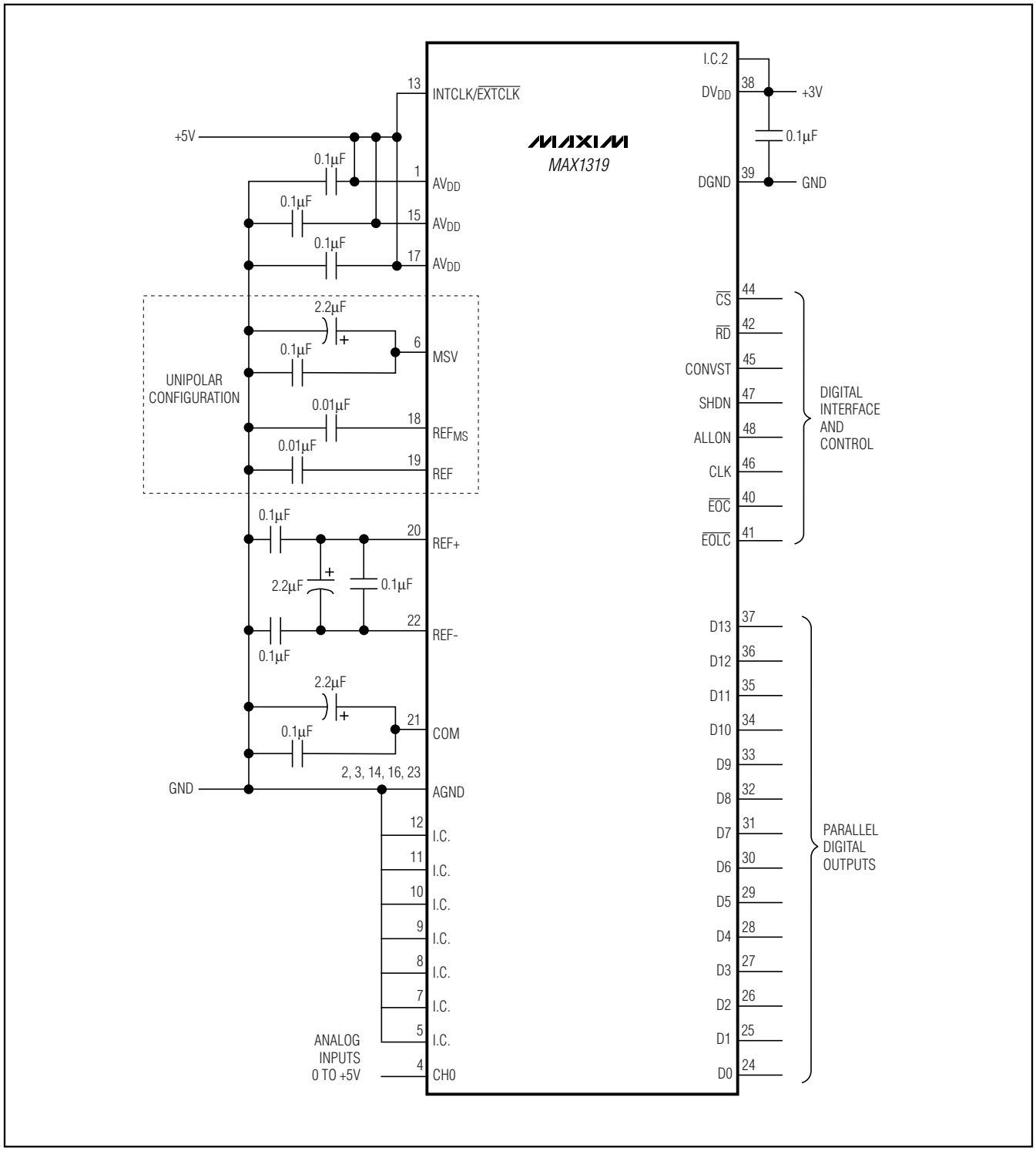
Chip Information

TRANSISTOR COUNT: 80,000

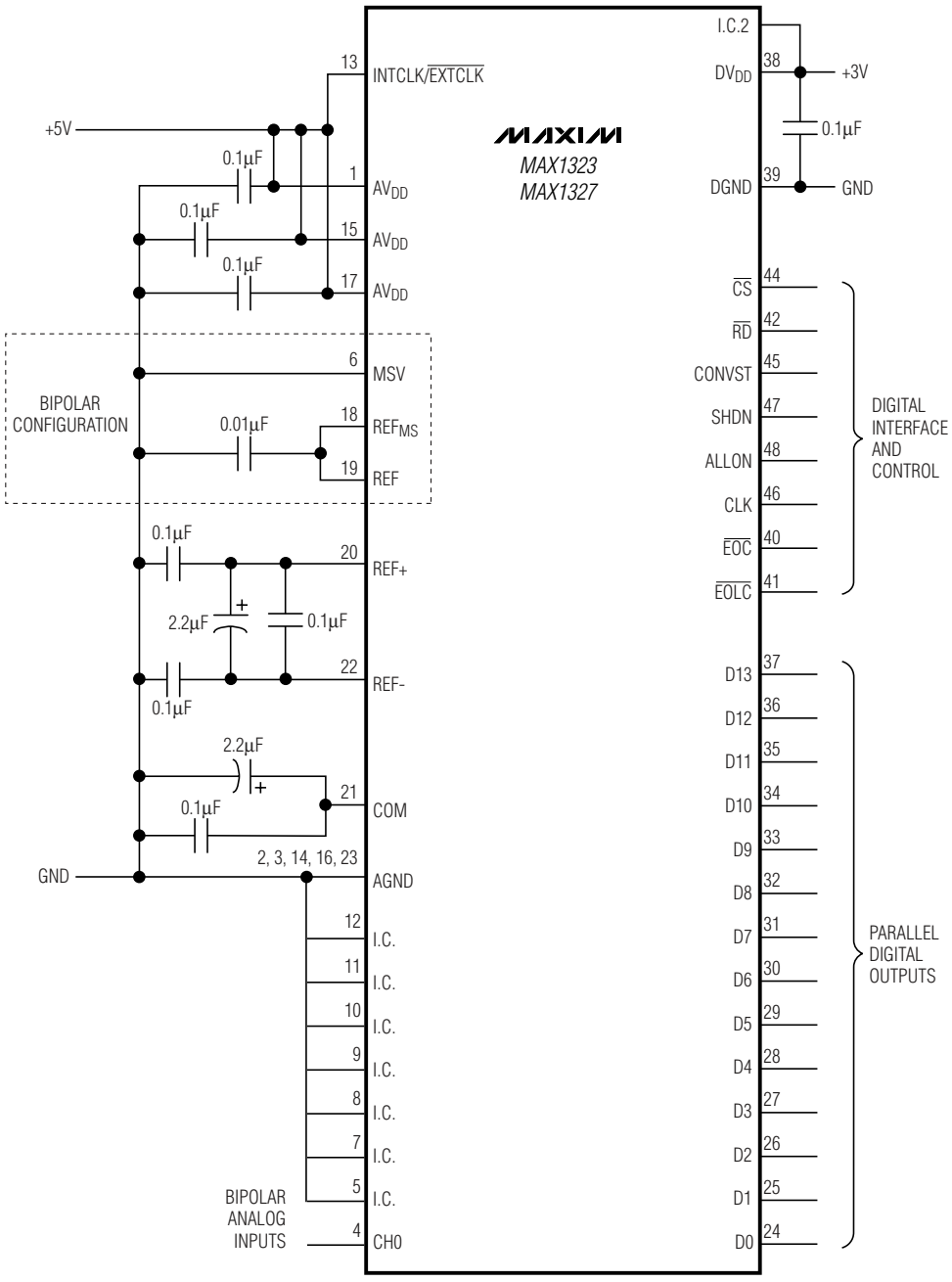
PROCESS: 0.6µm BiCMOS

526ksps, Single-Channel, 14-Bit, Parallel-Interface ADCs

Typical Operating Circuits



Typical Operating Circuits (continued)

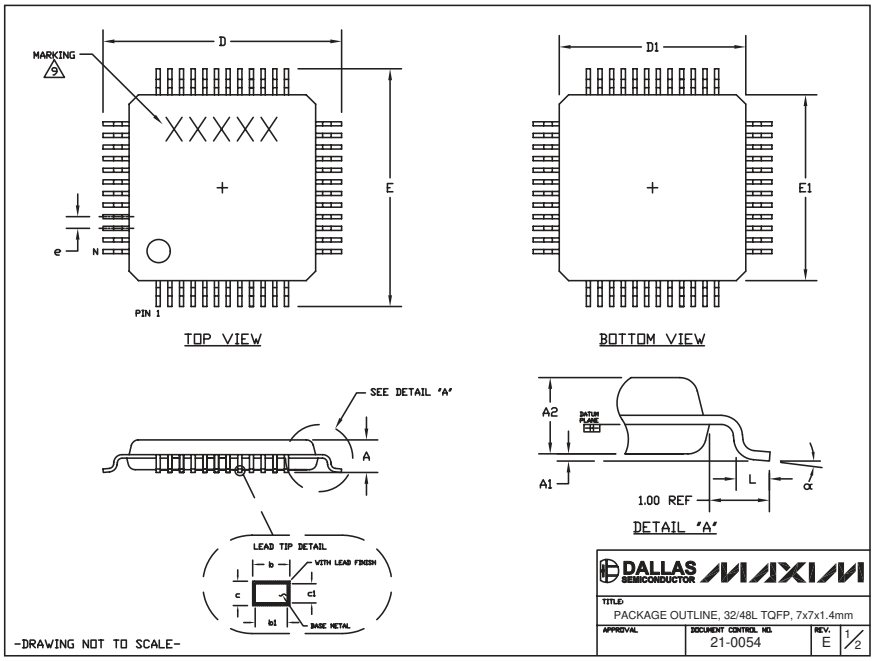


526ksps, Single-Channel, 14-Bit, Parallel-Interface ADCs

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

32L/48L TQFP.EPS



NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5-1982.
2. DATUM PLANE ⊟ IS LOCATED AT MOLD PARTING LINE AND COINCIDENT WITH LEAD, WHERE LEAD EXITS PLASTIC BODY AT BOTTOM OF PARTING LINE.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.25 MM ON D1 AND E1 DIMENSIONS.
4. THE TOP OF PACKAGE IS SMALLER THAN THE BOTTOM OF PACKAGE BY 0.15 MILLIMETERS.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. ALL DIMENSIONS ARE IN MILLIMETERS.
7. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95, REGISTRATION MS-026.
8. LEADS SHALL BE COPLANAR WITHIN .004 INCH.
9. MARKING SHOWN IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
10. NUMBER OF LEADS ARE SHOWN FOR REFERENCE ONLY.

JEDEC VARIATION				
	BBA		BBC	
	MIN.	MAX.	MIN.	MAX.
A	--	1.60	--	1.60
A_1	0.05	0.15	0.05	0.15
A_2	1.35	1.45	1.35	1.45
D	8.90	9.10	8.90	9.10
D_1	6.90	7.10	6.90	7.10
E	8.90	9.10	8.90	9.10
E_1	6.90	7.10	6.90	7.10
e	0.8 BSC.		0.5 BSC.	
L	0.45	0.75	0.45	0.75
b	0.30	0.45	0.17	0.27
b1	0.30	0.40	0.17	0.23
c	0.09	0.20	0.09	0.20
c1	0.09	0.16	0.09	0.16
N	32		48	
α	0°	7°	0°	7°

-DRAWING NOT TO SCALE-
DALLAS SEMICONDUCTOR MAXIM
TITLE: PACKAGE OUTLINE, 32/48L TQFP, 7x7x1.4mm
APPROVAL
DOCUMENT CONTROL NO. 21-0054
REV. E
2/2