Structure Silicon Monolithic Integrated Circuit

Product name Power management IC for cellular phone

Type **BH6053GU**

Features Switching regulator
Including 5 channel regulator

○ Absolute maximum ratings (Ta=25°C)

Parameter	Symbol	Limit	Symbol	Condition
Maximum applied voltage	VCC	7.0	V	
Power dissipation	Pd	1350 (*1)	mW	At single unit
Operating temperature range	Topr	-30 ~+75	°C	
Storage temperature range	Tstr	-55 ~ +125	°C	

(*1) 50mm×58mm×1.75mm At glass epoxy board mounting.
When it's used by more than Ta=25 °C, it's reduced by 13.5mW/°C.

○ Recommended operating range(Ta=-30 °C~+75 °C)

Parameter	Symbol	Limit			Unit	Condition
		Min.	Typ.	Max.		
Power supply voltage	VCC	3.0	3.6	4.5	V	REG1I~5I, BATP voltage

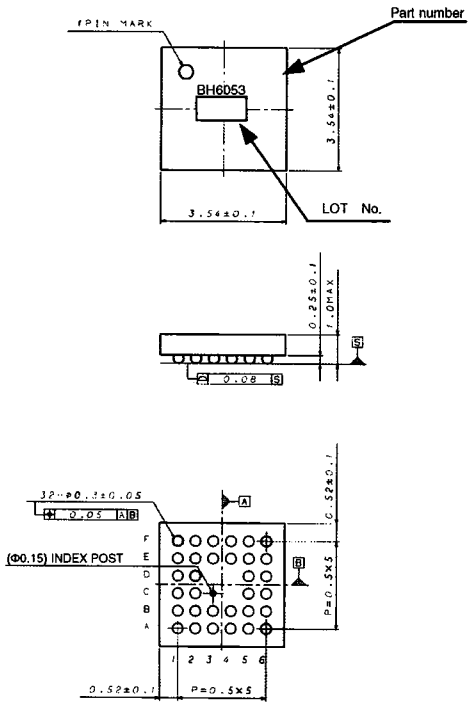
This chip is not designed to protect itself against radioactive rays.

○Electrical characteristic

Unless otherwise specified Ta=25 °C, VCC=REG1I=REG23I=REG4I=BATP=REG5I=3.6V

Parameter		Symbol	Spec			Unit	Condition
			Min.	Typ.	Max.		
Circuit current (No load)							
Circuit current 1		ICC1	-	9.1	14.0	μA	CNT1,2,3,4,5 SWEN=0V (Operated only reference voltage source)
Circuit current 2		ICC2	-	4.2	5.7	mA	CNT1,2,3,4,5=0V, SWEN,MODE=2.8V
Circuit current 3		ICC3	-	25	42.4	μA	CNT1,2,3,4,5=0V,SWEN=2.8V, MODE=0V
SWREG1							
1.5V Output voltage range	SW mode	Vosw1	1.450	1.500	1.550	V	Io=400mA,MODE=3.6V,SWVSEL=0V
	LDO mode	Voldo1	1.450	1.500	1.550	V	Io=50mA,MODE=0V,SWVSEL=0V
1.2V Output voltage range	SW mode	Vosw2	1.150	1.200	1.250	V	Io=400mA,MODE=3.6V, SWVSEL=3.6V
	LDO mode	Voldo2	1.150	1.200	1.250	V	Io=50mA,MODE=0V,SWVSEL=3.6V
Oscillator frequency		Fosc	0.78	1.05	1.35	MHz	SW mode
REG1							
2.6V Output voltage		Vo1	2.544	2.600	2.656	V	Io=150mA,REG1VSEL=0V
2.85V Output voltage		Vo2	2.794	2.850	2.906	V	Io=150mA,REG1VSEL=3.6V
Output current		Io	200	-	-	mA	
REG2							
Output voltage		Vo	1.755	1.800	1.845	V	Io=120mA
Output current		Io	150	-	-	mA	
REG3							
Output voltage		Vo	3.240	3.300	3.360	V	Io=150mA
Output current		Io	150	-	-	mA	
REG4							
Output voltage		Vo	1.755	1.800	1.845	V	Io=50mA
Output current		Io	50	-	-	mA	
REG5							
Output voltage		Vo1	1.460	1.500	1.540	V	Io=30mA,SWVSEL=0V
Output voltage		Vo2	1.160	1.200	1.240	V	Io=30mA,SWVSEL=3.6V
Output current		Io	50	-	-	mA	
CPU I/F 1 (CNT1,2,3,4,5,SWEN,MODE)							
Input current H level		IIH1	-10	1.95	10	μA	VIH=3.6V
Input current L level		IIL1	-10	0	10	μA	VIL=0V
CPU I/F 2 (SWVSEL,REG1VSEL)							
Input current H level		IIH2	-10	0	10	μA	VIH=3.6V
Input current L level		IIL2	-10	0	10	μA	VIL=0V
CPU I/F 3 (CNT1,2,3,4,5,SWEN,MODE)							
Input voltage H level		VIH	1.4	-	-	V	
Input voltage L level		VIL	-	0	0.25	V	
CPU I/F 4 (SWVSEL,REG1VSEL)							
Input voltage H level		VIH	VCCx0.8	-	VCC	V	
Input voltage L level		VIL	-	-	VCCx0.2	V	
UVLO (Under Voltage Lock Out)							
Detect voltage 1		VDETHL	2.4	2.5	2.6	V	VCC=3.6→0V SWEEP
Hystelisys		VHYS	25	50	100	mV	

○Dimensions diagram, Marking diagram

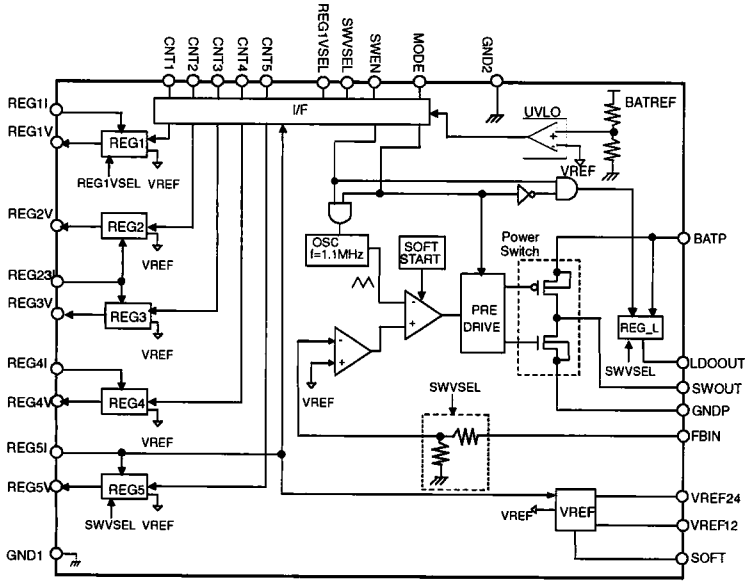


VCSP85H3(32 pin) (unit:mm)

○Pin assignment table

PIN	Pin name.	PIN	Pin name
B5	REG1I	A2	FBIN
A4	REG1V	B3	SOFT
A5	REG2V	A3	MODE
B6	REG23I	B4	SWEN
C6	REG3V	E4	CNT1
E2	REG4I	F3	CNT2
E1	REG4V	E3	CNT3
D6	REG5V	F2	CNT4
F4	VREF24	E6	CNT5
F5	VREF12	C5	REG5I
D5	GND1	D2	SWVSEL
D1	GND2	E5	REG1VSEL
B2	GNDP	A1	T1
B1	SWOUT	A6	T2
C2	BATP	F6	T3
C1	LDOOUT	F1	T4

○ Block diagram



○ Cautions on use

(1) Absolute Maximum Ratings

An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down devices, thus making Impossible to identify breaking mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.

(2) Power supply and GND line

Design PCB pattern to provide low impedance for the wiring between the power supply and the GND lines. Pay attention to the interference by common impedance of layout pattern when there are plural power supplies and GND lines. Especially, when there are GND pattern for small signal and GND pattern for large current included the external circuits, please separate each GND pattern. Furthermore, for all power supply terminals to ICs, mount a capacitor between the power supply and the GND terminal. At the same time, in order to use a capacitor, thoroughly check to be sure the characteristics of the capacitor to be used present no problem including the occurrence of capacity dropout at a low temperature, thus determining the constant.

(3) GND voltage

Make setting of the potential of the GND terminal so that it will be maintained at the minimum in any operating state. Furthermore, check to be sure no terminals are at a potential lower than the GND voltage including an actual electric transient.

(4) Short circuit between terminals and erroneous mounting

In order to mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between terminals or between the terminal and the power supply or the GND terminal, the ICs can break down.

(5) Operation in strong electromagnetic field

Be noted that using ICs in the strong electromagnetic field can malfunction them.

(6) Input terminals

In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the input terminal. Therefore, pay thorough attention not to handle the input terminals, such as to apply to the input terminals a voltage lower than the GND respectively, so that any parasitic element will operate. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply to the input terminals a voltage lower than the power supply voltage or within the guaranteed value of electrical characteristics.

(7) External capacitor

In order to use a ceramic capacitor as the external capacitor, determine the constant with consideration given to a degradation in the nominal capacitance due to DC bias and changes in the capacitance due to temperature, etc.

(8) Thermal shutdown circuit (TSD)

When junction temperatures become 150°C (typ) or higher, the thermal shutdown circuit operates and turns a switch OFF. The thermal shutdown circuit, which is aimed at isolating the LSI from thermal runaway as much as possible, is not aimed at the protection or guarantee of the LSI. Therefore, do not continuously use the LSI with this circuit operating or use the LSI assuming its operation.

(9) Thermal design

Perform thermal design in which there are adequate margins by taking into account the permissible dissipation (Pd) in actual states of use.

(10) LDO

Use each output of LDO by the independence. Don't use under the condition that each output is short-circuited because it has the possibility that the operation becomes unstable.

(11) DC/DC converter

Select the low DCR inductors to decrease power loss for DC/DC converter.

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As of 18th. April 2005