Low Voltage 1:20 Differential ECL/PECL/HSTL Clock Fanout Buffer

MC100ES6221

PRODUCT DISCONTINUATION NOTICE - LAST TIME BUY EXPIRES (JUNE 30, 2014)

The MC100ES6221 is a bipolar monolithic differential clock fanout buffer. Designed for most demanding clock distribution systems, the MC100ES6221 supports various applications that require the distribution of precisely aligned differential clock signals. Using SiGe technology and a fully differential architecture, the device offers very low skew outputs and superior digital signal characteristics. Target applications for this clock driver is high performance clock distribution in computing, networking and telecommunication systems.

LOW VOLTAGE DUAL 1:20 DIFFERENTIAL ECL/PECL/HSTL CLOCK FANOUT BUFFER

TB SUFFIX
52-LEAD LQFP PACKAGE
EXPOSED PAD
CASE 1336A-01

AE SUFFIX
52-LEAD LQFP PACKAGE
Pb-FREE PACKAGE
CASE 1336A-01

Features

- 1:20 differential clock fanout buffer
- 100 ps maximum device skew
- SiGe technology
- Supports DC to 2 GHz operation of clock or data signals
- ECL/PECL compatible differential clock outputs
- ECL/PECL/HSTL compatible differential clock inputs
- Single 3.3 V, –3.3 V, 2.5 V or –2.5 V supply
- Standard 52 lead LQFP package with exposed pad for enhanced thermal characteristics
- Supports industrial temperature range
- Pin and function compatible to the MC100EP221
- 52-lead Pb-free Package Available

  Use replacement part: 8T33FS6221

Functional Description

The MC100ES6221 is designed for low skew clock distribution systems and supports clock frequencies up to 2 GHz. The device accepts two clock sources. The CLK0 input can be driven by ECL or PECL compatible signals, the CLK1 input accepts HSTL compatible signals. The selected input signal is distributed to 20 identical, differential ECL/PECL outputs. If V_{BB} is connected to the $\overline{CLK0}$ or $\overline{CLK1}$ input and bypassed to GND by a 10 nF capacitor, the MC100ES6221 can be driven by single-ended ECL/PECL signals utilizing the V_{BB} bias voltage output.

In order to meet the tight skew specification of the device, both outputs of a differential output pair should be terminated, even if only one output is used. In the case where not all ten outputs are used, the output pairs on the same package side as the parts being used on that side should be terminated.

The MC100ES6221 can be operated from a single 3.3 V or 2.5 V supply. As most other ECL compatible devices, the MC100ES6221 supports positive (PECL) and negative (ECL) supplies. The MC100ES6221 is pin and function compatible to the MC100EP221.

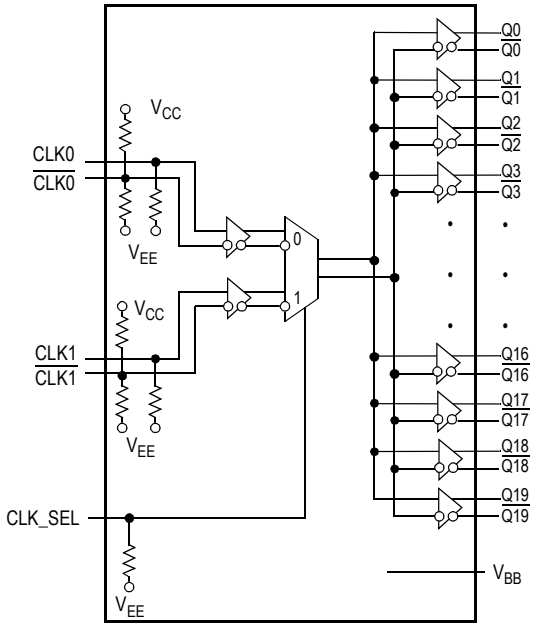


Figure 1. MC100ES6221 Logic Diagram

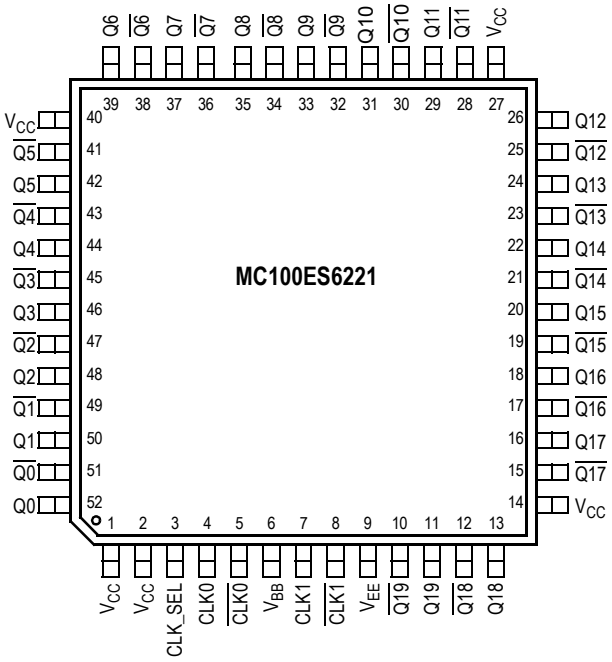


Figure 2. 52-Lead Package Pinout (Top View)

Table 1. Pin Configuration

Pin	I/O	Type	Function
CLK0, $\overline{CLK0}$	Input	ECL/PECL	Differential reference clock signal input
CLK1, $\overline{CLK1}$	Input	HSTL	Alternative differential reference clock signal input
CLK_SEL	Input	ECL/PECL	Reference clock input select
QA[0–19], QA[0–19]	Output	ECL/PECL	Differential clock outputs
V_{EE}[1]	Supply		Negative power supply
V_{CC}	Supply		Positive power supply. All V_{CC} pins must be connected to the positive power supply for correct DC and AC operation.
V_{BB}	Output	DC	Reference voltage output for single ended ECL and PECL operation

1. In ECL mode (negative power supply mode), V_{EE} is either –3.3 V or –2.5 V and V_{CC} is connected to GND (0 V). In PECL mode (positive power supply mode), V_{EE} is connected to GND (0 V) and V_{CC} is either +3.3 V or +2.5 V. In both modes, the input and output levels are referenced to the most positive supply (V_{CC}).

Table 2. Function Table

Pin	0	1
CLK_SEL	CLK0, $\overline{CLK0}$ input pair is the reference clock. CLK0 can be driven by ECL or PECL compatible signals.	CLK1, $\overline{CLK1}$ input pair is the reference clock. CLK1 can be driven by HSTL compatible signals.

Table 3. Absolute Maximum Ratings(1)

Symbol	Characteristics	Min	Max	Unit	Condition
V_{CC}	Supply Voltage	–0.3	3.6	V	
V_{IN}	DC Input Voltage	–0.3	V_{CC} + 0.3	V	
V_{OUT}	DC Output Voltage	–0.3	V_{CC} + 0.3	V	
I_{IN}	DC Input Current		±20	mA	
I_{OUT}	DC Output Current		±50	mA	
T_S	Storage Temperature	–65	125	°C	
T_{FUNC}	Functional Temperature Range	T_A = –40	T_J = +110	°C	

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 4. General Specifications

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{TT}	Output Termination Voltage		V_{CC} – 2(1)		V	
MM	ESD Protection (Machine Model)	200			V	
HBM	ESD Protection (Human Body Model)	4000			V	
CDM	ESD Protection (Charged Device Model)	2000			V	
LU	Latch-Up Immunity	200			mA	
C_{IN}	Input Capacitance		4.0		pF	Inputs
θ_{JA}, θ_{JB}, θ_{JC}	Thermal Resistance (junction-to-ambient, junction-to-board, junction-to-case)	See Table 9. Thermal Resistance			°C/W	
T_J	Operating Junction Temperature(2) (continuous operation) MTBF = 9.1 years	0		110	°C	

1. Output termination voltage V_{TT} = 0 V for V_{CC} = 2.5 V operation is supported but the power consumption of the device will increase.
2. Operating junction temperature impacts device life time. Maximum continuous operating junction temperature should be selected according to the application life time requirements (See application note AN1545 for more information). The device AC and DC parameters are specified up to 110°C junction temperature allowing the MC100ES6221 to be used in applications requiring industrial temperature range. It is recommended that users of the MC100ES6221 employ thermal modeling analysis to assist in applying the junction temperature specifications to their particular application.

Table 5. PECL DC Characteristics (V_{CC} = 2.5 V ± 5% or V_{CC} = 3.3 V ± 5%, V_{EE} = GND, T_J = 0°C to + 110°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
Clock Input Pair CLK0, $\overline{CLK0}$(1) (PECL differential signals)						
V_{PP}	Differential Input Voltage(2)	0.1		1.3	V	Differential operation
V_{CMR}	Differential Cross Point Voltage(3)	1.0		V_{CC} – 0.3	V	Differential operation
I_{IN}	Input Current(1)			±100	µA	$V_{IN} = V_{IL}$ or $V_{IN} = V_{IH}$
Clock Input Pair CLK1, $\overline{CLK1}$(4) (HSTL differential signals)						
V_{DIF}	Differential Input Voltage(5)	0.2		1.4	V	
V_X	Differential Cross Point Voltage(6)	0	0.68 - 0.9	V_{CC} – 0.7	V	
V_{IH}	Input High Voltage	V_X + 0.1		V_X + 0.7	V	
V_{IL}	Input Low Voltage	V_X – 0.7		V_X – 0.1	V	
I_{IN}	Input Current			±100	µA	$V_{IN} = V_X$ ± 0.2 V
Clock Inputs (PECL single ended signals)						
V_{IH}	Input Voltage High	V_{CC} – 1.165		V_{CC} – 0.880	V	
V_{IL}	Input Voltage Low	V_{CC} – 1.810		V_{CC} – 1.475	V	
I_{IN}	Input Current(7)			±100	µA	$V_{IN} = V_{IL}$ or $V_{IN} = V_{IH}$
PECL Clock Outputs (Q0–19, $\overline{Q0–19}$)						
V_{OH}	Output High Voltage	V_{CC} – 1.1	V_{CC} – 1.005	V_{CC} – 0.7	V	I_{OH} = –30 mA(8)
V_{OL}	Output Low Voltage	V_{CC} – 1.9	V_{CC} – 1.705	V_{CC} – 1.4	V	I_{OL} = –5 mA(8)
Supply current and V_{BB}						
I_{EE}(9)	Maximum Quiescent Supply Current without Output Termination Current		84	160	mA	V_{EE} pins
V_{BB}	Output Reference Voltage (f_{ref} < 1.0 GHz)(10)	V_{CC} – 1.42		V_{CC} – 1.20	V	I_{BB} = 0.4 mA

1. The input pairs CLK0, CLK1 are compatible to differential signaling standards. CLK0 is compatible to LVPECL signals and CLK1 meets both HSTL differential signal specifications. The difference between CLK0 and CLK1 is the differential input threshold voltage (V_{CMR}).
2. V_{PP} (DC) is the minimum differential input voltage swing required to maintain device functionality.
3. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} (DC) range and the input swing lies within the V_{PP} (DC) specification.
4. Clock inputs driven by differential HSTL compatible signals. Only applicable to CLK1, $\overline{CLK1}$.
5. V_{DIF} (DC) is the minimum differential HSTL input voltage swing required for device functionality.
6. V_X (DC) is the crosspoint of the differential HSTL input signal. Functional operation is obtained when the crosspoint is within the V_X (DC) range and the input swing lies within the V_{PP} (DC) specification.
7. Inputs have internal pullup/pulldown resistors which affect the input current.
8. Equivalent to a termination of 50 Ω to V_{TT}.
9. I_{CC} calculation: I_{CC} = (number of differential output used) x (I_{OH} + I_{OL}) + I_{EE}
   I_{CC} = (number of differential output used) x (V_{OH} – V_{TT}) ÷ R_{load} + (V_{OL} – V_{TT}) ÷ R_{load} + I_{EE}.
10. Using V_{BB} to bias unused single-ended inputs is recommended only up to a clock reference frequency of 1 GHz. Above 1 GHz, only differential input signals should be used with the MC100ES6221.

Table 6. ECL DC Characteristics (V_{EE} = –2.5 V ± 5% or V_{EE} = –3.3 V ± 5%, V_{CC} = GND, T_J = 0°C to + 110°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
Clock Input Pair CLK0, $\overline{CLK0}$ (ECL differential signals)						
V_{PP}	Differential Input Voltage[1]	0.1		1.3	V	Differential operation
V_{CMR}	Differential Cross Point Junction to top of Package Voltage[2]	V_{EE} + 1.0		–0.3	V	Differential operation
I_{IN}	Input Current[1]			±100	µA	$V_{IN} = V_{IL}$ or $V_{IN} = V_{IH}$
Clock Inputs (ECL single ended signals)						
V_{IH}	Input Voltage High	–1.165		–0.880	V	
V_{IL}	Input Voltage Low	–1.810		–1.475	V	
I_{IN}	Input Current[3]			±100	µA	$V_{IN} = V_{IL}$ or $V_{IN} = V_{IH}$
ECL Clock Outputs (Q0–A19, $\overline{Q0–Q19}$)						
V_{OH}	Output High Voltage	–1.1	–1.005	–0.7	V	I_{OH} = –30 mA[4]
V_{OL}	Output Low Voltage	–1.9	–1.705	–1.4	V	I_{OL} = –5 mA[4]
Supply Current and V_{BB}						
I_{EE}[5]	Maximum Quiescent Supply Current without Output Termination Current		84	160	mA	V_{EE} pins
V_{BB}	Output Reference Voltage (f_{ref} < 1.0 GHz)[6]	–1.42		–1.20	V	I_{BB} = 0.4 mA

1. V_{PP} (DC) is the minimum differential input voltage swing required to maintain device functionality.
2. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} (DC) range and the input swing lies within the V_{PP} (DC) specification.
3. Inputs have internal pullup/pulldown resistors which affect the input current.
4. Equivalent to a termination of 50 Ω to V_{TT}.
5. I_{CC} calculation: I_{CC} = (number of differential output used) x (I_{OH} + I_{OL}) + I_{EE}
   I_{CC} = (number of differential output used) x (V_{OH} – V_{TT}) ÷ R_{load} + (V_{OL} – V_{TT}) ÷ R_{load} + I_{EE}.
6. V_{BB} can be used to bias unused single-ended inputs up to a clock reference frequency of 1 GHz. Above 1 GHz, only differential signals should be used with the MC100ES6221.

Table 7. AC Characteristics (ECL: V_{EE} = –3.3 V ± 5% or V_{EE} = –2.5 V ± 5%, V_{CC} = GND) or (PECL: V_{CC} = 3.3 V ± 5% or V_{CC} = 2.5 V ± 5%, V_{EE} = GND, T_J = 0°C to + 110°C)[1]

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
Clock Input Pair CLK0, $\overline{CLK0}$ (PECL or ECL differential signals)						
V_{PP}	Differential Input Voltage[2] (peak-to-peak)	0.2		1.3	V	
V_{CMR}	Differential Input Crosspoint Voltage[3] PECL ECL	1.0 V_{EE} + 1.0		V_{CC} – 0.3 –0.3 V	V V	
f_{CLK}	Input Frequency	0		2000	MHz	Differential
t_{PD}	Propagation Delay CLK0 to Q0-19	400	540	670	ps	Differential
Clock Input Pair CLK1, $\overline{CLK1}$ (HSTL differential signals)						
V_{DIF}	Differential Input Voltage[4] (peak-to-peak)	0.2		1.3	V	
V_X	Differential Input Crosspoint Voltage[5]	0.1	0.68–0.9	V_{CC} – 1.0	V	
f_{CLK}	Input Frequency	0		1000	MHz	Differential
t_{PD}	Propagation Delay CLK1 to Q0–19	650	780	950	ps	Differential
PECL/ECL Clock Outputs (Q0–19, $\overline{Q0–19}$)						
$V_{O(P-P)}$	Differential Output Voltage (peak-to-peak) f_O < 1.0 GHz f_O < 2.0 GHz	 0.375 TDB	 0.630 0.250		 V V	
$t_{sk(O)}$	Output-to-Output Skew		50	100	ps	Differential
$t_{sk(PP)}$	Output-to-Output Skew (part-to-part) using CLK0 using CLK1 parts at one given T_J, V_{CC}, f_{ref}			 270 300 250	 ps ps ps	Differential
$t_{JIT(CC)}$	Output Cycle-to-Cycle Jitter RMS (1σ)			1	ps	
$t_{SK(P)}$	Output Pulse Skew[6]		30	50	ps	
DC_Q	Output Duty Cycle f_{REF} < 0.1 GHz f_{REF} < 1.0 GHz	49.5 45.0	50 50	50.5 55.0	% %	DC_{REF} = 50% DC_{REF} = 50%
t_r, t_f	Output Rise/Fall Time	50		350	ps	20% to 80%

1. AC characteristics apply for parallel output termination of 50 Ω to V_{TT}.
2. V_{PP} (AC) is the minimum differential ECL/PECL input voltage swing required to maintain AC characteristics including t_{PD} and device-to-device skew.
3. V_{CMR} (AC) is the crosspoint of the differential ECL/PECL input signal. Normal AC operation is obtained when the crosspoint is within the V_{CMR} (AC) range and the input swing lies within the V_{PP} (AC) specification. Violation of V_{CMR} (AC) or V_{PP} (AC) impacts the device propagation delay, device and part-to-part skew.
4. V_{DIF} (AC) is the minimum differential HSTL input voltage swing required to maintain AC characteristics including t_{PD} and device-to-device skew. Only applicable to CLKB.
5. V_X (AC) is the crosspoint of the differential HSTL input signal. Normal AC operation is obtained when the crosspoint is within the V_X (AC) range and the input swing lies within the V_{DIF} (AC) specification. Violation of V_X (AC) or V_{DIF} (AC) impacts the device propagation delay, device and part-to-part skew.
6. Output pulse skew is the absolute difference of the propagation delay times: $| t_{pLH} – t_{pHL} |$.

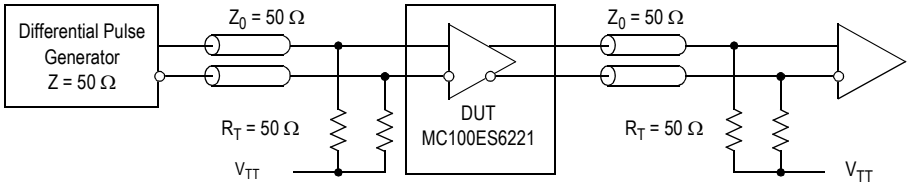


Figure 3. MC100ES6221 Test Reference

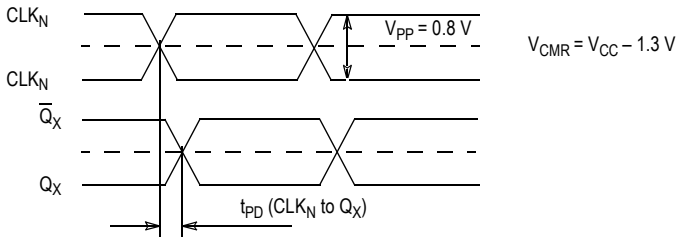


Figure 4. MC100ES6221 AC Test Reference Measurement Waveform

APPLICATIONS INFORMATION

Understanding the Junction Temperature Range of the MC100ES6221

To make the optimum use of high clock frequency and low skew capabilities of the MC100ES6221, the MC100ES6221 is specified, characterized and tested for the junction temperature range of T_J = 0°C to +110°C. Because the exact thermal performance depends on the PCB type, design, thermal management and natural or forced air convection, the junction temperature provides an exact way to correlate the application specific conditions to the published performance data of this data sheet. The correlation of the junction temperature range to the application ambient temperature range and vice versa can be done by calculation:

$$T_J = T_A + R_{thja} \cdot P_{tot}$$

Assuming a thermal resistance (junction to ambient) of 17°C/W (2s2p board, 200 ft/min airflow, see Table 8) and a typical power consumption of 1148 mW (all outputs terminated 50 ohms to V_{TT}, V_{CC} = 3.3 V, frequency independent), the junction temperature of the MC100ES6221 is approximately T_A + 21°C, and the minimum ambient temperature in this example case calculates to –21°C (the maximum ambient temperature is 89°C. See Table 8). Exceeding the minimum junction temperature specification of the MC100ES6221 does not have a significant impact on the device functionality. However, the continuous use the MC100ES6221 at high ambient temperatures requires thermal management to not exceed the specified maximum junction temperature. Please see the application note AN1545 for a power consumption calculation guideline.

Table 8. Ambient Temperature Ranges (P_{tot} = 1148 mW)

R_{thja} (2s2p board)		$T_{A, min}$ (1)	$T_{A, max}$
Natural convection	20°C/W	–23 °C	87°C
100 ft/min	18°C/W	–21 °C	89°C
200 ft/min	17°C/W	–20 °C	90°C
400 ft/min	16°C/W	–18 °C	92°C
800 ft/min	15°C/W	–17 °C	93°C

1. The MC100ES6221 device function is guaranteed from T_A = –40°C to T_J = 110°C

Maintaining Lowest Device Skew

The MC100ES6221 guarantees low output-to-output bank skew of 50 ps and a part-to-part skew of max. 270 ps. To ensure low skew clock signals in the application, both outputs of any differential output pair need to be terminated identically, even if only one output is used. When fewer than all nine output pairs are used, identical termination of all output pairs within the output bank is recommended. This will reduce the device power consumption while maintaining minimum output skew.

Power Supply Bypassing

The MC100ES6221 is a mixed analog/digital product. The differential architecture of the MC100ES6221 supports low noise signal operation at high frequencies. In order to maintain its superior signal quality, all V_{CC} pins should be bypassed by high-frequency ceramic capacitors connected to GND. If the spectral frequencies of the internally generated switching noise on the supply pins cross the series resonant point of an individual bypass capacitor, its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the noise bandwidth.

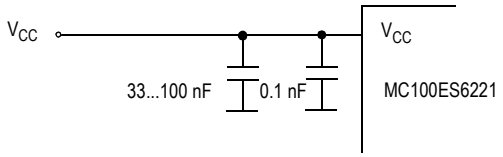


Figure 5. V_{CC} Power Supply Bypass

APPLICATIONS INFORMATION

Using the Thermally Enhanced Package of the MC100ES6221

The MC100ES6221 uses a thermally enhanced exposed pad (EP) 52 lead LQFP package. The package is molded so that the lead frame is exposed at the surface of the package bottom side. The exposed metal pad will provide the low thermal impedance that supports the power consumption of the MC100ES6221 high-speed bipolar integrated circuit and eases the power management task for the system design. A thermal land pattern on the printed circuit board and thermal vias are recommended in order to take advantage of the enhanced thermal capabilities of the MC100ES6221. Direct soldering of the exposed pad to the thermal land will provide an efficient thermal path. In multilayer board designs, thermal vias thermally connect the exposed pad to internal copper planes. Number of vias, spacing, via diameters and land pattern design depend on the application and the amount of heat to be removed from the package. A nine thermal via array, arranged in a 3 x 3 array and using a 1.2 mm pitch in the center of the thermal land is a requirement for MC100ES6221 applications on multi-layer boards. The recommended thermal land design comprises a 3 x 3 thermal via array as shown in Figure 6, providing an efficient heat removal path.

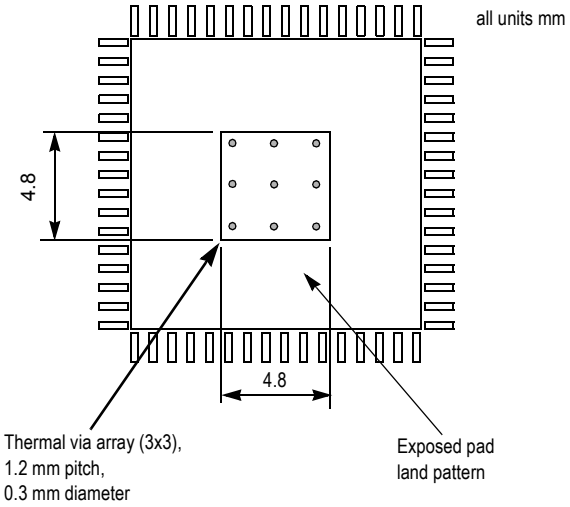


Figure 6. Recommended Thermal Land Pattern

The via diameter is should be approx. 0.3 mm with 1 oz. copper via barrel plating. Solder wicking inside the via resulting in voids during the solder process must be avoided. If the copper plating does not plug the vias, stencil print solder paste onto the printed circuit pad. This will supply enough solder paste to fill those vias and not starve the solder joints. The attachment process for exposed pad package is equivalent to standard surface mount packages. Figure 7 shows a recommend solder mask opening with respect to the recommended 3 x 3 thermal via array. Because a large solder mask opening may result in a poor release, the opening should be subdivided as shown in Figure 7. For the nominal package standoff 0.1 mm, a stencil thickness of 5 to 8 mils should be considered.

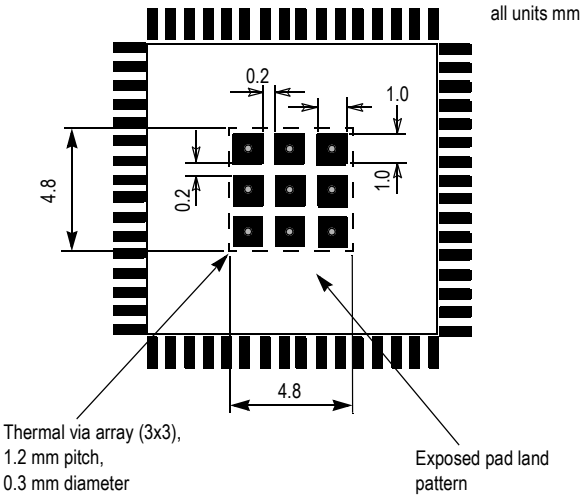


Figure 7. Recommended Solder Mask Openings

For thermal system analysis and junction temperature calculation the thermal resistance parameters of the package is provided:

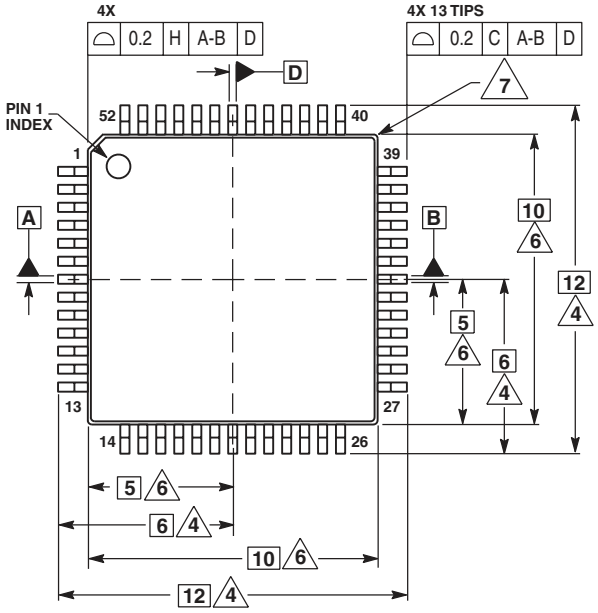
Table 9. Thermal Resistance(1)

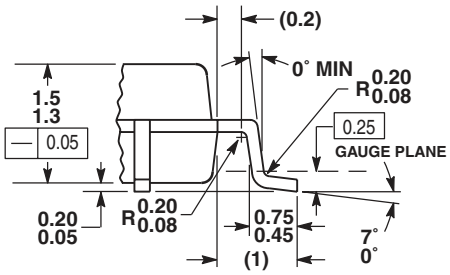
ConvectionL FPM	R_{THJA}(2) °C/W	R_{THJA}(3) °C/W	R_{THJC} °C/W	R_{THJB}(4) °C/W
Natural	20	48	4(5) 29(6)	16
100	18	47		
200	17	46		
400	16	43		
800	15	41		

1. Applicable for a 3 x 3 thermal via array.
2. Junction to ambient, four conductor layer test board (2S2P), per JES51–7 and JESD 51–5.
3. Junction to ambient, single layer test board, per JESD51–3.
4. Junction to board, four conductor layer test board (2S2P) per JESD 51–8.
5. Junction to exposed pad.
6. Junction to top of package.

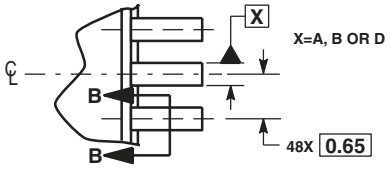
It is recommended that users employ thermal modeling analysis to assist in applying the general recommendations to their particular application. The exposed pad of the MC100ES6221 package does not have an electrical low impedance path to the substrate of the integrated circuit and its terminals. The thermal land should be connected to GND through connection of internal board layers.

PACKAGE DIMENSIONS

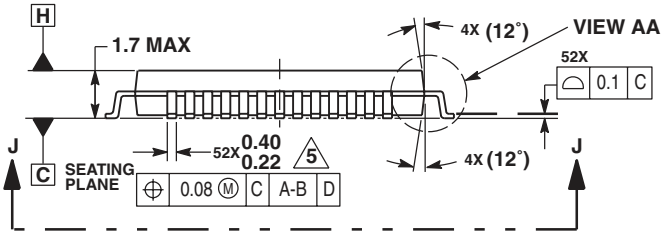


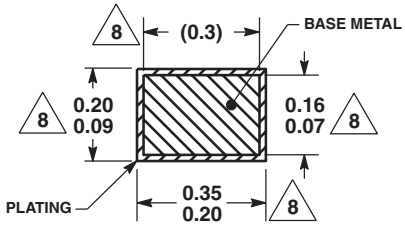


VIEW AA

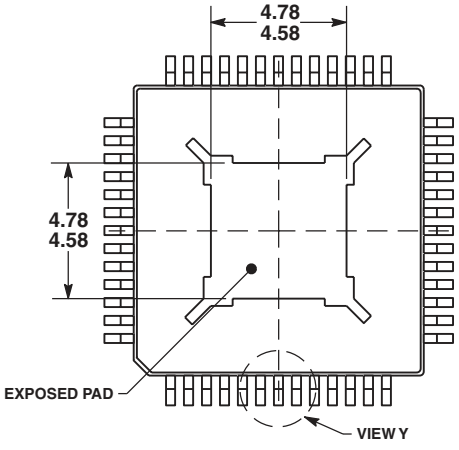


VIEW Y





SECTION B-B



VIEW J-J

NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.
4. DIMENSION TO BE DETERMINED AT SEATING PLANE C.
5. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.46 mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT BE LESS THAN 0.07 mm.
6. THIS DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. THIS DIMENSION IS MAXIMUM PLSTIC BODY SIZE DIMENSION INCLUDING MOLD MISMATCH.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.

CASE 1336A-01
ISSUE O
52-LEAD LQFP PACKAGE

Revision History Sheet

Rev	Table	Page	Description of Change	Date
6		1	Product Discontinuation Notice - Last Time Buy Expires (June 30, 2014) PDN# N-12-36R2	10/2/13

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