3-W STEREO AUDIO POWER AMPLIFIER WITH ADVANCED DC VOLUME CONTROL

FEATURES

- **3 W Into 16 Ω From 12-V Supply**
- **Volume Control for Speakers (BTL) and Headphones (SE)**
- **Differential Inputs**
- **Depop Circuitry**
- **1 μA Shutdown Current**
- **Surface-Mount Package**

APPLICATIONS

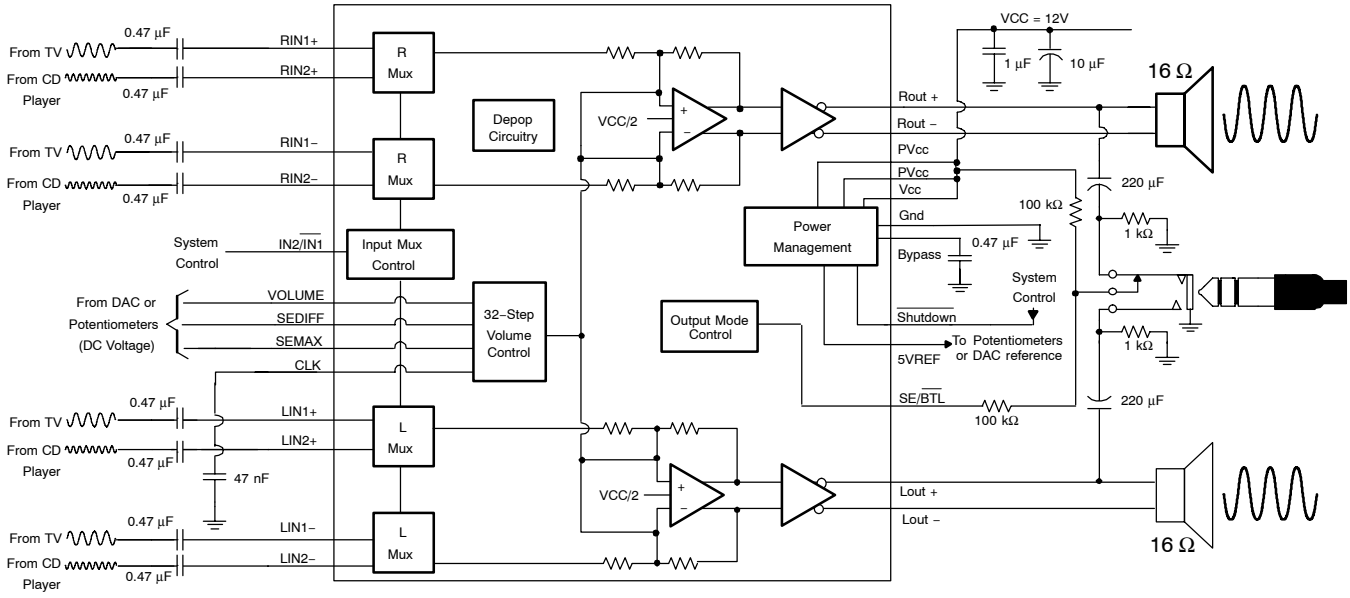
- **LCD Monitors and LCD TVs**
- **Multimedia Speakers**
- **Notebook Computers**

DESCRIPTION

The TPA6030A4 is designed to drive 3 W into 16-Ω speakers using a surface-mount package without the need for an external heatsink. These features make it ideal for 15″–17″ LCD monitors, small multimedia speakers, and notebook computers.

To simplify system design, the speaker volume level is adjusted by applying a dc voltage to the VOLUME terminal. The delta between speaker volume and headphone volume can be adjusted by applying a dc voltage to the SEDIFF terminal. To avoid an unexpected high volume level through the headphones, a third terminal, SEMAX, limits the headphone volume level when a dc voltage is applied. Integrated depop circuitry and the fully differential design minimize pops, clicks, and unwanted noise to provide a high level of audio performance.

The device is available in a 28-pin TSSOP PowerPAD™ package. The PowerPAD™ package is designed to transfer heat into the ground plane, eliminating the need for external heat sinks—minimizing solution cost and size.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a trademark of Texas Instruments.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

CAUTION:

During normal operation, shorting the outputs together, to ground, or to V_{CC} may cause permanent damage to the device.

ORDERING INFORMATION

SPECIFIED TEMPERATURE RANGE	PACKAGE DEVICE TSSOP (PWP)
–40°C to 85°C	TPA6030A4PWP

(1) The PWP package is available taped and reeled To order a taped and reeled part, add the suffix R to the part number (e.g., TPA6030A4PWPR).

PACKAGE DISSIPATION RATINGS

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
PWP	4.47W(1)	35.8 mW/°C	2.86 W	2.32 W

(1) The PowerPAD must be soldered to a thermal land on the printed-circuit board. Refer to the Texas Instruments document, *PowerPAD Thermally Enhanced Package Application Report* (literature number SLMA002) for more information on the PowerPAD package. The thermal data was measured on a PCB layout based on the information in the section entitled *Texas Instruments Recommended Board for PowerPAD* on page 33 of the before mentioned document.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

	TPA6030A4
Supply voltage, V_{CC}, PV_{CC}	–0.3 V to 15 V
IN2, $\overline{IN1}$ Input voltage, V_I	–0.3 V to V_{CC} + 0.3V
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A	–40°C to 85°C
Operating junction temperature range, T_J	–40°C to 150°C
Storage temperature range, T_{stg}	–65°C to 85°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
Supply voltage, PV_{CC}, V_{CC}		7	15	V
High input voltage, V_{IH}	SE/$\overline{BTL}$, IN2/$\overline{IN1}$	0.8V_{CC}	V_{CC}	V
	$\overline{SHUTDOWN}$	2	V_{CC}	
Low input voltage, V_{IL}	SE/$\overline{BTL}$, IN2/$\overline{IN1}$	0	0.5 V_{CC}	V
	$\overline{SHUTDOWN}$	0	0.8	
Operating free-air temperature, T_A		–40	85	°C

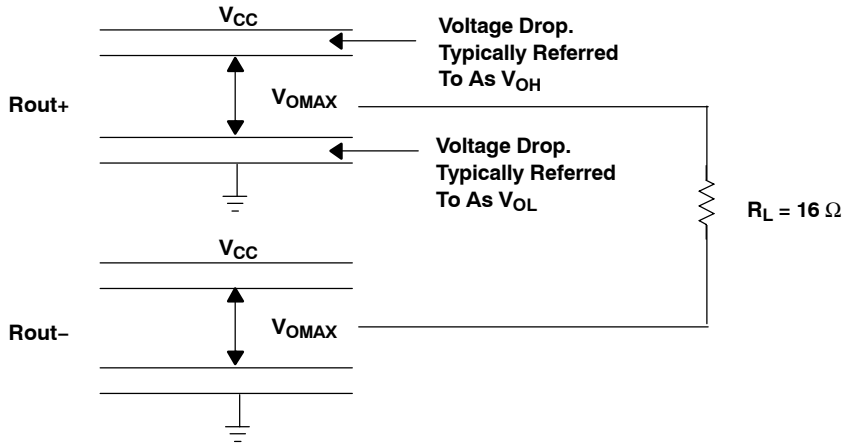
ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = PV_{CC} = 12 V, unless otherwise noted

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$\lvert V_{OS} \rvert$	Output offset	Volume = 36 dB, SE/$\overline{BTL}$ = 0 V	Out+ to Out–		10	55	mV
			Out+ to $V_{(BYPASS)}$		10	105	
			Out– to $V_{(BYPASS)}$		10	105	
PSRR	Power supply rejection ratio	V_{CC} = PV_{CC} = 12 V to 15 V		–42	–60		dB
$\lvert I_{IH} \rvert$	High-level input current	SE/$\overline{BTL}$, IN2/$\overline{IN1}$	V_{CC} = 15 V, V_I = V_{CC}			1	µA
		$\overline{SHUTDOWN}$,	V_{CC} = 15 V, V_I = 12 V			3	
$\lvert I_{IL} \rvert$	Low-level input current	SE/$\overline{BTL}$, IN2/$\overline{IN1}$	V_{CC} = 15 V, V_I = 0			1	µA
		$\overline{SHUTDOWN}$,	V_{CC} = 15 V, V_I = 0			1	
I_{CC}	Supply current	No load, $\overline{SHUTDOWN}$ = 2 V	SE/$\overline{BTL}$ = 0 V, V_{CC} = 7 V to 15 V		18	26	mA
			SE/$\overline{BTL}$ = V_{CC}, V_{CC} = 7 V to 15 V		11	16	
	Supply current, full clipping at outputs, stereo operation	R_L =16 Ω, SE/$\overline{BTL}$ = 0 V, $\overline{SHUTDOWN}$ = V_{CC}			1.2		A
$I_{CC(SD)}$	Supply current, shutdown mode	No Load, V_{CC}=15 V, $\overline{SHUTDOWN}$ = 0.8 V			1	3	µA
5VREF		V_{CC} = 7 V to 15 V, R_L = 16-Ω stereo, Pin floating		4.4	4.7	5.5	V
V_{OMAX}	DC maximum output voltage swing per output(1)	R_L =16 Ω, VOLUME = 5VREF, IN+ = (V_{CC} / 2) – 1 V and IN– = (V_{CC} / 2) + 1 V OR IN+ = (V_{CC} / 2) + 1 V and IN– = (V_{CC} / 2) – 1 V	V_{CC} = 7 V		4.4		V_{PP}
			V_{CC} = 12 V	7.6	8.4	9.3	
			V_{CC} = 15 V		9.8		

(1) See diagram below

DC MAXIMUM OUTPUT VOLTAGE SWING PER CHANNEL



OPERATING CHARACTERISTICS

T_A = 25°C, R_L = 16 Ω, Volume = 8.13 dB, unless otherwise noted3

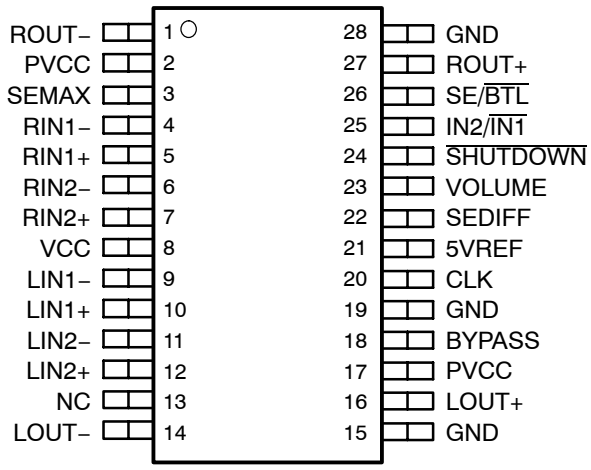
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
P_O	Output power	V_{CC} = 12 V	THD=1%, f = 1 kHz		2.2		W
			THD=10%, f = 1 kHz		3		
		V_{CC} = 15 V	THD=1%, f = 1 kHz		4(1,2)		
			THD=10%, f = 1 kHz		5(1,2)		
THD+N	Total harmonic distortion plus noise	P_O = 1 W,	f = 20 Hz to 20 kHz		0.1%		
B_{OM}	Maximum output power bandwidth	THD+N < 10%	V_{CC} = 7 V to 15 V		20		kHz
k_{SVR}	Supply ripple rejection ratio	f = 20 Hz–20 kHz, $C_{(BYPASS)}$ = 1 µF, $V_{(ripple)}$ = 100 mV_{rms}, BTL	V_{CC} = 7 V		–58		dB
			V_{CC} = 12 V		–60		
			V_{CC} = 15 V		–60		
Xtalk	Channel to channel output separation	f = 1 kHz, BTL,	Volume = 0.53 dB		–110		dB
SNR	Signal-to-noise ratio	f = 20 Hz to 20 kHz, BTL, Inputs ac grounded, THD+N = 0.5%, P_O = 2.35 W	Volume = 0.53 dB		102.5		dBV
			Volume = 36 dB		83		
	Attenuation, input to output in shutdown mode	SE, f = 20 Hz–20 kHz, R_L = 32 Ω, Volume = 30 dB			73		dB
		BTL, f = 20 Hz–20 kHz, R_L = 16 Ω, Volume = 36 dB			110		

(1) At T_A = 25°C, a derating factor of 48 mW/°C is necessary in order for the device to function properly in this configuration.

(2) If used on a board with a layout set forth on page 33 of the *PowerPAD Thermally Enhanced Package Application Report* (literature number SLMA002) to achieve a derating factor of 35.8mW/°C, it is possible to operate the device at these output power levels so long as it is in a mono, BTL configuration.

PIN ASSIGNMENTS

PWP PACKAGE
(TOP VIEW)



NC – No internal connection

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
5VREF	21	O	Internal 5-V reference for VOLUME, SEDIFF, and SEMAX pins ONLY
BYPASS	18	I	Connect capacitor to ground for BYPASS midrail voltage supply filtering
CLK	20	I	Connect capacitor to ground to set clock frequency of volume control counter
GND	15, 19, 28	I	Ground
IN2/$\overline{\text{IN1}}$	25	I	Controls input MUX, high selects IN2 inputs, low selects IN1 inputs
LIN1–	9	I	Left negative differential input, selected when IN2/$\overline{\text{IN1}}$ is held low
LIN1+	10	I	Left positive differential input, selected when IN2/$\overline{\text{IN1}}$ is held low
LIN2–	11	I	Left negative differential input, selected when IN2/$\overline{\text{IN1}}$ is held high
LIN2+	12	I	Left positive differential input, selected when IN2/$\overline{\text{IN1}}$ is held high
LOUT–	14	O	Left negative output in speaker mode and high impedance in headphone mode
LOUT+	16	I	Left positive output in speaker mode, and positive output in headphone mode
NC	13		No internal connection
PVCC	2,17	I	Power supply for the output stage
RIN1–	4	I	Right negative differential input, selected when IN2/$\overline{\text{IN1}}$ is held low
RIN1+	5	I	Right positive differential input, selected when IN2/$\overline{\text{IN1}}$ is held low
RIN2–	6	I	Right negative differential input, selected when IN2/$\overline{\text{IN1}}$ is held high
RIN2+	7	I	Right positive differential input, selected when IN2/$\overline{\text{IN1}}$ is held high
ROUT+	27	O	Right positive output in speaker mode, and positive output in headphone mode
ROUT–	1	O	Right negative output in speaker mode (BTL) and high impedance in headphone mode (SE)
SE/$\overline{\text{BTL}}$	26	I	Determines output mode, high selects headphone mode (SE), low selects speaker mode (BTL)
SEDIFF	22	I	Sets the difference between speaker and headphone volume (from –6 dB down to mute)
SEMAX	3	I	Sets maximum headphone volume. DC range is 0 to 5VREF
$\overline{\text{SHUTDOWN}}$	24	I	Shutdown terminal (active low, TTL compatible, V_{CC} compliant)
VCC	8	I	Supply voltage terminal
VOLUME	23	I	Master volume control. DC voltage range is 0 to 5VREF
THERMAL PAD	–	–	Connect to ground. The thermal pad must be soldered down in all applications to properly secure the device on the PC board. Properly soldering the thermal pad to the PC board is necessary for achieving the required heat transfer for device cooling.

VOLUME CONTROL

Table 1 shows the functionality of the 32-step volume control. The voltage difference between trip levels is 2.66% of 5VREF, and the difference between gain steps is 2.53 dB.

Table 1. Volume Control
(V_{CC} = 12 V, No Load, SEDIFF = 0 V, SEMAX = 5VREF)

VOLTAGE ON VOLUME PIN AS A PERCENTAGE OF 5VREF	SPEAKER VOLUME (dB)	HEADPHONE VOLUME (dB)
0–10	–80.00	–86.00
10–12.6	–40.00	–46.00
12.6–15.2	–37.47	–43.47
15.2–18	–34.93	–40.93
18–20.6	–32.40	–38.40
20.6–23.4	–29.87	–35.87
23.4–26	–27.33	–33.33
26–28.6	–24.80	–30.80
28.6–31.4	–22.27	–28.27
31.4–34	–19.73	–25.73
34–36.6	–17.20	–23.20
36.6–39.4	–14.67	–20.67
39.4–42	–12.13	–18.13
42–44.6	–9.60	–15.60
44.6–47.2	–7.07	–13.07
47.2–50	–4.53	–10.53
50–52.6	–2.00	–8.00
52.6–55.4	0.53	–5.47
55.4–58	3.07	–2.93
58–60.6	5.60	–0.40
60.6–63.4	8.13	2.13
63.4–66	10.67	4.67
66–68.6	13.20	7.20
68.6–71.4	15.73	9.73
71.4–74	18.27	12.27
74–76.6	20.80	14.80
76.6–79.4	23.33	17.33
79.4–82	25.87	19.87
82–84.6	28.40	22.40
84.6–87.4	30.93	24.93
87.4–90	33.47	27.47
90–100	36.00	30.00

Refer to the section entitled Volume Control Description in the Application Information section of this data sheet for more details regarding the use of the volume control.

The volume in single-ended (SE) mode is determined by the following equation:

SE Volume = min [(VOLUME − SEDIFF) or (SEMAX)] − 6 dB, where VOLUME is the voltage (expressed in terms of %VREF) applied to the VOLUME pin, SEDIFF is the voltage (%VREF) applied to the SEDIFF pin, and SEMAX is the voltage (%VREF) applied to the SEMAX pin. The SE Volume control is integrated into the 32-step volume control. A block diagram of the SE Volume control portion is shown in Figure 1.

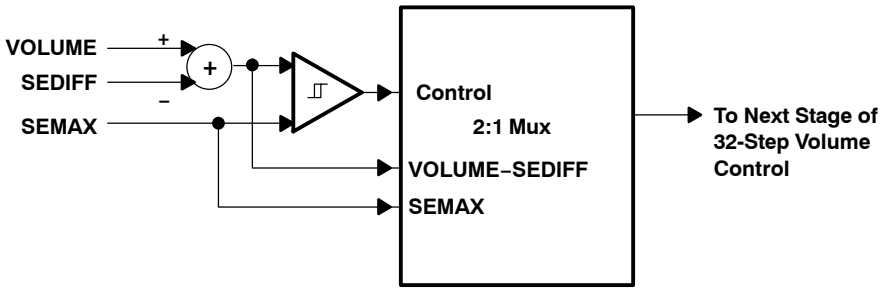


Figure 1. Block Diagram of the SE Volume Control

Refer to the section entitled Volume Control Description in the Application Information section of this data sheet for more details regarding the use of the volume control.

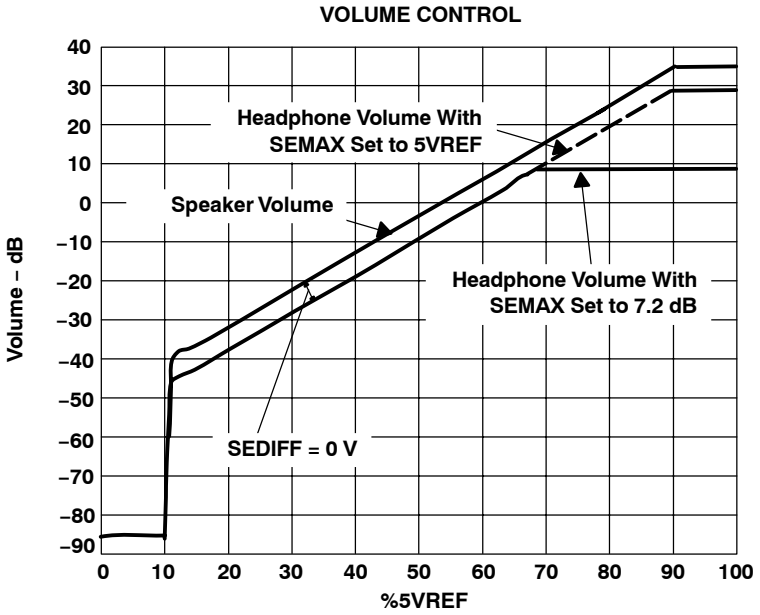


Figure 2. Speakers (BTL) and Headphones (SE) Volume vs %5VREF

Figure 2 illustrates the functionality of the TPA6030A4 volume control. As the voltage applied to the VOLUME control pin is increased, the volume increases.

Increasing the voltage on the SEDIFF pin increases the delta in volume between speaker (BTL) and headphone (SE) volume from a minimum of 6 dB to a maximum reduction in headphone volume, resulting in mute.

The SEMAX input limits the maximum output level in headphone mode. The dashed line shows operation with SEMAX set to 5VREF, which results in maximum output in headphone mode. The horizontal line in Figure 2 shows operation with SEDIFF set to 0V, and SEMAX set to 67.3% of 5VREF, for a maximum volume in headphone mode of 7.2 dB.

Neither SEMAX nor SEDIFF have any affect on the volume in speaker mode.

TYPICAL CHARACTERISTICS

TABLE OF GRAPHS

			FIGURE
THD+N	Total harmonic distortion plus noise (BTL)	vs Output power	3
		vs Frequency	5
THD+N	Total harmonic distortion plus noise (SE)	vs Output power	4
		vs Frequency	6
	Crosstalk (BTL)	vs Frequency	7
CMRR	Common mode rejection ratio	vs Frequency	8
		vs Common-mode input voltage	9
	Closed loop response (BTL)	vs Frequency	10
P_D	Power dissipation	vs Output power (per channel)	11
R_i	Input resistance	vs Volume	12
R_L	Recommended load impedance	vs Supply voltage	13

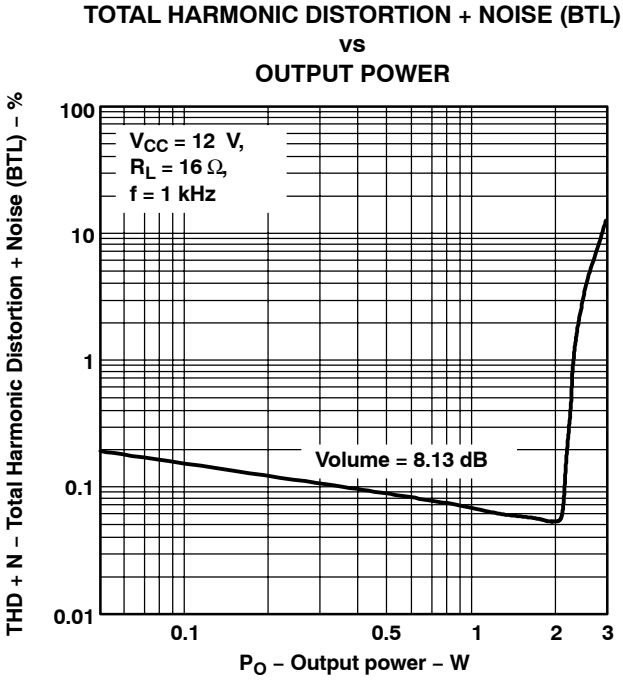


Figure 3

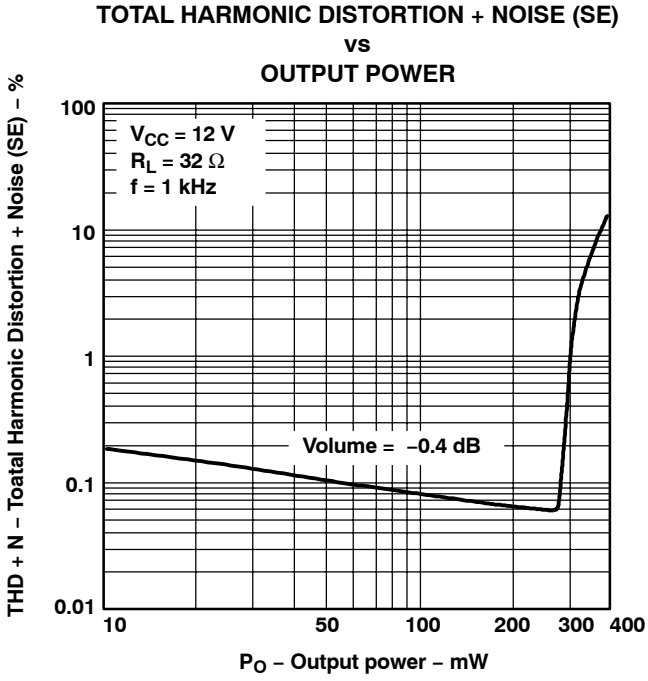


Figure 4

TOTAL HARMONIC DISTORTION + NOISE (BTL)
vs
FREQUENCY

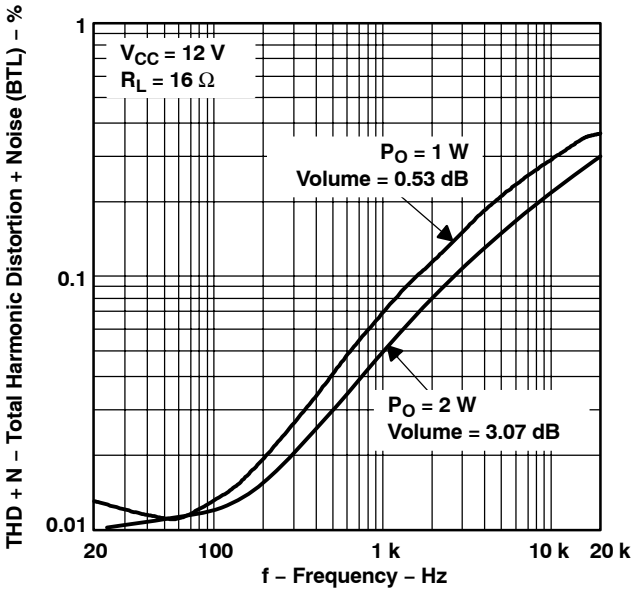


Figure 5

TOTAL HARMONIC DISTORTION + NOISE (SE)
vs
FREQUENCY

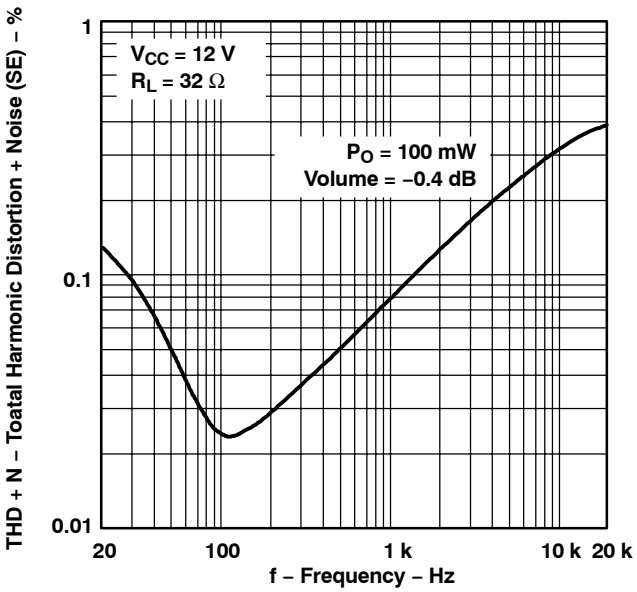


Figure 6

CROSSTALK (BTL)
vs
FREQUENCY

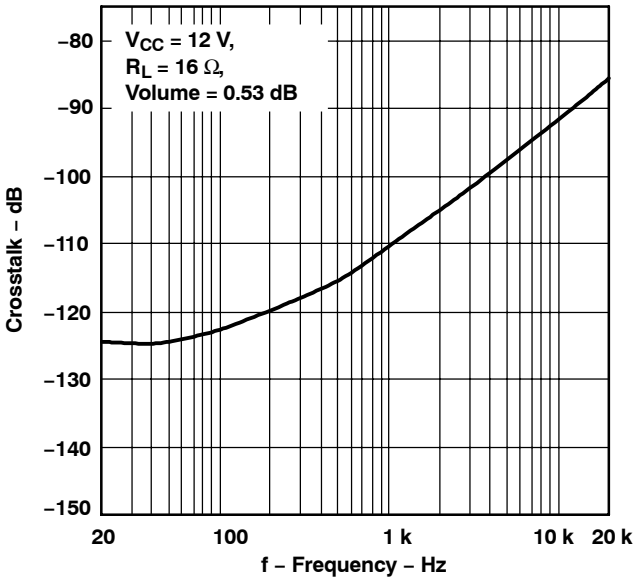


Figure 7

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

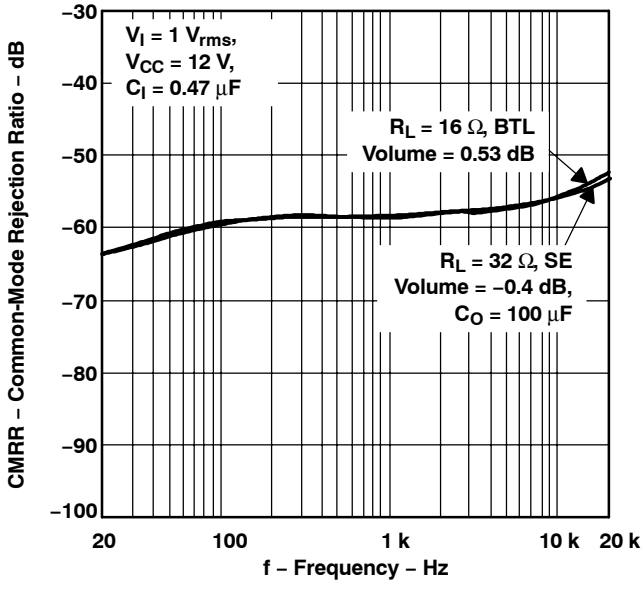


Figure 8

COMMON-MODE REJECTION RATIO vs COMMON-MODE INPUT VOLTAGE

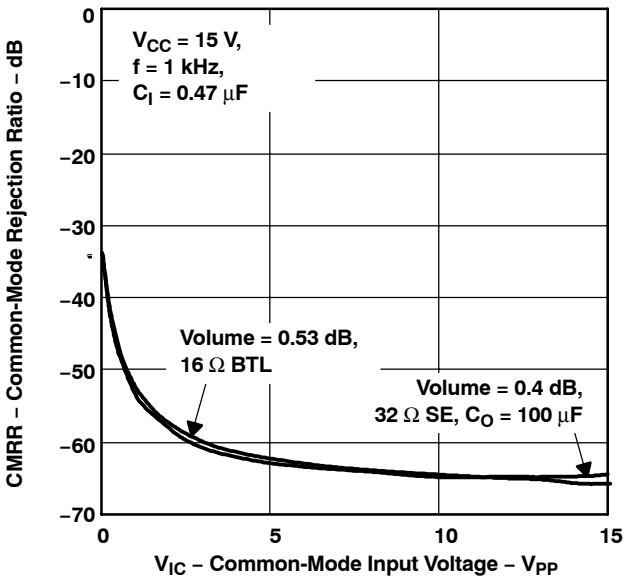


Figure 9

CLOSED LOOP RESPONSE (BTL) vs FREQUENCY

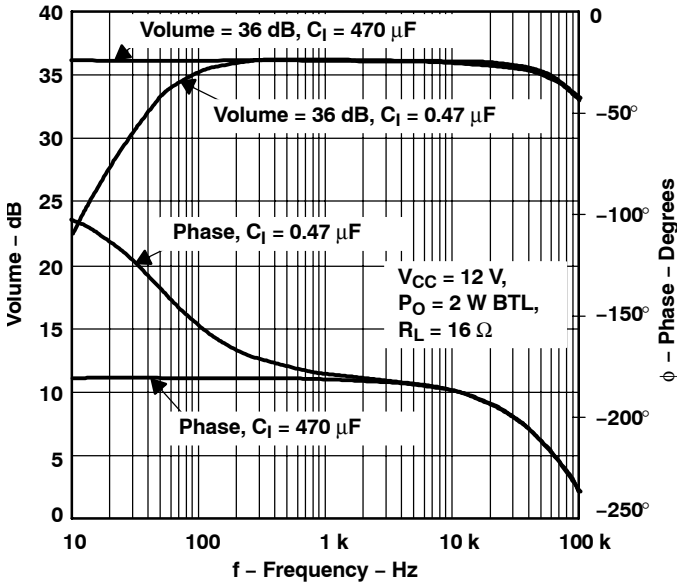


Figure 10

POWER DISSIPATION vs OUTPUT POWER (PER CHANNEL)

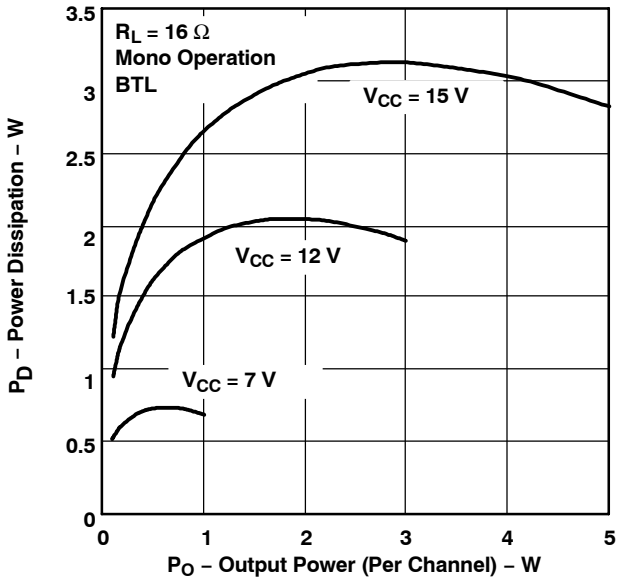


Figure 11

INPUT RESISTANCE vs VOLUME

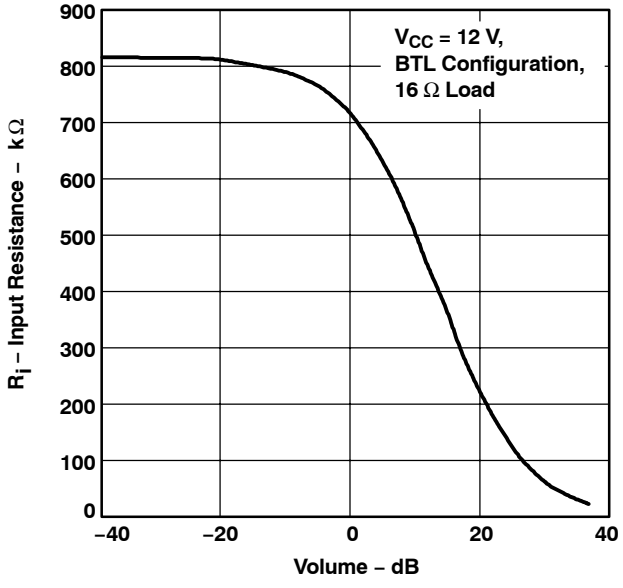


Figure 12

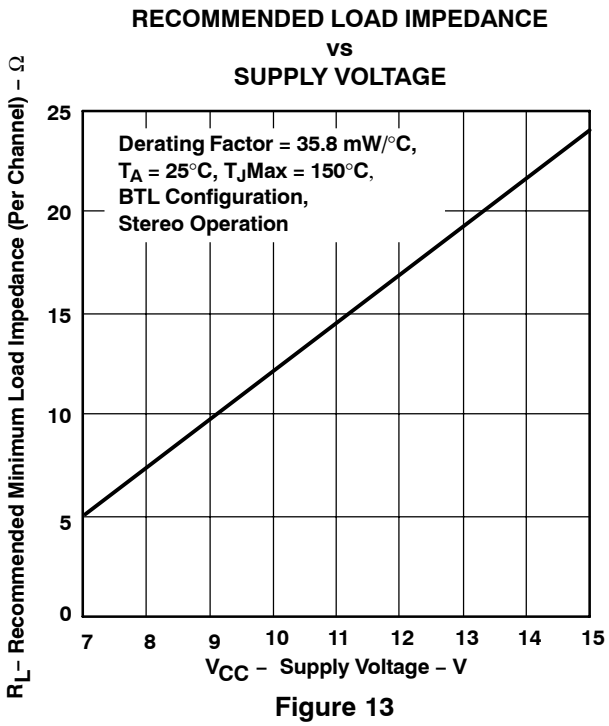

RECOMMENDED LOAD IMPEDANCE
vs
SUPPLY VOLTAGE
Derating Factor = 35.8 mW/°C,
TA = 25°C, TJMax = 150°C,
BTL Configuration,
Stereo Operation
RL – Recommended Minimum Load Impedance (Per Channel) – Ω
VCC – Supply Voltage – V
0
5
10
15
20
25
7
8
9
10
11
12
13
14
15

Figure 13

APPLICATION INFORMATION

VOLUME, SEDIFF, AND SEMAX OPERATION

The three pins labeled VOLUME, SEDIFF, and SEMAX control the speaker (BTL) volume (VOLUME pin only) and the headphone (SE) volume. All three of these pins are controlled with a dc voltage. These voltages are a percentage of the voltage on the 5VREF pin. The 5VREF pin sources up to 5 mA when V_{CC} = 12 V. It is specifically designed to be a reference voltage supply for the volume control that can be used with analog-to-digital converters (ADCs), resistor divider networks, and potentiometers.

When driving in BTL mode, the VOLUME pin is the only pin that controls the volume. Table 1 shows the different volumes and the corresponding voltages applied to the VOLUME pin. When driving in SE mode, all three pins can be used to control the volume. Table 2 shows the different headphone volumes and the corresponding voltages applied to each pin.

The TPA6030A4 allows the user to specify a difference between the BTL volume and the SE volume. This is desirable because it allows the user to avoid any listening discomfort when plugging in headphones. The volume in headphone mode is proportional to that in speaker mode, and is no less than 6 dB lower (refer to the section labeled *bridge−tied load versus single-ended load* for an explanation).

The SEDIFF and SEMAX pins control the difference in volume between speaker and headphone modes. As the voltage on the SEDIFF pin is increased, the difference between the BTL and SE volumes is also increased. Applying a lower voltage on the SEDIFF pin decreases the volume difference. So, for example, if the speaker volume was set to 36 dB, and SEMAX was set to 5VREF, one could vary SEDIFF to get a headphone volume from as much as 30 dB to as little as −86 dB, or mute.

The SEMAX pin can be used to set the maximum possible headphone volume. The greater the voltage applied to this pin, the higher the maximum volume. If the voltage reaches 5VREF, any volume level set by the VOLUME and SEDIFF pins passes on through to the headphones. Should the voltage on SEMAX go to 0 V, the headphones would be muted, regardless of what voltage is applied to the VOLUME and SEDIFF pins. The level set by the SEMAX pin does not affect headphone volumes below that maximum level. Table 2 shows examples of how these pins interact with each other.

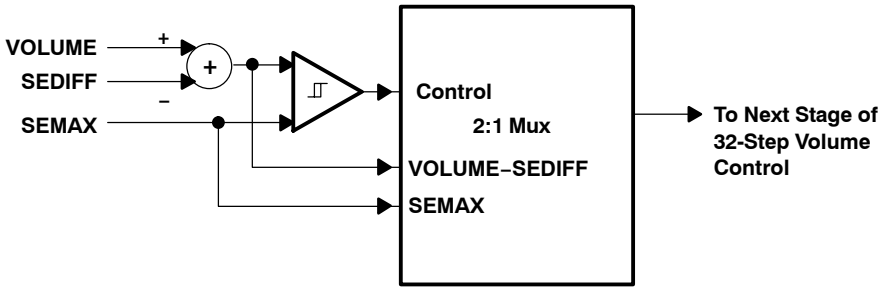


Figure 14. Block Diagram of the SE Volume Control

Table 2. Assorted Headphone and Speaker Volume Configurations

MODE	VOLTAGE ON VOLUME PIN (%5VREF)	VOLTAGE ON SEDIFF PIN (%5VREF)	VOLTAGE ON SEMAX PIN (%5VREF)	HEADPHONE VOLUME dB	SPEAKER VOLUME dB
HP	100	0	100	30	N/A
HP	0	0	100	−86	N/A
HP	100	100	0	−86	N/A
HP	60	0	100	2.13	N/A
HP	100	40	40	−18.13	N/A
HP	100	40	80	2.13	N/A
Speaker	60	0	100	N/A	8.13
Speaker	100	X	X	N/A	36
Speaker	0	X	X	N/A	−80

X = Don't care

CLOCK PIN

The TPA6030A4 has an internal clock whose frequency is controlled by the value of an external capacitor on pin 20. The relationship between the capacitor and the clock frequency is seen in Figure 15.

The clock plays a pivotal role in the functionality of the TPA6030A4. It determines how quickly the volume can change. When a voltage is applied to the VOLUME pin (or if in SE mode, the SEDIFF or SEMAX pins as well), it causes a change in volume. The volume does not change instantaneously. It moves one step for every sixteen clock cycles. For example, if the volume is initially at 36 dB in BTL mode, and then a voltage is applied to the VOLUME pin to set the volume to 0.53 dB, the volume decreases by 14 steps. With a 47-nF capacitor connected to the clock pin, the clock frequency is 390 Hz. The time it takes for the volume to reach the desired level is 574 ms. See equation 1.

$$\text{Total time} = \#\text{ of Volume Steps} \left(\frac{16}{\text{Clock Frequency}} \right) \quad (1)$$

Figure 16 demonstrates how the volume changes with respect to the clock cycles, and how the frequency of the clock affects the time necessary for each step. The triangular waveform is the voltage on the clock pin, and in this case, the clock frequency is 390 Hz. Each volume step takes 41 ms, which is consistent with equation 1.

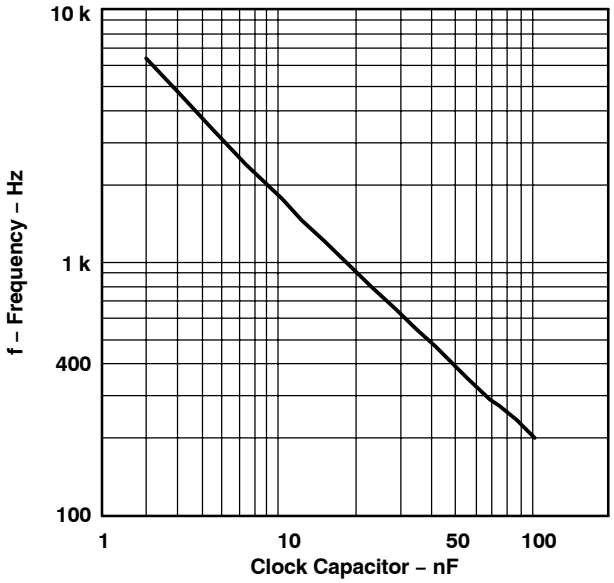


Figure 15. Clock Frequency vs Capacitance on Clock Pin

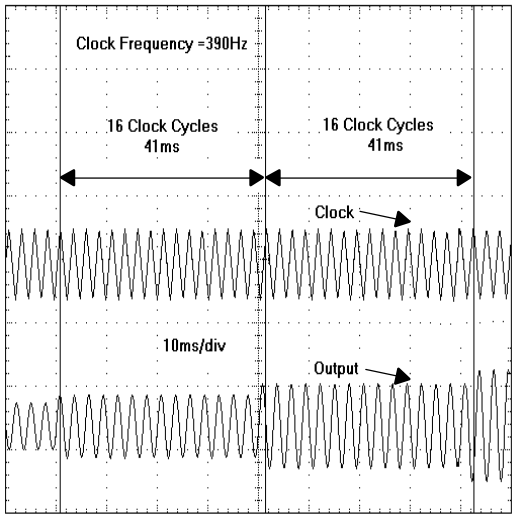


Figure 16. How the Volume Changes With Respect to the Clock

SHUTDOWN

The shutdown function of the TPA6030A4 is designed to bring all the outputs and the BYPASS pin to dc ground. The output transistors are turned off, and the current consumption of the device drops to less than 3 μA.

In order for the part to go into shutdown, the $\overline{\text{SHUTDOWN}}$ pin must be held at a logic low (0.8 V to 0 V). Once the $\overline{\text{SHUTDOWN}}$ pin is held at a logic low, the volume must ramp down to mute. The device goes through each volume step until the output is muted. That is why it takes longer for the device to shut down at higher volume levels (see Figures 17, 18, and 21). The device has to go through more steps. Once the volume is muted, the dc voltage of the outputs go to ground. The time it takes for this stage of the shutdown process is proportional to the size of the BYPASS capacitor. The smaller the capacitor, the more quickly the device shuts down. See Figure 21. However, making the BYPASS capacitor too small likely results in unwanted *pop*. The recommended range of values are between 0.1 μF to 1 μF.

The start-up time, however, is not dependent upon the volume level. Figures 19 and 20 show that the start-up time for the TPA6030A4 is not dependent upon the volume level. When the $\overline{\text{SHUTDOWN}}$ pin is held at a logic high (2 V to V_{CC}), the dc level of the outputs begin to increase. At the same time, the volume control is ramping up until it reaches the desired volume level.

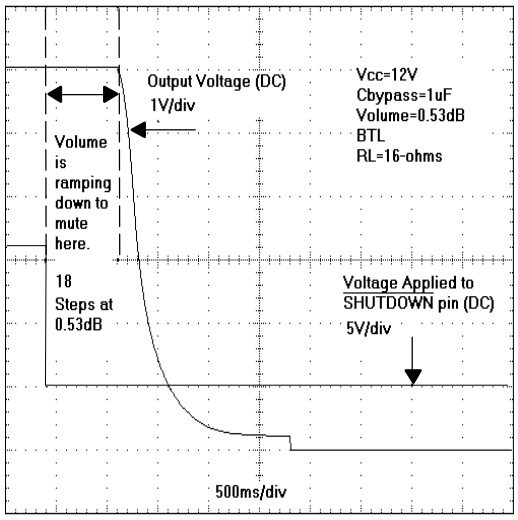


Figure 17. Shutdown Curve When the Volume = 0.53 dB

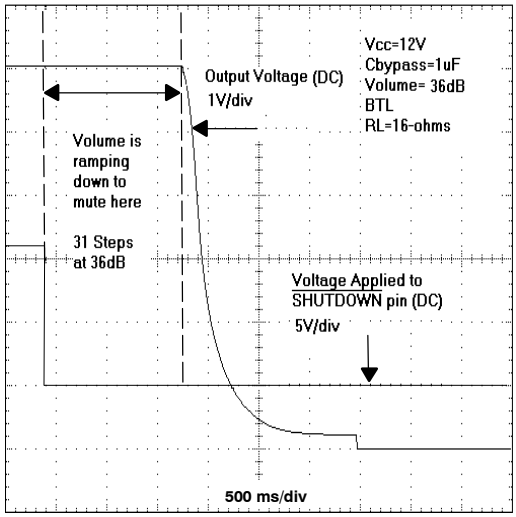


Figure 18. Shutdown Curve When the Volume = 36 dB

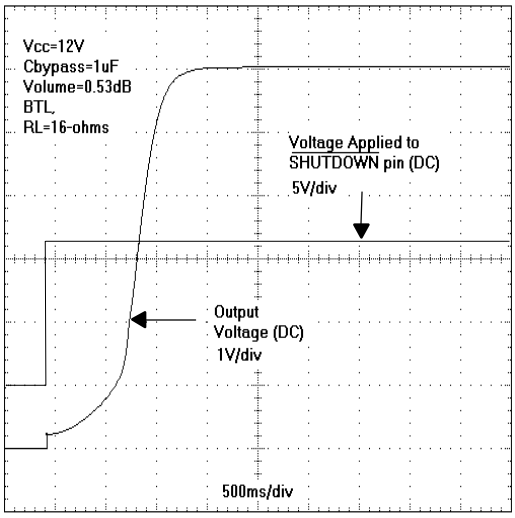


Figure 19. Start-Up Curve When the Volume = 0.53 dB

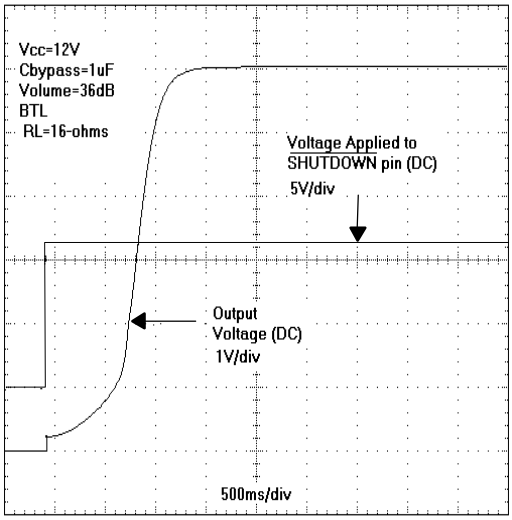


Figure 20. Start-Up Curve When the Volume = 36 dB

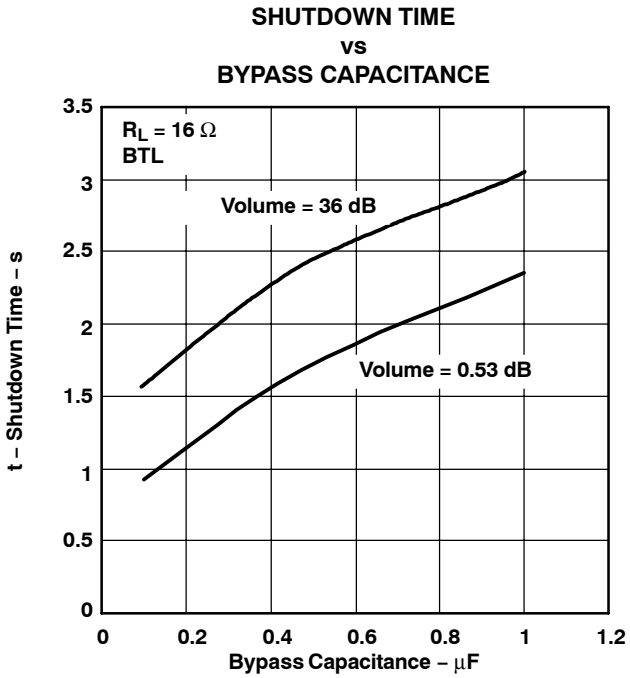


Figure 21. Shutdown Time vs Bypass Capacitance

APPLICATION CIRCUIT

Application circuit using the TPA6030A4 in an LCD monitor with headphone outputs and volume control.

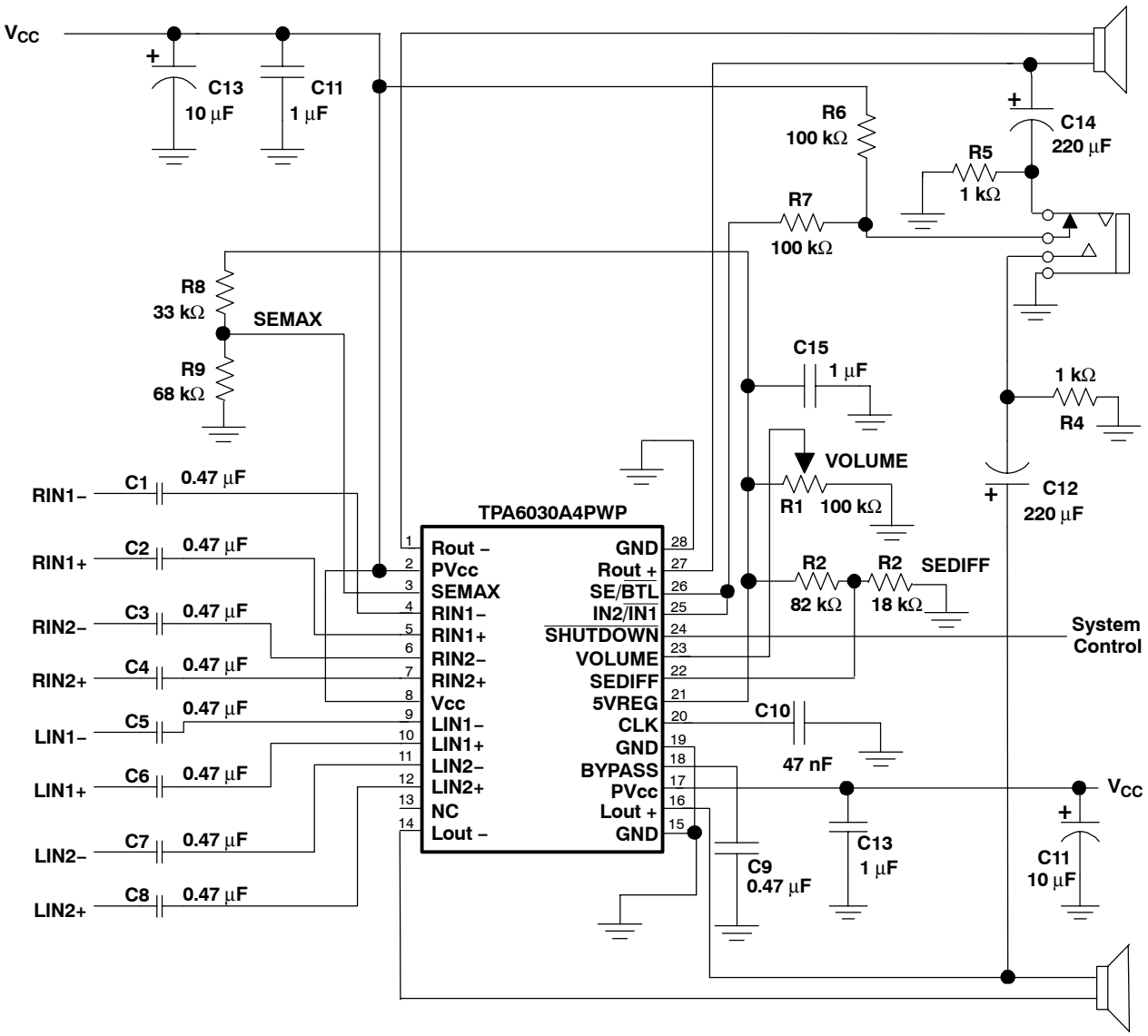


Figure 22. Typical Application Circuit for an LCD Monitor

Volume Control Description

The circuit shown in Figure 22 automatically switches between headphone outputs and speaker outputs when a headphone plug is inserted or removed from the headphone jack. Additionally, this circuit uses resistor divider networks to limit the headphone volume. Resistors R8 and R9 form a divider network that applies 67% of 5VREF to the SEMAX pin, which results in a maximum output of 7.2 dB. Resistors R2 and R3 form a divider network that applies 18% of 5VREF to the SEDIFF pin.

The effect of the resistor dividers can be observed when the output is switched from speaker to headphone mode. If the voltage on the volume pin is greater than 85% of 5VREF, the resistor divider network around SEMAX limits the headphone volume to 7.2 dB. If the voltage on the VOLUME pin falls below 85% of 5VREF, SEDIFF limits the headphone volume to 13.6 dB less than the speaker volume. To convert a percentage of 5VREF to volume in dB, refer to the column in Table 1 labeled *%5VREF*, and find the corresponding speaker volume. That value can then be substituted into the following equations for VOLUME, SEDIFF, or SEMAX. It is important, however, to find the minimum based on the %5VREF *before* converting to dB.

$$\text{SE Volume} = \min\left[(\text{VOLUME} - \text{SEDIFF}) \text{ or } (\text{SEMAX})\right] - 6 \text{ dB} \quad (2)$$

When the voltage on the VOLUME pin is > 85% of 5VREF, or at 90% of 5VREF for example, the headphone volume is determined by the following equation:

$$\text{SE Volume} = \min\left[(90\%5\text{VREF} - 18\%5\text{VREF}) \text{ or } (67\%5\text{VREF})\right] - 6 \text{ dB} =$$

$$67\%5\text{VREF} - 6\text{dB} = 13.2 \text{ dB} - 6 \text{ dB} = 7.2 \text{ dB} \quad (3)$$

When the voltage on the VOLUME pin is < 85% of 5VREF, or at 50% of 5VREF for example, the headphone volume is determined by the following equation:

$$\text{SE volume} = \min\left[(50\%5\text{VREF} - 18\%5\text{VREF}) \text{ or } (67\%5\text{VREF})\right] - 6 \text{ dB} =$$

$$32\%5\text{VREF} - 6 \text{ dB} = -19.73 \text{ dB} - 6 \text{ dB} = -25.73 \text{ dB} \quad (4)$$

When the voltage on the VOLUME pin = 85% of 5VREF, both SEMAX and SEDIFF have the same affect on the headphone volume.

$$\text{SE Volume} = \min\left[(85\%5\text{VREF} - 18\%5\text{VREF}) \text{ or } (67\%5\text{VREF})\right] - 6 \text{ dB} =$$

$$67\%5\text{VREF} - 6 \text{ dB} = 13.2 \text{ dB} - 6 \text{ dB} = 7.2 \text{ dB} \quad (5)$$

–46 dB is the lowest the SE volume can go without going into mute. So, for example, if the end calculation for the SE volume was –50 dB, the actual volume would be mute.

It is important to note that the evaluation module (EVM) for the TPA6030A4, SLOP365, does not have fixed resistors for setting the voltages on the VOLUME, SEDIFF, and SEMAX pins. It has potentiometers in place of the resistor divider networks for added flexibility. Potentiometers may be used in an application as well.

Another method of controlling the voltage on the SEDIFF and SEMAX pins would be to apply the voltage with an external controller, using 5VREF as a reference voltage.

Input Capacitor, C_I

The input capacitor allows the amplifier to bias the input signal to the proper dc level for proper operation. In this case, the input capacitor, C_I, and the input impedance of the amplifier, R_I, form a high-pass filter with the corner frequency determined in equation 6. Figure 23 shows how the input capacitor and the input resistor within the amplifier interact.

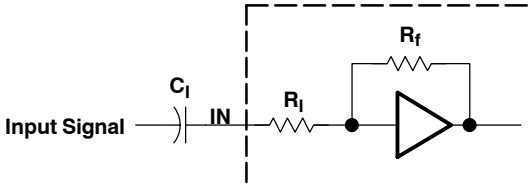
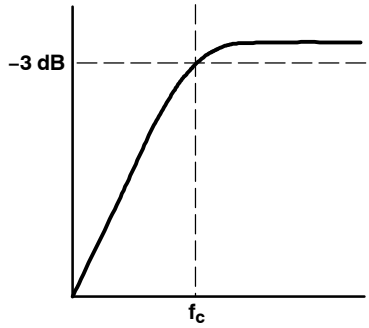


Figure 23. Input Resistor and Input Capacitor

$$f_{c(highpass)} = \frac{1}{2\pi R_I C_I} \quad (6)$$



The value of C_I is important to consider as it directly affects the low frequency, or bass, performance of the circuit. Futhermore, the input impedance changes with a change in volume. The higher the volume, the lower the input impedance. To determine the appropriate capacitor value, reconfigure equation 6 into equation 7. The value of the input resistor, R_I, can be determined from Figure 12.

$$C_I = \frac{1}{2\pi R_I f_c} \quad (7)$$

Low leakage tantalum or ceramic capacitors are recommended. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications as the dc level there is held at $V_{CC}/2$, which is likely higher than the source dc level. Note that it is important to confirm the capacitor polarity in each specific application. Recommended capacitor values are between 0.1 μF and 1 μF.

Power Supply Decoupling, C_S

The TPA6030A4 is a high-performance audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types to reduce different types of noise on the power supply leads. For higher frequency transients, spikes, or digital noise on the power supply, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1 μF, should be placed as close as possible to the device V_{CC} pin. For filtering lower frequency noise signals, a larger aluminum electrolytic capacitor of 10 μF or greater should be placed near the audio power amplifier.

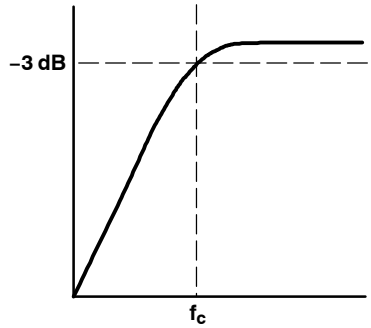
Midrail Bypass Capacitor, $C_{(BYPASS)}$

The midrail bypass capacitor, $C_{(BYPASS)}$, has several important functions. During start-up or recovery from shutdown mode, $C_{(BYPASS)}$ determines the rate at which the amplifier starts up. $C_{(BYPASS)}$ also reduces noise coupled into the output signal by the power supply. Generally, ceramic or tantalum low-ESR capacitors with values ranging from 0.1 μF to 1.0 μF are recommended for the best THD and noise performance.

Output Coupling Capacitor, C_C

In a typical single-supply SE configuration, an output coupling capacitor, C_C, is required to block the dc bias at the output of the amplifier, thus preventing dc currents from flowing through the load. This in turn reduces the current draw of the amplifier significantly. As with the input coupling capacitor, the output coupling capacitor and impedance of the load form a high pass filter governed by equation 8.

$$f_{c(highpass)} = \frac{1}{2\pi R_L C_C} \quad (8)$$



Large values of C_C are required to pass low frequencies to the load. Consider an example where C_C is 220 μF, and the load varies from 16 Ω, 32 Ω, 10 kΩ, and 47 kΩ. Table 3 summarizes the frequency response characteristics of each of the preceding configurations.

Table 3. Load Impedances vs Low Frequency Characteristics in SE Mode

R_L (Ω)	C_C (μF)	LOWEST FREQUENCY (Hz)
16	220	45
32	220	23
10k	220	0.07
47k	220	0.015

Using Low-ESR Capacitors

Low-ESR capacitors are recommended throughout this applications section. A real (as opposed to ideal) capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across the resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance, the more the real capacitor behaves like an ideal capacitor.

Bridge-Tied Load Versus Single-Ended Mode

Figure 24 shows a Class-AB audio power amplifier (APA) in a bridge-tied-load (BTL) configuration. The TPA6030A4 amplifier consists of two Class-AB differential amplifiers driving both the positive and negative terminals of the load (per channel). Specifically, differential drive means that as one side amplifier (the positive terminal, for example) is slewing up, the other side is slewing down, and vice versa. This doubles the voltage swing across the load as opposed to a ground-referenced load, or a single-ended load. Power is proportional to the square of the voltage. Plugging 2x $V_{O(PP)}$ into the power equation yields 4X the output power from the same supply rail and load impedance as would have been obtained with a ground referenced load (see equation 9).

$$V_{(RMS)} = \frac{V_{O(PP)}}{2\sqrt{2}} \quad (9)$$

$$\text{Power} = \frac{V_{(RMS)}^2}{R_L}$$

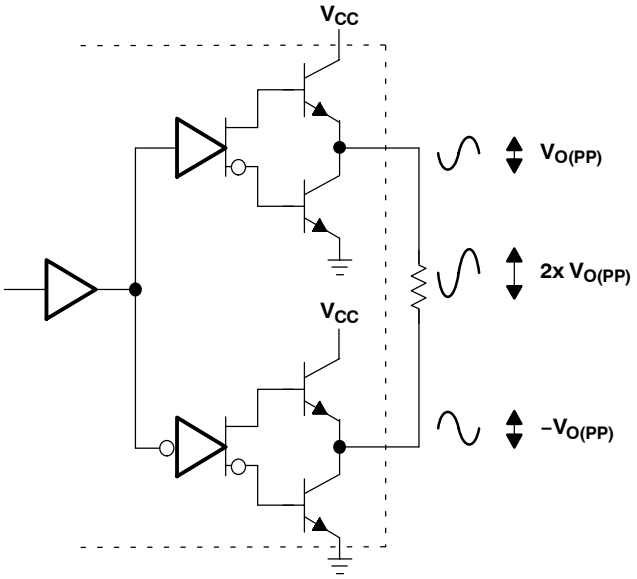


Figure 24. Bridge-Tied-Load Configuration

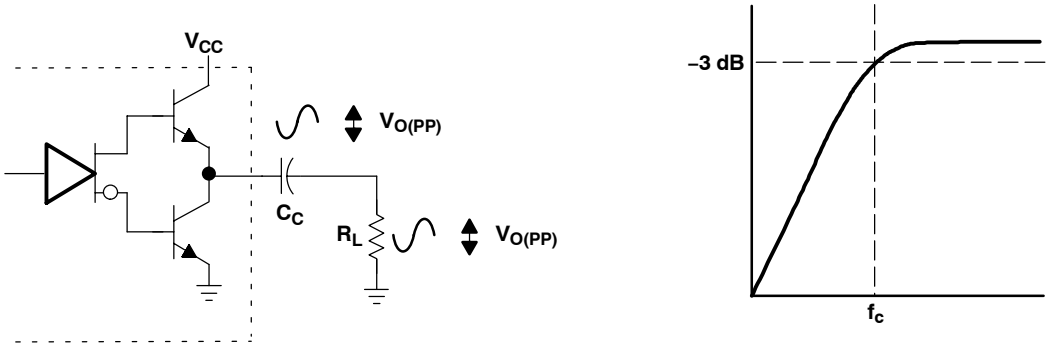


Figure 25. Single-Ended Configuration and Frequency Response

Bridge-tying the outputs in a typical computer audio, or LCD TV or multimedia LCD monitor application drastically increases output power. For example, if an amplifier in a single-ended configuration was capable of outputting a maximum of 250 mW for a given load with a supply voltage of 12 V, then that same amplifier would be able to output 1 W of power in a BTL configuration with the same supply voltage and load. In addition to the increase in output power, the BTL configuration does not suffer from the same low frequency issues that plague the single-ended configuration. In a BTL configuration, there is no need for an output capacitor to block dc, so no unwanted filtering occurs. In addition, the BTL configuration saves money and space, as the dc-blocking capacitors needed for single-ended operation are large and expensive. For example, with an 8-Ω load in SE operation, the user needs a capacitor of 995 μF to obtain a lower cutoff frequency of 20 Hz. This capacitor would be very expensive and very large.

Single-Ended Operation

Figure 25 shows a Class-AB audio power amplifier in an SE configuration. In SE mode, the load is driven from the primary amplifier for each channel (Rout+ and Lout+, terminals 27 and 16 respectively). The amplifier switches from BTL to SE mode when the SE/$\overline{\text{BTL}}$ pin is held high(1). This puts the negative outputs of the amplifier into a high impedance state, and reduces the amplifier's gain according to the voltage applied to SEDIFF and SEMAX.

SE/$\overline{\text{BTL}}$ Operation

The ability of the TPA6030A4 to easily switch between BTL and SE modes is one of its most important cost saving features. This feature eliminates the requirement for an additional headphone amplifier in applications where internal stereo speakers are driven in BTL mode but an external headphone must be accommodated. The follower amplifiers that drive Rout– and Lout– (terminals 1 and 14) are controlled by the SE/$\overline{\text{BTL}}$ input (terminal 26). When SE/$\overline{\text{BTL}}$ is held low(1), the amplifiers are on and the TPA6030A4 is in the BTL mode. When SE/$\overline{\text{BTL}}$ is held high(1), only the positive output amplifiers are on. The negative outputs enter a high impedance state, which configures the TPA6030A4 as an SE driver from the Rout+ and Lout+ outputs (terminals 27 and 16). Control of the SE/$\overline{\text{BTL}}$ input can be from a separate voltage source or, more typically, from a resistor divider network. See Figure 26 for an example of a resistor divider network.

Using a readily available 1/8-in. (3,5 mm) stereo headphone jack, the control switch is closed when no plug is inserted. When closed, the parallel combination of R5 and R7 (see Figure 22) pulls the SE/$\overline{\text{BTL}}$ pin low(1), causing the device to operate in BTL mode. When a plug is inserted, the 1-kΩ resistor is disconnected and the SE/$\overline{\text{BTL}}$ input is pulled high(1). When the input goes high(1), the negative output amplifiers go into a state of high impedance, essentially open circuiting the speaker. The positive output amplifiers then drive through the output capacitor (C_O) into the headphone jack.

IN2/$\overline{\text{IN1}}$ Operation

The TPA6030A4 has the ability to switch between the two input sources. Those sources are dubbed IN2 and IN1. There is no functional difference between the two inputs. Both perform equally well with any audio signal (provided that signal is within the specified limits set forth earlier in this document). However, only one input at a time is allowed through to the output. IN2/$\overline{\text{IN1}}$ (terminal 26) controls which input is allowed into the amplifier. As with SE/$\overline{\text{BTL}}$, IN2/$\overline{\text{IN1}}$ can be controlled by either a separate voltage source or, more typically, from a resistor divider network. See Figure 26 for an example of a resistor divider network.

(1) Refer to the table entiled *Recommended Operating Conditions*.

Tying the SE/$\overline{\text{BTL}}$ and IN2/$\overline{\text{IN1}}$ Pins Together

In some applications, it may be desirable to have one input specifically for BTL operation and one input specifically for SE operation. This is accomplished by tying the SE/$\overline{\text{BTL}}$ and IN2/$\overline{\text{IN1}}$ pins together and connecting them to a common control voltage. An example of this type of configuration can be found in Figure 22. The two pins are tied together and are connected to the resistor divider network. That network is connected to the stereo headphone jack, and is closed when no plug is inserted. This pulls both the IN2/$\overline{\text{IN1}}$ and SE/$\overline{\text{BTL}}$ pins low, causing the amplifier to go into BTL mode using the IN1 (RIN1 and LIN1) inputs. Should a headphone plug be inserted into the headphone jack, both inputs would be pulled high, and the amplifier would be in SE mode using the IN2 inputs.

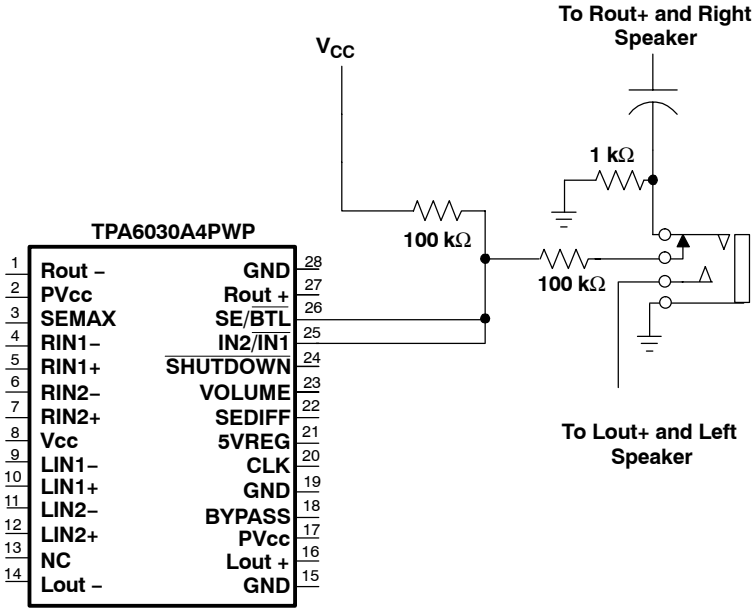


Figure 26. Resistor Divider Network

THERMAL INFORMATION

Class-AB amplifiers are inefficient. The primary cause of these inefficiencies is a voltage drop across the output stage transistors. There are two components of the internal voltage drop. One is the headroom or dc voltage drop that varies inversely to output power. The second component is due to the sinewave nature of the output. The total voltage drop can be calculated by subtracting the RMS value of the output voltage from V_{CC}. The internal voltage drop multiplied by the average value of the supply current, I_{CC}avg, determines the internal power dissipation of the amplifier.

An easy-to-use equation to calculate efficiency starts out as being equal to the ratio of power from the power supply to the power delivered to the load. To accurately calculate the RMS and average values of power in the load and in the amplifier, the current and voltage waveform shapes must first be understood (see Figure 27).

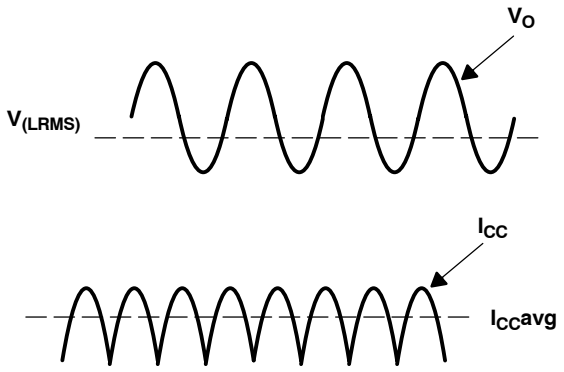


Figure 27. Voltage and Current Waveforms for BTL Amplifiers

Although the voltages and currents for SE and BTL are sinusoidal in the load, currents from the supply are very different between SE and BTL configurations. In an SE application the current waveform is a half-wave rectified waveform, whereas in BTL it is a full-wave rectified waveform. This means RMS conversion factors are different. Keep in mind that for most of the waveform both the push and pull transistors are not on at the same time, which supports the fact that each amplifier in the BTL device only draws current from the supply for half the waveform. The following equations are the basis for calculating amplifier efficiency:

$$\text{Efficiency of a BTL amplifier} = \frac{P_L}{P_{SUP}} \tag{10}$$

where:

$$P_L = \frac{V_{LRMS}^2}{R_L}, \text{ and } V_{LRMS} = \frac{V_P}{\sqrt{2}}, \text{ therefore, } P_L = \frac{V_P^2}{2R_L} \text{ per channel}$$

$$P_{SUP} = V_{CC} I_{CC}avg + V_{CC} I_{CC(q)}$$

$$\text{and } I_{CC}avg = \frac{1}{\pi}\int_0^{\pi} \frac{V_P}{R_L} \sin(t)\, dt = -\frac{V_P}{\pi R_L}\left[\cos(t)\right]_0^{\pi} = \frac{2V_P}{\pi R_L} \tag{11}$$

$$\text{where } V_P = \sqrt{2\, P_L\, R_L}$$

therefore,

$$P_{SUP} = \frac{2\, V_{CC}\, V_P}{\pi R_L} + V_{CC}\, I_{CC(q)} \tag{12}$$

P_L = Power delivered to load (per channel)
P_{SUP} = Power drawn from power supply
V_{LRMS} = RMS voltage on BTL load
R_L = Load resistance
V_P = Peak voltage on BTL load
I_{CC}avg = Average current drawn from the power supply
V_{CC} = Power supply voltage
η_{BTL} = Efficiency of a BTL amplifier
η_{SE} = Efficiency of a SE amplifier

Equation 12 represents the power drawn from the supply during mono operation. For stereo operation, the first term of equation 12 is doubled while the second term in the equation, quiescent power, does not change.

Equation 13 represents the power drawn from the supply during stereo operation.

$$P_{SUP(stereo)} = \frac{4\,V_{CC}V_P}{\pi R_L} + V_{CC}\,I_{CC(q)} \tag{13}$$

Substituting P_L and P_{SUP} into equation 10:

$$\eta_{BTL(stereo)} = \frac{2\,P_L}{\frac{4V_{CC}V_P}{\pi R_L} + V_{CC}\,I_{CC(q)}} = \frac{2\pi\,P_L\,R_L}{4V_{CC}V_P + V_{CC}\,I_{CC(q)}\,\pi R_L}$$

Note the factor of 2 in the numerator for stereo operation.
Recall that:

$$V_P = \sqrt{2\,P_L\,R_L}$$

therefore,

$$\eta_{BTL(stereo)} = \frac{2\pi\,P_L\,\sqrt{R_L}}{4V_{CC}\,\sqrt{2P_L} + V_{CC}\,I_{CC(q)}\,\pi\sqrt{R_L}} \tag{14}$$

For SE operation, the current waveform is halfwave rectified. Therefore, I_{CC}avg must be recalculated.

In an SE system:

$$I_{CCavg} = \frac{1}{\pi}\int_0^{\frac{\pi}{2}} \frac{V_P}{R_L}\sin(t)\,dt = -\frac{V_P}{\pi R_L}\left[\cos(t)\right]_0^{\frac{\pi}{2}} = \frac{V_P}{\pi\,R_L} \tag{15}$$

therefore,

$$P_{SUP} = \frac{V_{CC}V_P}{\pi\,R_L} + V_{CC}\,I_{CC(q)} \tag{16}$$

Stereo operation has the same effect in SE as it does in BTL when doubling the first term of the equation dealing with power drawn from the supply (equation 16).

$$P_{SUP(stereo)} = \frac{2\,V_{CC}V_P}{\pi\,R_L} + V_{CC}\,I_{CC(q)} \tag{17}$$

Following the same steps for SE operation as in BTL operation:

$$\eta_{SE(stereo)} = \frac{2\,P_L}{\frac{2\,V_{CC}V_P}{\pi\,R_L} + V_{CC}\,I_{CC(q)}} = \frac{2\pi\,P_L\,R_L}{2V_{CC}V_P + V_{CC}\,I_{CC(q)}\,\pi R_L}$$

Recall that:

$$V_P = \sqrt{2\,P_L\,R_L}$$

therefore,

$$\eta_{SE(stereo)} = \frac{2\pi\,P_L\,\sqrt{R_L}}{2V_{CC}\sqrt{2P_L} + V_{CC}\,I_{CC(q)}\,\pi\sqrt{R_L}} \tag{18}$$

Figures 28 through 31 demonstrate how the maximum ambient temperature changes with respect to V_{CC}, R_L, and the derating factor.

Table 4. Efficiency and Maximum Ambient Temperature vs Output Power in 12-V Stereo 16-Ω BTL Systems(1)

OUTPUT POWER (PER CHANNEL) (W)	EFFICIENCY (%)	INTERNAL DISSIPATION (W)	POWER FROM SUPPLY (W)	MAX AMBIENT TEMPERATURE (°C)
0.25	17.1	2.4	2.92	82
0.50	24.8	3.0	4.04	65
1	35.6	3.6	5.62	49
2	50.9	3.9	7.88	42
3	62.7	3.6	9.57	50

(1) $I_{CC(q)}$ = 18 mA as shown in the electrical characteristics table.

Table 5. Efficiency and Maximum Ambient Temperature vs Output Power in 12-V Stereo 8-Ω SE Systems(2)

OUTPUT POWER (PER CHANNEL) (W)	EFFICIENCY (%)	INTERNAL DISSIPATION (W)	POWER FROM SUPPLY (W)	MAX AMBIENT TEMPERATURE (°C)
0.05	10.1	0.89	0.99	125
0.1	14.9	1.14	1.34	118
0.25	24.5	1.54	2.04	107
0.5	35.3	1.13	2.83	99
0.75	43.6	1.94	3.44	96
1	50.6	1.95	3.95	95

(2) $I_{CC(q)}$ = 11 mA as shown in the electrical characteristics table.

Tables 4 and 5 employ equations 14 and 18 respectively to calculate efficiencies for different output power levels. Calculating the efficiency for a specific system is the key to proper power supply design. For a stereo 3-W audio system with 16-Ω loads and a 12-V supply, the maximum draw on the power supply is almost 9.6 W.

A final point to remember about Class-AB amplifiers is how to manipulate the terms in the efficiency equations to the best advantage when possible. Note that in equations 14 and 18, V_{CC} is in the denominator. This indicates that as V_{CC} goes down, efficiency goes up. Additionally, R_L appears in both the numerator and denominator. Since the more dominant term is in the numerator, as R_L goes up, the efficiency goes up.

A simple formula for calculating the power dissipated, P_{DISS}, is as follows:

$$P_{DISS} = (1-\eta)P_{SUP}$$

The maximum ambient temperature, T_A, depends on the heat sinking ability of the PCB system. The derating factor for a 28-pin PWP is shown in the dissipation rating table.
Converting this to θ_{JA}:

$$\Theta_{JA} = \frac{1}{\text{Derating Factor}} = \frac{1}{0.0358} = 27.93°C/W \quad (19)$$

Given Θ_{JA}, the maximum allowable junction temperature, and the maximum internal dissipation, the maximum ambient temperature can be calculated using equation 21. The maximum recommended junction temperature for the TPA6030A4 is 150°C.

$$T_A\,\text{Max} = T_J\,\text{Max} - \Theta_{JA}\,P_{Diss} \quad (20)$$

The maximum ambient temperature for the TPA6030A4 operating with a 12-V supply, and driving 3 W into 16-Ω loads (stereo operation) is:

$$T_A\,\text{Max} = 150 - 27.93\,(3.6) = 50.2°C$$

MAXIMUM AMBIENT TEMPERATURE vs OUTPUT POWER (PER CHANNEL)

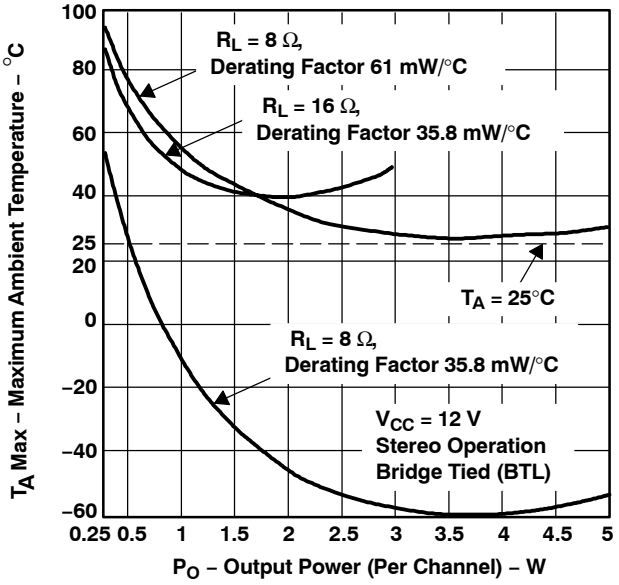


Figure 28

MAXIMUM AMBIENT TEMPERATURE vs OUTPUT POWER (PER CHANNEL)

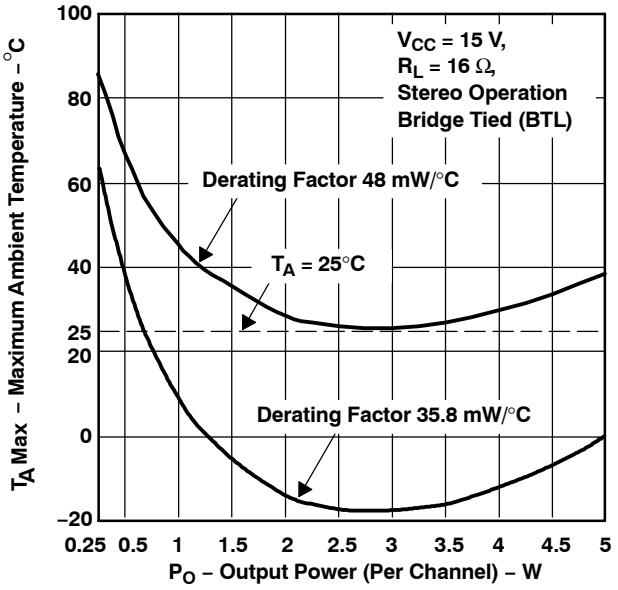


Figure 29

MAXIMUM AMBIENT TEMPERATURE vs OUTPUT POWER (PER CHANNEL)

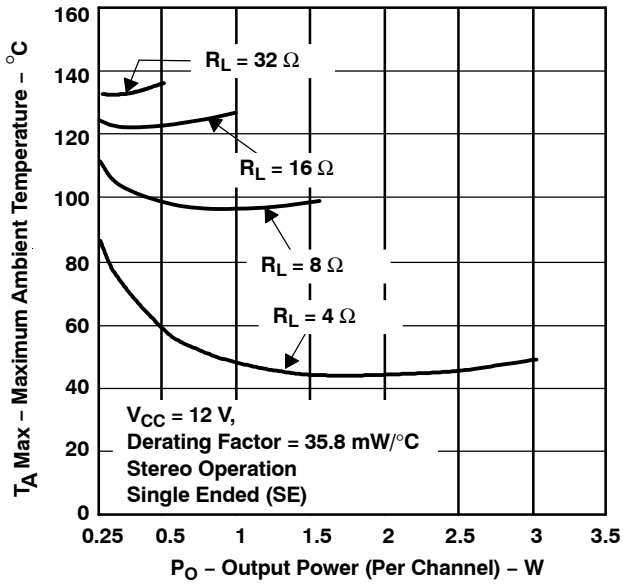


Figure 30

MAXIMUM AMBIENT TEMPERATURE vs OUTPUT POWER (PER CHANNEL)

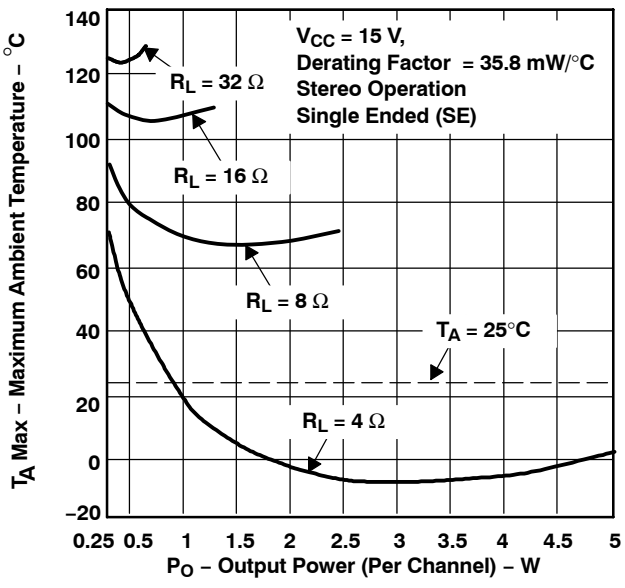


Figure 31

The derating factor is crucial for proper thermal performance. The higher the derating factor, the more power can be dissipated from the device. Board layout affects the derating factor, and should be optimized to achieve the best thermal performance. Using boards with large copper planes that are uncut by signal or power paths help tremendously. Using heavier copper, 2 oz. as opposed to 1 oz., is also beneficial. Placing the device close to a fan is another way to enhance thermal performance. Most importantly, the PowerPAD must be properly soldered down. Refer to the *PowerPAD Thermally Enhanced Package* application note (SLMA002).

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPA6030A4PWP	ACTIVE	HTSSOP	PWP	28	50	RoHS & Green	NIPDAU	Level-4-260C-72 HR	-40 to 85	TPA6030A4	Samples
TPA6030A4PWPR	ACTIVE	HTSSOP	PWP	28	2000	RoHS & Green	NIPDAU	Level-4-260C-72 HR	-40 to 85	TPA6030A4	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

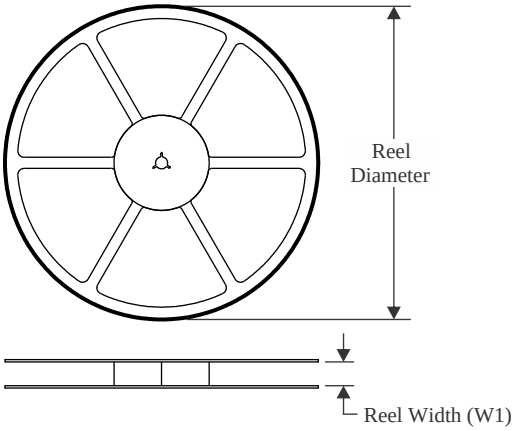
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

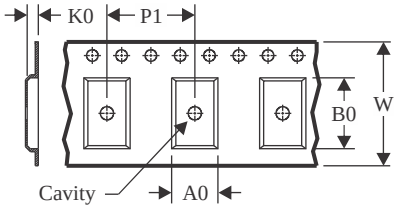
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

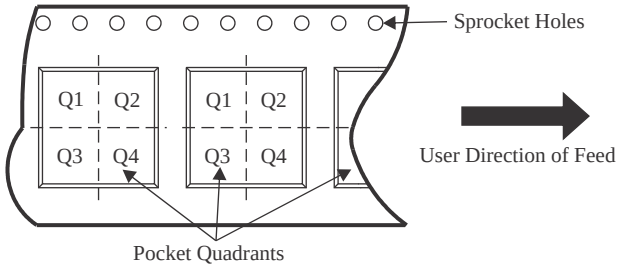


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

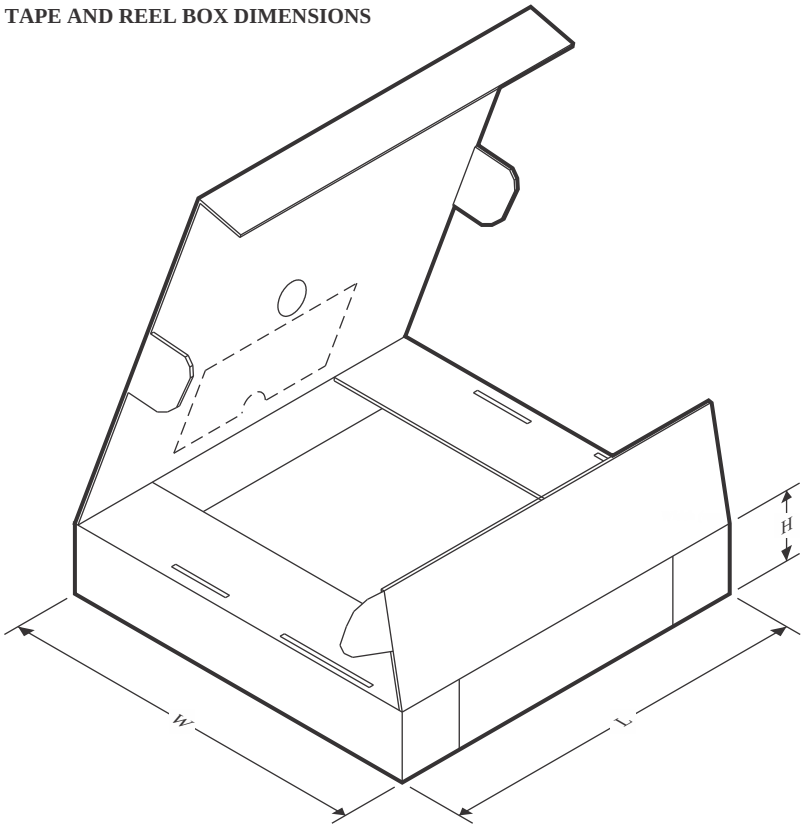
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPA6030A4PWPR	HTSSOP	PWP	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1

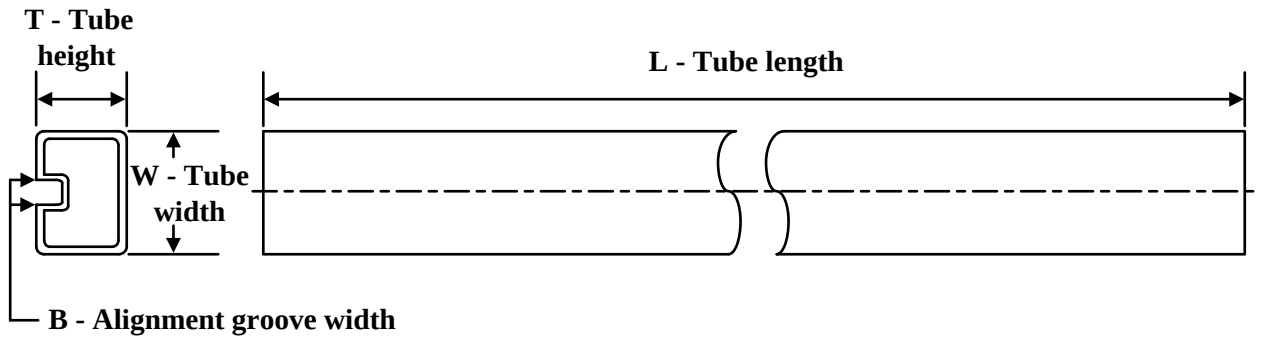
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPA6030A4PWPR	HTSSOP	PWP	28	2000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPA6030A4PWP	PWP	HTSSOP	28	50	530	10.2	3600	3.5

GENERIC PACKAGE VIEW

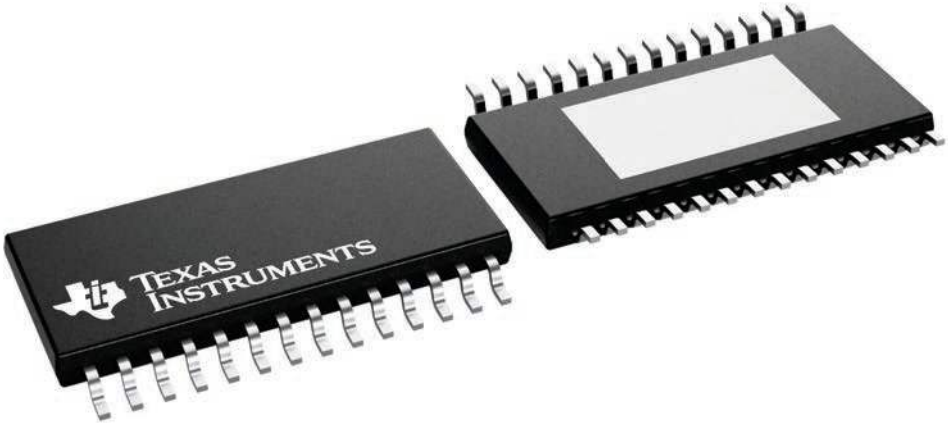
PWP 28

PowerPAD™ TSSOP - 1.2 mm max height

4.4 x 9.7, 0.65 mm pitch

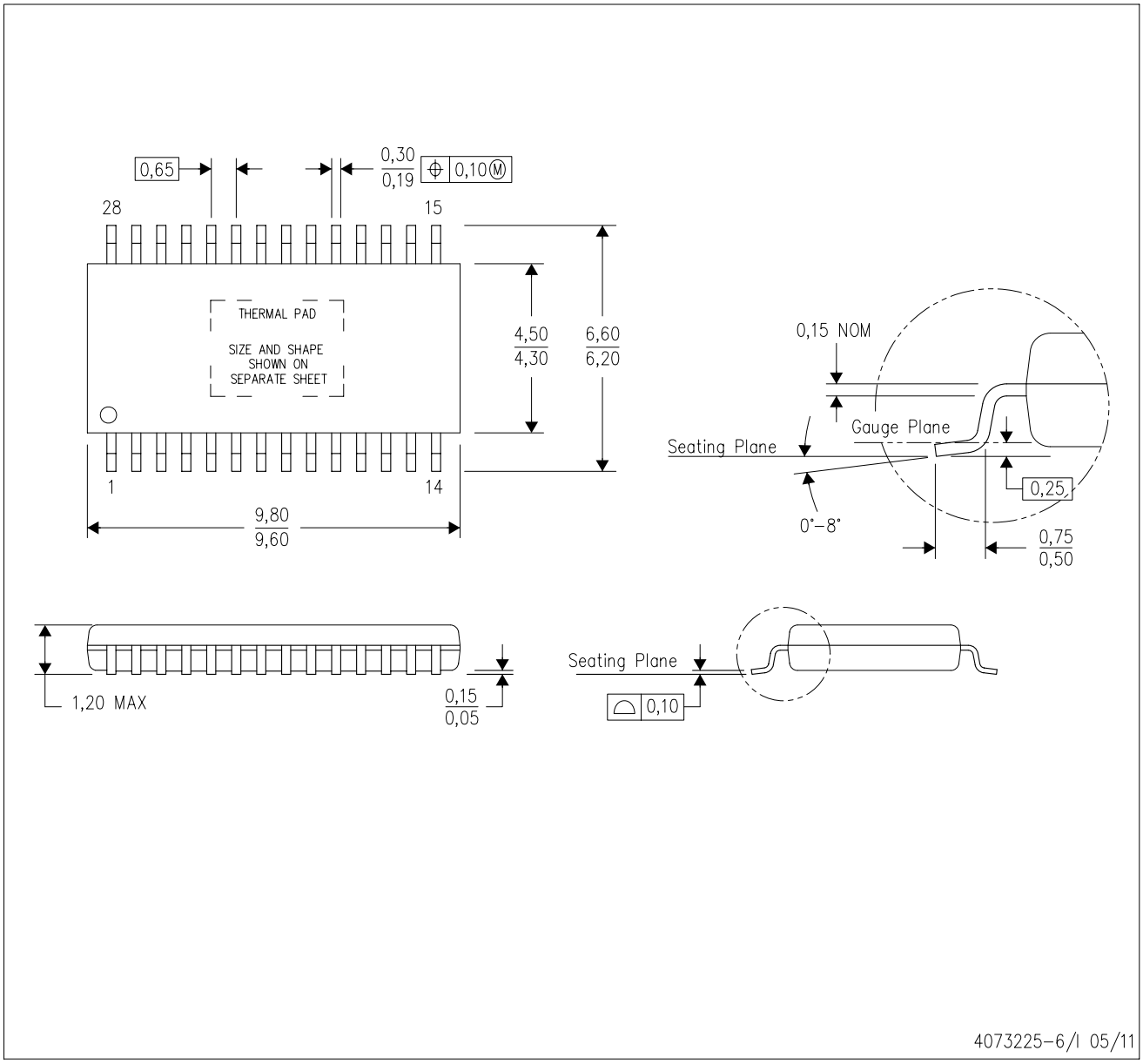
SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224765/B

PWP (R–PDSO–G28) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

PowerPAD is a trademark of Texas Instruments.

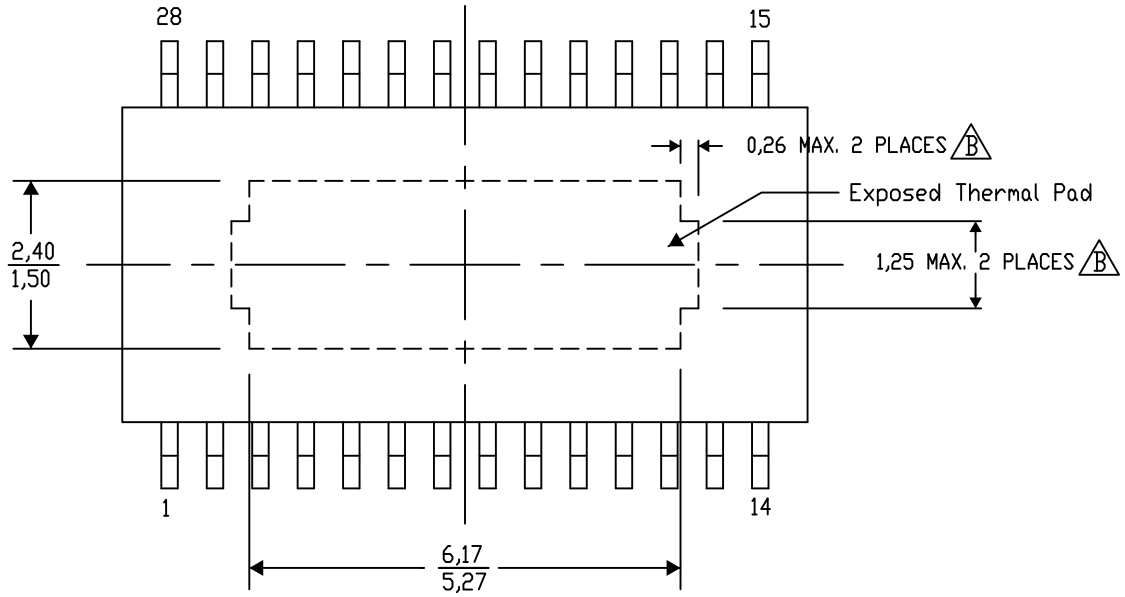
PWP (R–PDSO–G28) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

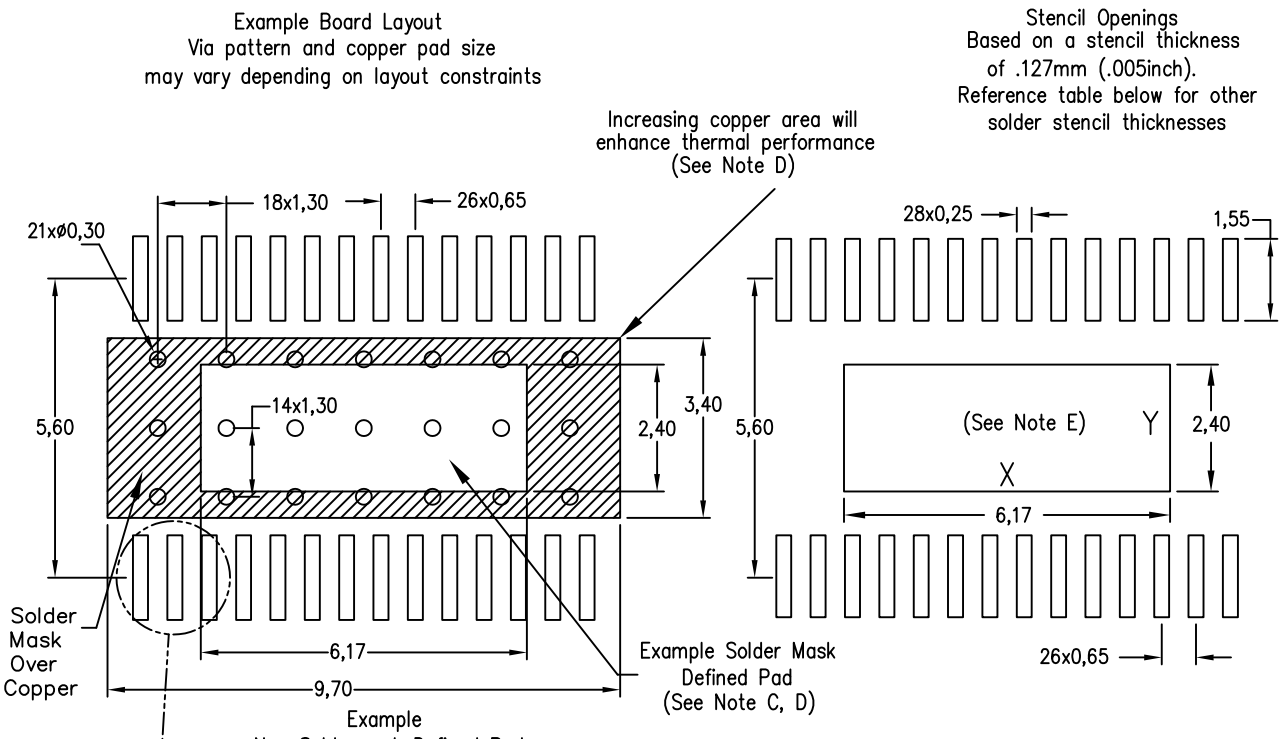
4206332–33/AO 01/16

NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PWP (R–PDSO–G28) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	6.6	2.6
0.127mm	6.17	2.4
0.152mm	5.8	2.3
0.178mm	5.6	2.2

4207609–19/W 09/15

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets.
E. For specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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