

Octal T1/E1/J1 Line Interface Unit

Features

- ❑ Industry-standard Footprint
- ❑ Octal E1/T1/J1 Short-haul Line Interface Unit
- ❑ Low Power
- ❑ No external component changes for 100 Ω/120 Ω/75 Ω operation.
- ❑ Pulse shapes can be customized by the user.
- ❑ Internal AMI, B8ZS, or HDB3 Encoding/Decoding
- ❑ LOS Detection per T1.231, ITU G.775, ETSI 300-233
- ❑ G.772 Non-Intrusive Monitoring
- ❑ G.703 BITS Clock Recovery
- ❑ Crystal-less Jitter Attenuation
- ❑ Serial/Parallel Microprocessor Control Interfaces
- ❑ Transmitter Short Circuit Current Limiter (<50mA)
- ❑ TX Drivers with Fast High-Z and Power Down
- ❑ JTAG boundary scan compliant to IEEE 1149.1.
- ❑ 144-Pin LQFP & 160-Pin LFBGA Packages

ORDERING INFORMATION

| | |
|-------------|--------------------------|
| CS61884-IQZ | 144-pin LQFP, Lead Free |
| CS61884-IRZ | 160-pin LFBGA, Lead Free |

Description

The CS61884 is a full-featured octal E1/T1/J1 short-haul LIU that supports both 1.544 Mbps or 2.048 Mbps data transmission. Each channel provides crystal-less jitter attenuation that complies with the most stringent standards. Each channel also provides internal AMI/B8ZS/HDB3 encoding/decoding. To support enhanced system diagnostics, channel zero can be configured for G.772 non-intrusive monitoring of any of the other 7 channels' receive or transmit paths.

The CS61884 makes use of ultra-low-power, matched-impedance transmitters and receivers to reduce power beyond that achieved by traditional driver designs. By achieving a more precise line match, this technique also provides superior return loss characteristics. Additionally, the internal line matching circuitry reduces the external component count. All transmitters have controls for independent power down and High-Z.

Each receiver provides reliable data recovery with over 12 dB of cable attenuation. The receiver also incorporates LOS detection compliant to the most recent specifications.

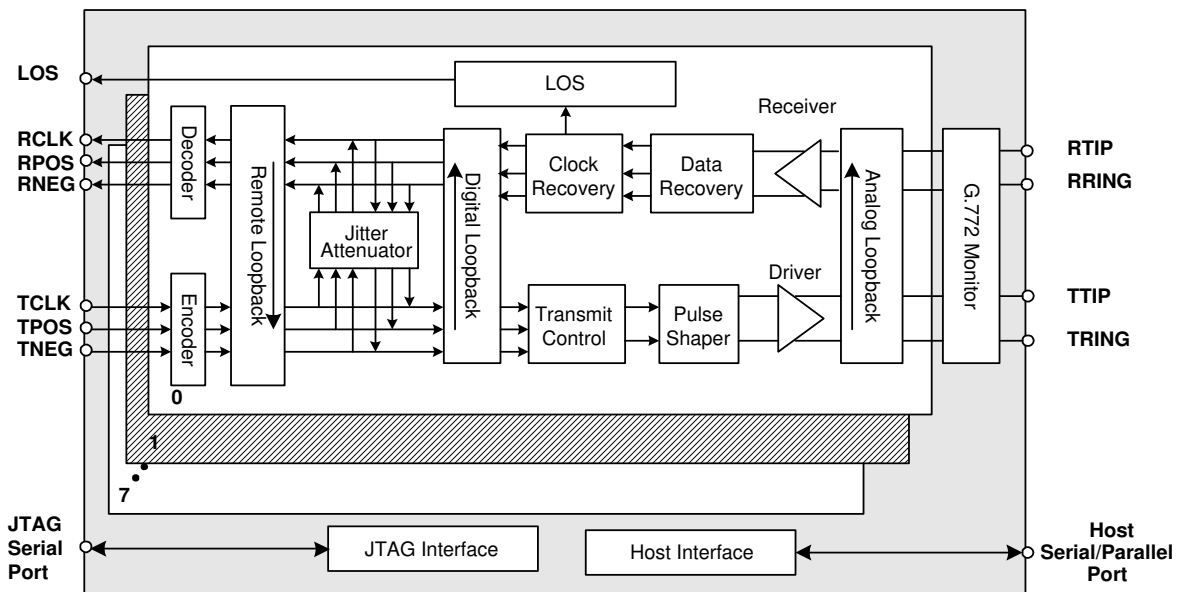


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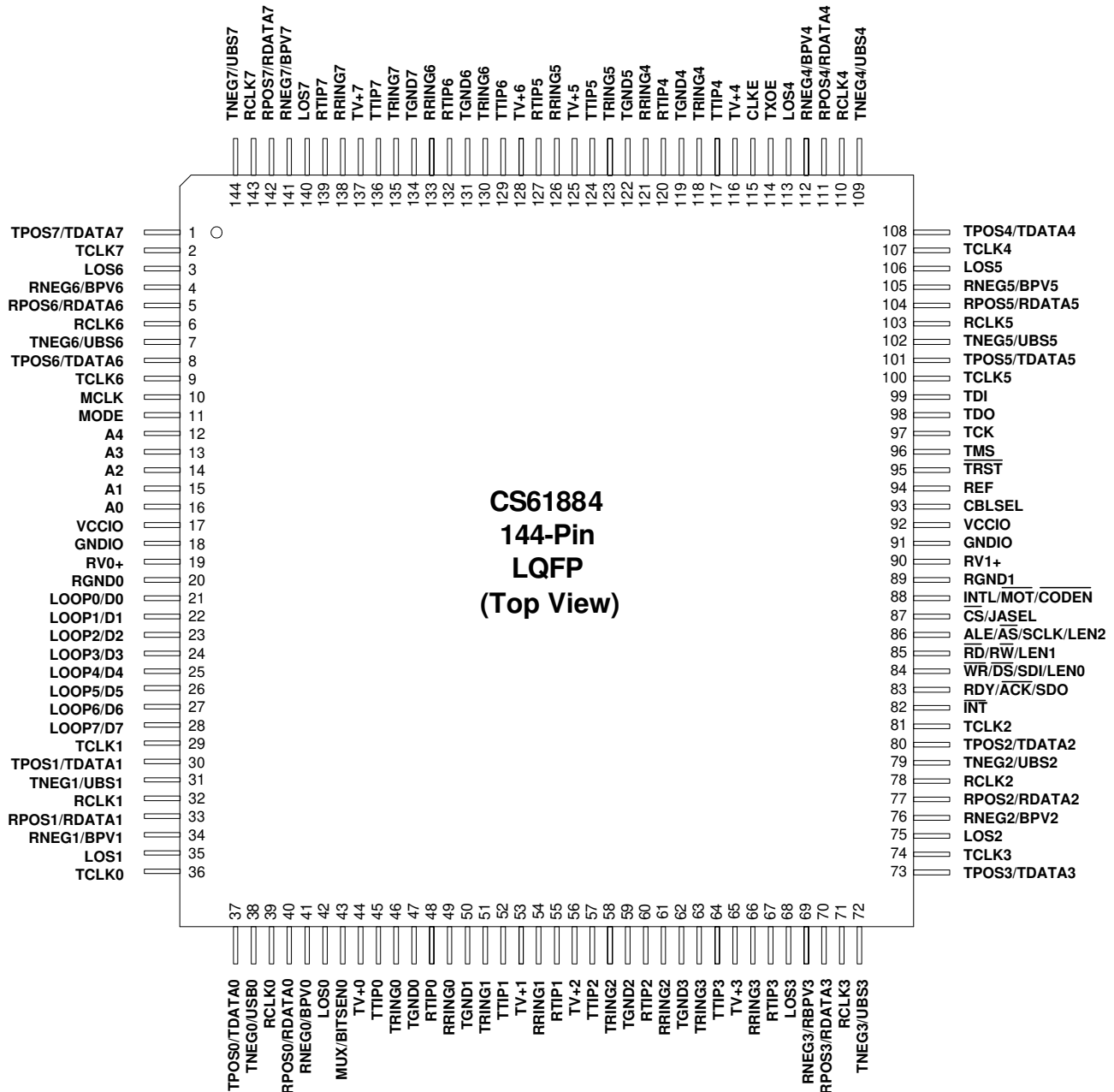
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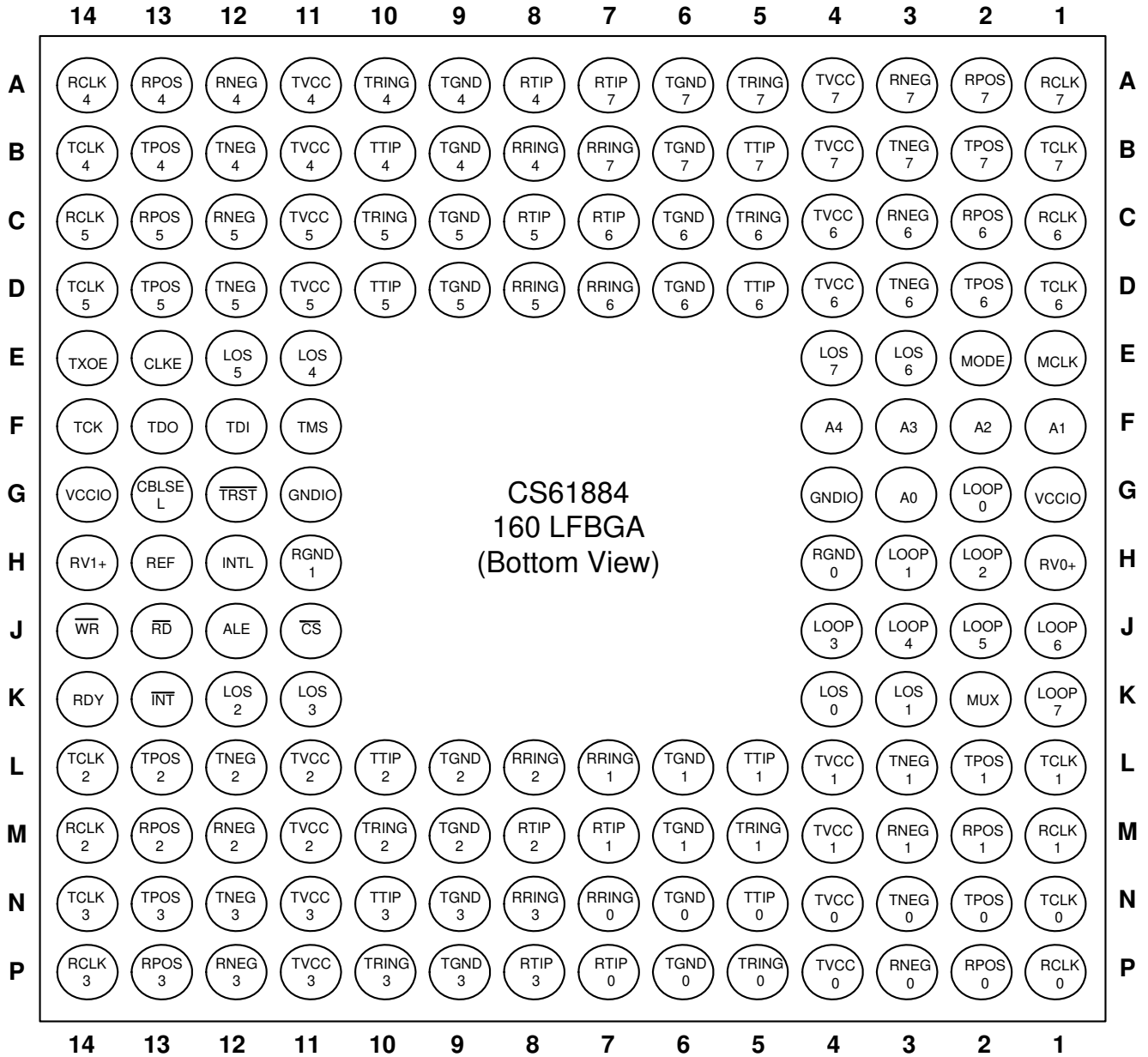
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1. PINOUT - LQFP

Figure 1. CS61884 144-LQFP Pinout

2. PINOUT - LFBGA

Figure 2. CS61884 160-Ball LFBGA Pinout

3. PIN DESCRIPTIONS

3.1 Power Supplies

| SYMBOL | LQFP | LFBGA | TYPE | DESCRIPTION |
|----------------|----------|------------|------|---|
| VCCIO | 17 92 | G1 G14 | | Power Supply, Digital Interface: Power supply for digital interface pins; typically 3.3V. |
| GNDIO | 18 91 | G4 G11 | | Ground, Digital Interface: Power supply ground for the digital interface; typically 0 Volts |
| RV0+ RV1+ | 19 90 | H1 H14 | | Power Supply, Core Circuitry: Power supply for all sub-circuits except the transmit driver; typically +3.3 Volts |
| RGND0 RGND1 | 20 89 | H4 H11 | | Ground, Core Circuitry: Ground for sub-circuits except the TX driver; typically 0 Volts |
| TV+0 | 44 | N4, P4 | | Power Supply, Transmit Driver 0 Power supply for transmit driver 0; typically +3.3 Volts |
| TGND0 | 47 | N6, P6 | | Ground, Transmit Driver 0 Power supply ground for transmit driver 0; typically 0 Volts |
| TV+1 | 53 | L4, M4 | | Power Supply, Transmit Driver 1 |
| TGND1 | 50 | L6, M6 | | Ground, Transmit Driver 1 |
| TV+2 | 56 | L11 M11 | | Power Supply, Transmit Driver 2 |
| TGND2 | 59 | L9, M9 | | Ground, Transmit Driver 2 |
| TV+3 | 65 | N11 P11 | | Power Supply, Transmit Driver 3 |
| TGND3 | 62 | N9, P9 | | Ground, Transmit Driver 3 |
| TV+4 | 116 | A11 B11 | | Power Supply, Transmit Driver 4 |
| TGND4 | 119 | A9, B9 | | Ground, Transmit Driver 4 |
| TV+5 | 125 | C11 D11 | | Power Supply, Transmit Driver 5 |
| TGND5 | 122 | C9, D9 | | Ground, Transmit Driver 5 |
| TV+6 | 128 | C4, D4 | | Power Supply, Transmit Driver 6 |
| TGND6 | 131 | C6, D6 | | Ground, Transmit Driver 6 |
| TV+7 | 137 | A4, B4 | | Power Supply, Transmit Driver 7 |
| TGND7 | 134 | A6, B6 | | Ground, Transmit Driver 7 |

3.2 Control

| SYMBOL | LQFP | LFBGA | TYPE | DESCRIPTION | | | | | | | | |
|-----------|--------------------|-------|------|--|-----------|----------------|-----|---------------|------|--------------------|---------|------------------|
| MCLK | 10 | E1 | I | <p>Master Clock Input This pin is a free running reference clock that should be either 1.544 MHz for T1/J1 or 2.048 MHz for E1 operation. This timing reference is used as follows:</p> <ul style="list-style-type: none"> - Timing reference for the clock recovery and jitter attenuation circuitry. - RCLK reference during Loss of Signal (LOS) conditions - Transmit clock reference during Transmit all Ones (TAOS) condition - Wait state timing for microprocessor interface - When this pin is held "High", the PLL clock recovery circuit is disabled. In this mode, the CS61884 receivers function as simple data slicers. - When this pin is held "Low", the receiver paths are powered down and the output pins RCLK, RPOS, and RNEG are High-Z. | | | | | | | | |
| MODE | 11 | E2 | I | <p>Mode Select This pin is used to select whether the CS61884 operates in Serial host, Parallel host or Hardware mode.</p> <p>Host Mode - The CS61884 is controlled through either a serial or a parallel microprocessor interface (Refer to HOST MODE (See Section 13 on page 32).</p> <p>Hardware Mode - The microprocessor interface is disabled and the device control/status are provided through the pins on the device.</p> <p style="text-align: center;">Table 1. Operation Mode Selection</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Pin State</th> <th>OPERATING Mode</th> </tr> </thead> <tbody> <tr> <td>LOW</td> <td>Hardware Mode</td> </tr> <tr> <td>HIGH</td> <td>Parallel Host Mode</td> </tr> <tr> <td>VCCIO/2</td> <td>Serial Host Mode</td> </tr> </tbody> </table> <p>NOTE: For serial host mode connect this pin to a resistor divider consisting of two 10KΩ resistors between VCCIO and GNDIO.</p> | Pin State | OPERATING Mode | LOW | Hardware Mode | HIGH | Parallel Host Mode | VCCIO/2 | Serial Host Mode |
| Pin State | OPERATING Mode | | | | | | | | | | | |
| LOW | Hardware Mode | | | | | | | | | | | |
| HIGH | Parallel Host Mode | | | | | | | | | | | |
| VCCIO/2 | Serial Host Mode | | | | | | | | | | | |

| SYMBOL | LQFP | LFBGA | TYPE | DESCRIPTION | | | | | | | | | |
|-----------------------------------|--------------------|----------------|------|---|-----------|--------------------|---------------|------|-------------|---------------|-----|-----------------|----------------|
| MUX/BITSEN0 | 43 | K2 | I | <p>Multiplexed Interface/Bits Clock Select Host Mode - This pin configures the microprocessor interface for multiplexed or non-multiplexed operation. Hardware mode - This pin is used to enable channel 0 as a G.703 BITS Clock recovery channel (Refer to BUILDING INTEGRATED TIMING SYSTEMS (BITS) CLOCK MODE (See Section 8 on page 23). Channel 1 through 7 are not affected by this pin during hardware mode. During host mode the G.703 BITS Clock recovery function is enabled by the Bits Clock Enable Register (1Eh) (See Section 14.31 on page 41).</p> <p style="text-align: center;">Table 2. Mux/Bits Clock Selection</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Pin State</th> <th>Parallel Host Mode</th> <th>Hardware Mode</th> </tr> </thead> <tbody> <tr> <td>HIGH</td> <td>multiplexed</td> <td>BITS Clock ON</td> </tr> <tr> <td>LOW</td> <td>non multiplexed</td> <td>BITS Clock OFF</td> </tr> </tbody> </table> <p>NOTE: The MUX pin only controls the BITS Clock function in Hardware Mode</p> | Pin State | Parallel Host Mode | Hardware Mode | HIGH | multiplexed | BITS Clock ON | LOW | non multiplexed | BITS Clock OFF |
| Pin State | Parallel Host Mode | Hardware Mode | | | | | | | | | | | |
| HIGH | multiplexed | BITS Clock ON | | | | | | | | | | | |
| LOW | non multiplexed | BITS Clock OFF | | | | | | | | | | | |
| $\overline{\text{INT}}$ | 82 | K13 | O | <p>Interrupt Output This active low output signals the host processor when one of the CS61884's internal status register bits has changed state. When the status register is read, the interrupt is cleared. The various status changes that would force $\overline{\text{INT}}$ active are maskable via internal interrupt enable registers.</p> <p>NOTE: This pin is an open drain output and requires a 10 kΩ pull-up resistor.</p> | | | | | | | | | |
| RDY/ $\overline{\text{ACK}}$ /SDO | 83 | K14 | O | <p>Data Transfer Acknowledge/Ready/Serial Data Output Intel Parallel Host Mode - During a read or write register access, RDY is asserted "Low" to acknowledge that the device has been accessed. An asserted "High" acknowledges that data has been written or read. Upon completion of the bus cycle, this pin High-Z. Motorola Parallel Host Mode - During a data bus read operation this pin "ACK" is asserted "High" to indicate that data on the bus is valid. An asserted "Low" on this pin during a write operation acknowledges that a data transfer to the addressed register has been accepted. Upon completion of the bus cycle, this pin High-Z. NOTE: Wait state generation via RDY/$\overline{\text{ACK}}$ is disabled in RZ mode (No Clock Recovery). Serial Host Mode - When the microprocessor interface is configured for serial bus operation, "SDO" is used as a serial data output. This pin is forced into a high impedance state during a serial write access. The CLKE pin controls whether SDO is valid on the rising or falling edge of SCLK. Upon completion of the bus cycle, this pin High-Z. Hardware Mode - This pin is not used and should be left open.</p> | | | | | | | | | |

| SYMBOL | LQFP | LFBGA | TYPE | DESCRIPTION | | | | | | | | |
|--|-----------------------------|-------|------|--|-----------|-----------------------------|-----|---------------|------|--------------|------|----------|
| $\overline{WR}/\overline{DS}/SDI/LEN0$ | 84 | J14 | I | <p>Data Strobe/ Write Enable/Serial Data/Line Length Input Intel Parallel Host Mode - This pin "\overline{WR}" functions as a write enable.</p> <p>Motorola Parallel Host Mode - This pin "\overline{DS}" functions as a data strobe input.</p> <p>Serial Host Mode - This pin "SDI" functions as the serial data input.</p> <p>Hardware Mode - As LEN0, this pin controls the transmit pulse shapes for both E1 and T1/J1 modes. This pin also selects which mode is used E1 or T1/J1 (Refer to Table 5 on page 25).</p> | | | | | | | | |
| $\overline{RD}/\overline{RW}/LEN1$ | 85 | J13 | I | <p>Read/Write/ Read Enable/Line Length Input Intel Parallel Host Mode - This pin "\overline{RD}" functions as a read enable.</p> <p>Motorola Parallel Host Mode - This pin "$\overline{R}/\overline{W}$" functions as the read/write input signal.</p> <p>Hardware Mode - As LEN1, this pin controls the transmit pulse shapes for both E1 and T1/J1 modes. This pin also selects which mode is used E1 or T1/J1 (Refer to Table 5 on page 25).</p> | | | | | | | | |
| $ALE/\overline{AS}/SCLK/LE N2$ | 86 | J12 | I | <p>Address Latch Enable/Serial Clock/Address Strobe/Line Length Input Intel Parallel Host Mode - This pin "ALE" functions as the Address Latch Enable when configured for multiplexed address/data operation.</p> <p>Motorola Parallel Host Mode - This pin "\overline{AS}" functions as the active "low" address strobe when configured for multiplexed address/data operation.</p> <p>Serial Host Mode - This pin "SCLK" is the serial clock used for data I/O on SDI and SDO.</p> <p>Hardware Mode - As LEN2, this pin controls the transmit pulse shapes for both E1 and T1/J1 modes. This pin also selects which mode is used E1 or T1/J1 (Refer to Table 5 on page 25).</p> | | | | | | | | |
| $\overline{CS}/JASEL$ | 87 | J11 | I | <p>Chip Select Input/Jitter Attenuator Select Host Mode - This active low input is used to enable accesses to the microprocessor interface in either serial or parallel mode.</p> <p>Hardware Mode - This pin controls the position of the Jitter Attenuator.</p> <table border="1" data-bbox="821 1587 1383 1730"> <thead> <tr> <th>Pin State</th> <th>Jitter Attenuation Position</th> </tr> </thead> <tbody> <tr> <td>LOW</td> <td>Transmit Path</td> </tr> <tr> <td>HIGH</td> <td>Receive Path</td> </tr> <tr> <td>OPEN</td> <td>Disabled</td> </tr> </tbody> </table> | Pin State | Jitter Attenuation Position | LOW | Transmit Path | HIGH | Receive Path | OPEN | Disabled |
| Pin State | Jitter Attenuation Position | | | | | | | | | | | |
| LOW | Transmit Path | | | | | | | | | | | |
| HIGH | Receive Path | | | | | | | | | | | |
| OPEN | Disabled | | | | | | | | | | | |

| SYMBOL | LQFP | LFBGA | TYPE | DESCRIPTION |
|--|------|-------|------|---|
| INTL/ $\overline{\text{MOT}}/\overline{\text{CODE}}/\overline{\text{N}}$ | 88 | H12 | I | <p>Motorola/Intel/Coder Mode Select Input</p> <p>Parallel Host Mode - When this pin is “Low” the microprocessor interface is configured for operation with Motorola processors. When this pin is “High” the microprocessor interface is configured for operation with Intel processors.</p> <p>Hardware Mode - When the CS61884 is configured for unipolar operation, this pin, CODEN, configures the line encoding/decoding function. When CODEN is low, B8ZS/HDB3 encoders/decoders are enabled for T1/J1 or E1 operation respectively. When CODEN is high, AMI encoding/decoding is activated. This is done for all eight channels.</p> |
| TXOE | 114 | E14 | I | <p>Transmitter Output Enable</p> <p>Host mode - Operates the same as in hardware mode. Individual drivers can be set to a high impedance state via the Output Disable Register (12h) (See Section 14.19 on page 39).</p> <p>Hardware Mode - When TXOE pin is asserted Low, all the TX drivers are forced into a high impedance state. All other internal circuitry remains active.</p> |
| CLKE | 115 | E13 | I | <p>Clock Edge Select</p> <p>In clock/data recovery mode, setting CLKE “high” will cause RPOS/RNEG to be valid on the falling edge of RCLK and SDO to be valid on the rising edge of SCLK. When CLKE is set “low”, RPOS/RNEG is valid on the rising edge of RCLK, and SDO is valid on the falling edge of SCLK. When the part is operated in data recovery mode, the RPOS/RNEG output polarity is active “high” when CLKE is set “high” and active “low” when CLKE is set “low”.</p> |

3.3 Address Inputs/Loopbacks

| SYMBOL | LQFP | LFBGA | TYPE | DESCRIPTION |
|----------|------|-------|------|--|
| A4 | 12 | F4 | I | <p>Address Selector Input</p> <p>Parallel Host Mode - During non-multiplexed parallel host mode operation, this pin function as the address 4 input for the parallel interface.</p> <p>Hardware Mode - The A4 pin must be tied low at all times.</p> |
| A3 | 13 | F3 | I | <p>Non-Intrusive Monitoring/Address Selector Inputs</p> <p>Parallel Host Mode - During non-multiplexed parallel host mode operation, these pins function as address A[3:0] inputs for the parallel interface.</p> <p>Hardware Mode - The A[3:0] pins are used for port selection during non-intrusive monitoring. In non-intrusive monitoring mode, receiver 0's input is internally connected to the transmit or receive ports on one of the other 7 channels. The recovered clock and data from the selected port are output on RPOS0/RNEG0 and RCLK0. Additionally, the data from the selected port can be output on TTIP0/TRING0 by activating the remote loopback function for channel 0 (Refer to Performance Monitor Register (0Bh) (See Section 14.12 on page 36).</p> |
| A2 | 14 | F2 | I | |
| A1 | 15 | F1 | I | |
| A0 | 16 | G3 | I | |
| LOOP0/D0 | 21 | G2 | I/O | <p>Loopback Mode Selector/Parallel Data Input/Output</p> <p>Parallel Host Mode - In non-multiplexed microprocessor interface mode, these pins function as the bi-directional 8-bit data port. When operating in multiplexed microprocessor interface mode, these pins function as the address and data inputs/outputs.</p> <p>Hardware Mode</p> <ul style="list-style-type: none"> - No Loopback - The CS61884 is in a normal operating state when LOOP is left open (unconnected) or tied to VCCIO/2. - Local Loopback - When LOOP is tied High, data transmitted on TTIP and TRING is looped back into the analog input of the corresponding channel's receiver and output on RPOS and RNEG. Input Data present on RTIP and RRING is ignored. - Remote Loopback - When LOOP is tied Low the recovered clock and data received on RTIP and RRING is looped back for transmission on TTIP and TRING. Data on TPOS and TNEG is ignored. |
| LOOP1/D1 | 22 | H3 | I/O | |
| LOOP2/D2 | 23 | H2 | I/O | |
| LOOP3/D3 | 24 | J4 | I/O | |
| LOOP4/D4 | 25 | J3 | I/O | |
| LOOP5/D5 | 26 | J2 | I/O | |
| LOOP6/D6 | 27 | J1 | I/O | |
| LOOP7/D7 | 28 | K1 | I/O | |

3.4 Cable Select

| SYMBOL | LQFP | LFBGA | TYPE | DESCRIPTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|------------|----------------|--------------|--|----------|--------|--------------|-----------|-------|------------|----------------|----------|-------|------|----------------|----------|-------|-----|----------------|----------|----|------------|----------------|--------------|----|------|---------------|----------|----|-----|---------------|----------|
| CBLSEL | 93 | G13 | I | <p>Cable Impedance Select</p> <p>Host Mode - The input voltage to this pin does not effect normal operation.</p> <p>Hardware Mode - This pin is used in combination with the LEN control pins (Refer to Table 5, “Hardware Mode Line Length Configuration Selection,” on page 25) to set the line impedance for all eight receivers and transmitters. This pin also selects whether or not all eight receivers use an internal or external line matching network (Refer to the Table below for proper settings).</p> <p style="text-align: center;">Table 3. Cable Impedance Selection</p> <table border="1"> <thead> <tr> <th>E1/T1/J1</th> <th>CBLSEL</th> <th>Transmitters</th> <th>Receivers</th> </tr> </thead> <tbody> <tr> <td>T1/J1</td> <td>No Connect</td> <td>100 Ω Internal</td> <td>Internal</td> </tr> <tr> <td>T1/J1</td> <td>HIGH</td> <td>100 Ω Internal</td> <td>Internal</td> </tr> <tr> <td>T1/J1</td> <td>LOW</td> <td>100 Ω Internal</td> <td>External</td> </tr> <tr> <td>E1</td> <td>No Connect</td> <td>120 Ω Internal</td> <td>Inter or Ext</td> </tr> <tr> <td>E1</td> <td>HIGH</td> <td>75 Ω Internal</td> <td>Internal</td> </tr> <tr> <td>E1</td> <td>LOW</td> <td>75 Ω Internal</td> <td>External</td> </tr> </tbody> </table> <p>NOTE: Refer to Figure 17 on page 51 and Figure 18 on page 52 for appropriate external line matching components. All transmitters use internal matching networks.</p> | E1/T1/J1 | CBLSEL | Transmitters | Receivers | T1/J1 | No Connect | 100 Ω Internal | Internal | T1/J1 | HIGH | 100 Ω Internal | Internal | T1/J1 | LOW | 100 Ω Internal | External | E1 | No Connect | 120 Ω Internal | Inter or Ext | E1 | HIGH | 75 Ω Internal | Internal | E1 | LOW | 75 Ω Internal | External |
| E1/T1/J1 | CBLSEL | Transmitters | Receivers | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| T1/J1 | No Connect | 100 Ω Internal | Internal | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| T1/J1 | HIGH | 100 Ω Internal | Internal | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| T1/J1 | LOW | 100 Ω Internal | External | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E1 | No Connect | 120 Ω Internal | Inter or Ext | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E1 | HIGH | 75 Ω Internal | Internal | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E1 | LOW | 75 Ω Internal | External | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

3.5 Status

| SYMBOL | LQFP | LFBGA | TYPE | DESCRIPTION |
|--------|------|-------|------|---|
| LOS0 | 42 | K4 | O | <p>Loss of Signal Output</p> <p>The LOS output pins can be configured to indicate a loss of signal (LOS) state that is compliant to either T1.231, ITU G.775 or ETSI 300 233. These pins are asserted “High” to indicate LOS. The LOS output returns low when an input signal is present for the time period dictated by the associated specification (Refer to Loss-of-Signal (LOS) (See Section 10.5 on page 27)).</p> |
| LOS1 | 35 | K3 | O | |
| LOS2 | 75 | K12 | O | |
| LOS3 | 68 | K11 | O | |
| LOS4 | 113 | E11 | O | |
| LOS5 | 106 | E12 | O | |
| LOS6 | 3 | E3 | O | |
| LOS7 | 140 | E4 | O | |

3.6 Digital Rx/Tx Data I/O

| SYMBOL | LQFP | LFBGA | TYPE | DESCRIPTION | | | | | | | | | | | | | | | |
|---------------------------|----------|---------------|--------|--|------|------|--------|---|---|-------|---|---|---------------|---|---|---------------|---|---|-------|
| TCLK0 | 36 | N1 | I | <p>Transmit Clock Input Port 0</p> <ul style="list-style-type: none"> - When TCLK is active, the TPOS and TNEG pins function as NRZ inputs that are sampled on the falling edge of TCLK. - If MCLK is active, TAOS will be generated when TCLK is held High for 16 MCLK cycles. <p>NOTE: MCLK is used as the timing reference during TAOS and must have the appropriate stability.</p> <ul style="list-style-type: none"> - If TCLK is held High in the absence of MCLK, the TPOS and TNEG inputs function as RZ inputs. In this mode, the transmit pulse width is set by the pulse-width of the signal input on TPOS and TNEG. To enter this mode, TCLK must be held high for at least 12 μS. - If TCLK is held Low, the output drivers enter a low-power, high impedance state. | | | | | | | | | | | | | | | |
| TPOS0/TDATA0 TNEG0/UBS | 37 38 | N2 N3 | I I | <p>Transmit Positive Pulse/Transmit Data Input Port 0 Transmit Negative Pulse/Unipolar-Bipolar Select Port 0</p> <p>The function of the TPOS/TDATA and TNEG/UBS inputs are determined by whether Unipolar, Bipolar or RZ input mode has been selected.</p> <p>Bipolar Mode - In this mode, NRZ data on TPOS and TNEG are sampled on the falling edge of TCLK and transmitted onto the line at TTIP and TRING respectively. A "High" input on TPOS results in transmission of a positive pulse; a "High" input on TNEG results in a transmission of a negative pulse. The translation of TPOS/TNEG inputs to TTIP/TRING outputs is as follows:</p> <table border="1" data-bbox="776 1266 1430 1444"> <thead> <tr> <th>TPOS</th> <th>TNEG</th> <th>OUTPUT</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Space</td> </tr> <tr> <td>1</td> <td>0</td> <td>Positive Mark</td> </tr> <tr> <td>0</td> <td>1</td> <td>Negative Mark</td> </tr> <tr> <td>1</td> <td>1</td> <td>Space</td> </tr> </tbody> </table> <p>Unipolar mode - Unipolar mode is activated by holding TNEG/UBS "High" for more than 16 TCLK cycles, when MCLK is present. The falling edge of TCLK samples a unipolar data stream on TPOS/TDATA.</p> <p>RZ Mode - To activate RZ mode tie TCLK "High" with the absence of MCLK. In this mode, the duty cycle of the TPOS and TNEG inputs determine the pulse width of the output signal on TTIP and TRING.</p> | TPOS | TNEG | OUTPUT | 0 | 0 | Space | 1 | 0 | Positive Mark | 0 | 1 | Negative Mark | 1 | 1 | Space |
| TPOS | TNEG | OUTPUT | | | | | | | | | | | | | | | | | |
| 0 | 0 | Space | | | | | | | | | | | | | | | | | |
| 1 | 0 | Positive Mark | | | | | | | | | | | | | | | | | |
| 0 | 1 | Negative Mark | | | | | | | | | | | | | | | | | |
| 1 | 1 | Space | | | | | | | | | | | | | | | | | |

| SYMBOL | LQFP | LFBGA | TYPE | DESCRIPTION |
|--------------|------|-------|------|--|
| RCLK0 | 39 | P1 | O | <p>Receive Clock Output Port 0</p> <ul style="list-style-type: none"> - When MCLK is active, this pin outputs the recovered clock from the signal input on RTIP and RRING. In the event of LOS, the RCLK output transitions from the recovered clock to MCLK. - If MCLK is held “High”, the clock recovery circuitry is disabled and the RCLK output is driven by the XOR of RNEG and RPOS. - If MCLK is held “Low”, this output is in a high-impedance state. |
| RPOS0/RDATA0 | 40 | P2 | O | <p>Receive Positive Pulse/ Receive Data Output Port 0 Receive Negative Pulse/Bipolar Violation Output Port 0</p> <p>The function of the RPOS/RDATA and RNEG/BPV outputs are determined by whether Unipolar, Bipolar, or RZ input mode has been selected. During LOS, the RPOS/RNEG outputs will remain active.</p> <p>NOTE: The RPOS/RNEG outputs can be High-Z by holding MCLK Low.</p> <p>Bipolar Output Mode - When configured for Bipolar operation, NRZ Data is recovered from RTIP/RRING and output on RPOS/RNEG. A high signal on RPOS or RNEG correspond to the receipt of a positive or negative pulse on RTIP/RRING respectively. The RPOS/RNEG outputs are valid on the falling or rising edge of RCLK as configured by CLKE.</p> <p>Unipolar Output Mode - When unipolar mode is activated, the recovered data is output on RDATA. The decoder signals bipolar Violations on the RNEG/BPV pin.</p> <p>RZ Output Mode - In this mode, the RPOS/RNEG pins output RZ data recovered by slicing the signal present on RTIP/RRING. A positive pulse on RTIP with respect to RRING generates a logic 1 on RPOS; a positive pulse on RRING with respect to RTIP generates a logic 1 on RNEG. The polarity of the output on RPOS/RNEG is selectable using the CLKE pin. In this mode, external circuitry is used to recover clock from the received signal.</p> |
| RNEG0/BPV0 | 41 | P3 | O | |
| TCLK1 | 29 | L1 | I | Transmit Clock Input Port 1 |
| TPOS1/TDATA1 | 30 | L2 | I | Transmit Positive Pulse/Transmit Data Input Port 1 |
| TNEG1/UBS1 | 31 | L3 | I | Transmit Negative Pulse/Unipolar-Bipolar Select Port 1 |
| RCLK1 | 32 | M1 | O | Receive Clock Output Port 1 |
| RPOS1/RDATA1 | 33 | M2 | O | Receive Positive Pulse/ Receive Data Output Port 1 |
| RNEG1/BPV1 | 34 | M3 | O | Receive Negative Pulse/Bipolar Violation Output Port 1 |
| TCLK2 | 81 | L14 | I | Transmit Clock Input Port 2 |
| TPOS2/TDATA2 | 80 | L13 | I | Transmit Positive Pulse/Transmit Data Input Port 2 |
| TNEG2/UBS2 | 79 | L12 | I | Transmit Negative Pulse/Unipolar-Bipolar Select Port 2 |

| SYMBOL | LQFP | LFBGA | TYPE | DESCRIPTION |
|---------------|-------------|--------------|-------------|--|
| RCLK2 | 78 | M14 | O | Receive Clock Output Port 2 |
| RPOS2/RDATA2 | 77 | M13 | O | Receive Positive Pulse/ Receive Data Output Port 2 |
| RNEG2/BPV2 | 76 | M12 | O | Receive Negative Pulse/Bipolar Violation Output Port 2 |
| TCLK3 | 74 | N14 | I | Transmit Clock Input Port 3 |
| TPOS3/TDATA3 | 73 | N13 | I | Transmit Positive Pulse/Transmit Data Input Port 3 |
| TNEG3/UBS3 | 72 | N12 | I | Transmit Negative Pulse/Unipolar-Bipolar Select Port 3 |
| RCLK3 | 71 | P14 | O | Receive Clock Output Port 3 |
| RPOS3/RDATA3 | 70 | P13 | O | Receive Positive Pulse/ Receive Data Output Port 3 |
| RNEG3/BPV3 | 69 | P12 | O | Receive Negative Pulse/Bipolar Violation Output Port 3 |
| TCLK4 | 107 | B14 | I | Transmit Clock Input Port 4 |
| TPOS4/TDATA4 | 108 | B13 | I | Transmit Positive Pulse/Transmit Data Input Port 4 |
| TNEG4/UBS4 | 109 | B12 | I | Transmit Negative Pulse/Unipolar-Bipolar Select Port 4 |
| RCLK4 | 110 | A14 | O | Receive Clock Output Port 4 |
| RPOS4/RDATA4 | 111 | A13 | O | Receive Positive Pulse/ Receive Data Output Port 4 |
| RNEG4/BPV4 | 112 | A12 | O | Receive Negative Pulse/Bipolar Violation Output Port 4 |
| TCLK5 | 100 | D14 | I | Transmit Clock Input Port 5 |
| TPOS5/TDATA5 | 101 | D13 | I | Transmit Positive Pulse/Transmit Data Input Port 5 |
| TNEG5/UBS5 | 102 | D12 | I | Transmit Negative Pulse/Unipolar-Bipolar Select Port 5 |
| RCLK5 | 103 | C14 | O | Receive Clock Output Port 5 |
| RPOS5/RDATA5 | 104 | C13 | O | Receive Positive Pulse/ Receive Data Output Port 5 |
| RNEG5/BPV5 | 105 | C12 | O | Receive Negative Pulse/Bipolar Violation Output Port 5 |
| TCLK6 | 9 | D1 | I | Transmit Clock Input Port 6 |
| TPOS6/TDATA6 | 8 | D2 | I | Transmit Positive Pulse/Transmit Data Input Port 6 |
| TNEG6/UBS6 | 7 | D3 | I | Transmit Negative Pulse/Unipolar-Bipolar Select Port 6 |
| RCLK6 | 6 | C1 | O | Receive Clock Output Port 6 |
| RPOS6/RDATA6 | 5 | C2 | O | Receive Positive Pulse/ Receive Data Output Port 6 |
| RNEG6/BPV6 | 4 | C3 | O | Receive Negative Pulse/Bipolar Violation Output Port 6 |
| TCLK7 | 2 | B1 | I | Transmit Clock Input Port 7 |
| TPOS7/TDATA7 | 1 | B2 | I | Transmit Positive Pulse/Transmit Data Input Port 7 |
| TNEG7/UBS7 | 144 | B3 | I | Transmit Negative Pulse/Unipolar-Bipolar Select Port 7 |

| SYMBOL | LQFP | LFBGA | TYPE | DESCRIPTION |
|--------------|------|-------|------|--|
| RCLK7 | 143 | A1 | O | Receive Clock Output Port 7 |
| RPOS7/RDATA7 | 142 | A2 | O | Receive Positive Pulse/ Receive Data Output Port 7 |
| RNEG7/BPV7 | 141 | A3 | O | Receive Negative Pulse/Bipolar Violation Output Port 7 |

3.7 Analog RX/TX Data I/O

| SYMBOL | LQFP | LFBGA | TYPE | DESCRIPTION |
|--------|------|-------|------|---|
| TTIP0 | 45 | N5 | O | Transmit Tip Output Port 0 Transmit Ring Output Port 0 TTIP and TRING pins are the differential outputs of the transmit driver. The driver internally matches impedances for E1 75 Ω, E1 120 Ω and T1/J1 100 Ω lines requiring only a 1:2 transformer. The CBLSEL pin is used to select the appropriate line matching impedance only in “Hardware” mode. In host mode, the appropriate line matching impedance is selected by the Line Length Data Register (11h) (See Section 14.18 on page 39). NOTE: TTIP and TRING are forced to a high impedance state when the TCLK pin is “Low” for over 12μS or the TXOE pin is forced “Low”. |
| TRING0 | 46 | P5 | O | |
| RTIP0 | 48 | P7 | I | Receive Tip Input Port 0 Receive Ring Input Port 0 RTIP and RRING are the differential line inputs to the receiver. The receiver uses either Internal Line Impedance or External Line Impedance modes to match the line impedances for E1 75Ω, E1 120Ω or T1/J1 100Ω modes. Internal Line Impedance Mode - The receiver uses the same external resistors to match the line impedance (Refer to Figure 17 on page 51). External Line Impedance Mode - The receiver uses different external resistors to match the line impedance (Refer to Figure 18 on page 52). - In host mode, the appropriate line impedance is selected by the Line Length Data Register (11h) (See Section 14.18 on page 39). - In hardware mode, the CBLSEL pin in combination with the LEN pins select the appropriate line impedance. (Refer to Table 3 on page 15 for proper line impedance settings). NOTE: Data and clock recovered from the signal input on these pins are output via RCLK, RPOS, and RNEG. |
| RRING0 | 49 | N7 | I | |
| TTIP1 | 52 | L5 | O | Transmit Tip Output Port 1 |
| TRING1 | 51 | M5 | O | Transmit Ring Output Port 1 |
| RTIP1 | 55 | M7 | I | Receive Tip Input Port 1 |
| RRING1 | 54 | L7 | I | Receive Ring Input Port 1 |

| SYMBOL | LQFP | LFBGA | TYPE | DESCRIPTION |
|---------------|-------------|--------------|-------------|-----------------------------|
| TTIP2 | 57 | L10 | O | Transmit Tip Output Port 2 |
| TRING2 | 58 | M10 | O | Transmit Ring Output Port 2 |
| RTIP2 | 60 | M8 | I | Receive Tip Input Port 2 |
| RRING2 | 61 | L8 | I | Receive Ring Input Port 2 |
| TTIP3 | 64 | N10 | O | Transmit Tip Output Port 3 |
| TRING3 | 63 | P10 | O | Transmit Ring Output Port 3 |
| RTIP3 | 67 | P8 | I | Receive Tip Input Port 3 |
| RRING3 | 66 | N8 | I | Receive Ring Input Port 3 |
| TTIP4 | 117 | B10 | O | Transmit Tip Output Port 4 |
| TRING4 | 118 | A10 | O | Transmit Ring Output Port 4 |
| RTIP4 | 120 | A8 | I | Receive Tip Input Port 4 |
| RRING4 | 121 | B8 | I | Receive Ring Input Port 4 |
| TTIP5 | 124 | D10 | O | Transmit Tip Output Port 5 |
| TRING5 | 123 | C10 | O | Transmit Ring Output Port 5 |
| RTIP5 | 127 | C8 | I | Receive Tip Input Port 5 |
| RRING5 | 126 | D8 | I | Receive Ring Input Port 5 |
| TTIP6 | 129 | D5 | O | Transmit Tip Output Port 6 |
| TRING6 | 130 | C5 | O | Transmit Ring Output Port 6 |
| RTIP6 | 132 | C7 | I | Receive Tip Input Port 6 |
| RRING6 | 133 | D7 | I | Receive Ring Input Port 6 |
| TTIP7 | 136 | B5 | O | Transmit Tip Output Port 7 |
| TRING7 | 135 | A5 | O | Transmit Ring Output Port 7 |
| RTIP7 | 139 | A7 | I | Receive Tip Input Port 7 |
| RRING7 | 138 | B7 | I | Receive Ring Input Port 7 |

3.8 JTAG Test Interface

| SYMBOL | LQFP | LFBGA | TYPE | DESCRIPTION |
|--------------------------|------|-------|------|--|
| $\overline{\text{TRST}}$ | 95 | G12 | I | JTAG Reset This active Low input resets the JTAG controller. This input is pulled up internally and may be left as a NC when not used. |
| TMS | 96 | F11 | I | JTAG Test Mode Select Input This input enables the JTAG serial port when active High. This input is sampled on the rising edge of TCK. This input is pulled up internally and may be left as a NC when not used. |
| TCK | 97 | F14 | I | JTAG Test Clock Data on TDI is valid on the rising edge of TCK. Data on TDO is valid on the falling edge of TCK. When TCK is stopped high or low, the contents of all JTAG registers remain unchanged. Tie pin low through a 10 K Ω resistor when not used. |
| TDO | 98 | F13 | O | JTAG Test Data Output JTAG test data is shifted out of the device on this pin. Data is output on the falling edge of TCK. Leave as NC when not used. |
| TDI | 99 | F12 | I | JTAG Test Data Input JTAG test data is shifted into the device using this pin. The pin is sampled on the rising edge of TCK. TDI is pulled up internally and may be left as a NC when not used. |

3.9 Miscellaneous

| SYMBOL | LQFP | LFBGA | TYPE | DESCRIPTION |
|--------|------|-------|------|--|
| REF | 94 | H13 | I | Reference Input This pin must be tied to ground through 13.3 K Ω 1% resistor. This pin is used to set the internal current level. |

4. OPERATION

The CS61884 is a full featured line interface unit for up to eight E1/T1/J1 lines. The device provides an interface to twisted pair or co-axial media. A matched impedance technique is employed that reduces power and eliminates the need for matching resistors. As a result, the device can interface directly to the line through a transformer without the need for matching resistors on the transmit side. The receive side uses the same resistor values for all E1/T1/J1 settings.

5. POWER-UP

On power-up, the device is held in a static state until the power supply achieves approximately 70% of the power supply voltage. Once the power supply threshold is passed, the analog circuitry is calibrated, the control registers are reset to their default settings, and the various internal state machines are reset. The reset/calibration process completes in about 30 ms.

6. MASTER CLOCK

The CS61884 requires a 2.048 MHz or 1.544 MHz reference clock with a minimum accuracy of ± 100 ppm. This clock may be supplied from internal system timing or a CMOS crystal oscillator and input to the MCLK pin.

The receiver uses MCLK as a reference for clock recovery, jitter attenuation, and the generation of RCLK during LOS. The transmitter uses MCLK as the transmit timing reference during a blue alarm transmit all ones condition. In addition, MCLK provides the reference timing for wait state generation.

In systems with a jittered transmit clock, MCLK should not be tied to the transmit clock, a separate crystal oscillator should drive the reference clock input. Any jitter present on the reference clock will not be filtered by the jitter attenuator and can cause the CS61884 to operate incorrectly.

7. G.772 MONITORING

The receive path of channel zero of the CS61884 can be used to monitor the receive or transmit paths of any of the other channels. The signal to be monitored is multiplexed to channel zero through the G.772 Multiplexer. The multiplexer and channel zero then form a G.772 compliant digital Protected Monitoring Point (PMP). When the PMP is connected to the channel, the attenuation in the signal path is negligible across the signal band. The signal can be observed using RPOS, RNEG, and RCLK of channel zero or by putting channel zero in remote loop-back, the signal can be observed on TTIP and TRING of channel zero.

The G.772 monitoring function is available during both host mode and hardware mode operation. In host modes, individual channels are selected for monitoring via the **Performance Monitor Register (0Bh)** (See Section 14.12 on page 36). In hardware mode, individual channels are selected through the A3:A0 pins (Refer to [Table 4](#) below for address settings).

Table 4. G.772 Address Selection

| Address [A3:A0] | Channel Selection |
|-----------------|-------------------------|
| 0000 | Monitoring Disabled |
| 0001 | Receiver Channel # 1 |
| 0010 | Receiver Channel # 2 |
| 0011 | Receiver Channel # 3 |
| 0100 | Receiver Channel # 4 |
| 0101 | Receiver Channel # 5 |
| 0110 | Receiver Channel # 6 |
| 0111 | Receiver Channel # 7 |
| 1000 | Monitoring Disabled |
| 1001 | Transmitter Channel # 1 |
| 1010 | Transmitter Channel # 2 |
| 1011 | Transmitter Channel # 3 |
| 1100 | Transmitter Channel # 4 |
| 1101 | Transmitter Channel # 5 |
| 1110 | Transmitter Channel # 6 |
| 1111 | Transmitter Channel # 7 |

NOTE: In hardware mode the A4 pin must be tied low at all times.

8. BUILDING INTEGRATED TIMING SYSTEMS (BITS) CLOCK MODE

This mode is used to enable one or more channels as a stand-alone timing recovery unit used for G.703 Clock Recovery.

In hardware mode, BITS Clock mode is selected by pulling the MUX pin “HIGH”. This enables only channel zero as a stand-alone timing recovery unit, no other channel can be used as a timing recovery unit.

In host mode, each channel can be setup as an independent G.703 timing recovery unit, through the **Bits Clock Enable Register (1Eh)** (See Section 14.31 on page 41), setting the desired bit to “1” enables BITS Clock mode for that channel. The following diagrams show how the BITS clock function operates.

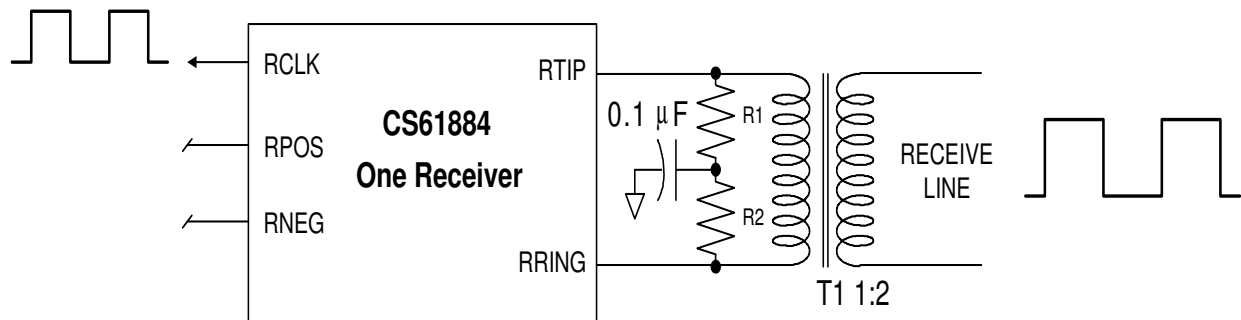


Figure 3. G.703 BITS Clock Mode in NRZ Mode

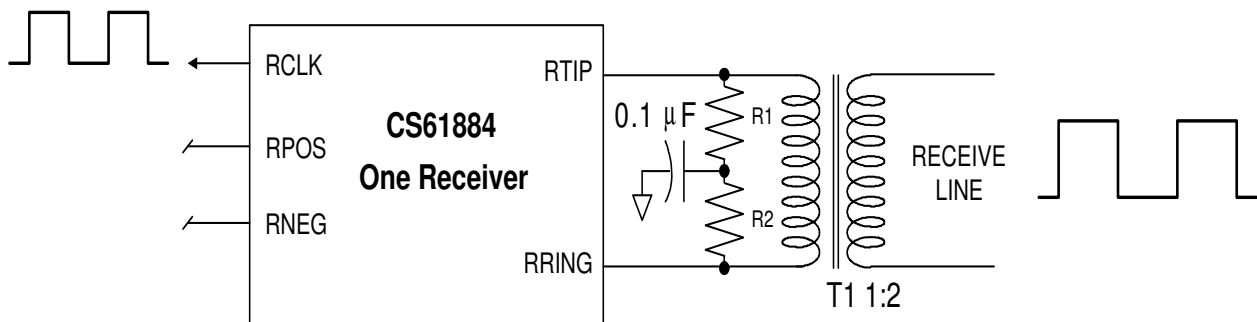


Figure 4. G.703 BITS Clock Mode in RZ Mode

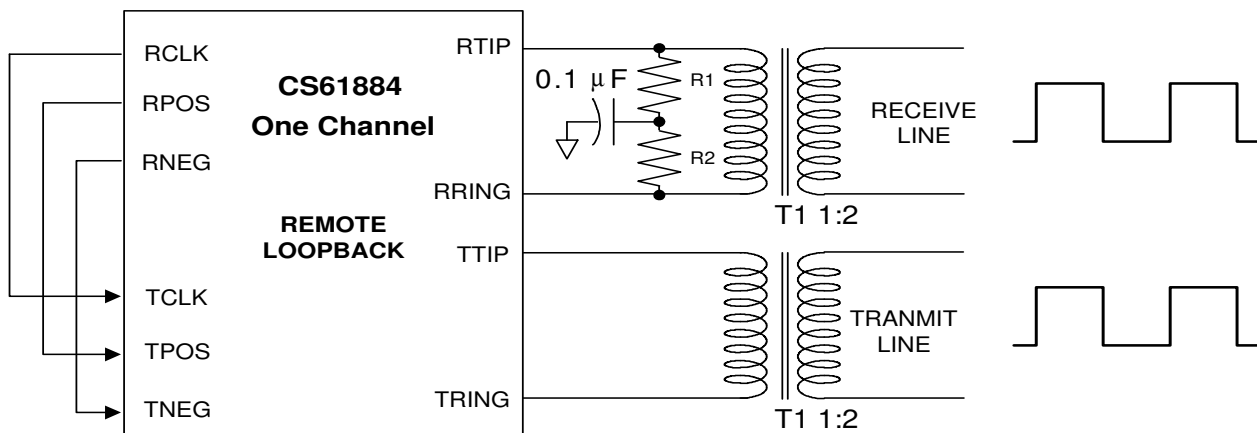


Figure 5. G.703 BITS Clock Mode in Remote Loopback

9. TRANSMITTER

The CS61884 contains eight identical transmitters that each use a low power matched impedance driver to eliminate the need for external load matching resistors, while providing superior return loss. As a result, the TTIP/TRING outputs can be connected directly to the transformer allowing one hardware circuit for 100 Ω (T1/J1), 120 Ω (E1), and 75 Ω (E1) applications.

Digital transmit data is input into the CS61884 through the TPOS/TNEG input pins. These pins accept data in one of three formats: unipolar, bipolar, or RZ. In either unipolar or bipolar mode, the CS61884 internally generates a pulse shape compliant to the ANSI T1.102 mask for T1/J1 or the G.703 mask for E1 (Refer to [Figure 6](#) and [Figure 7](#)). The pulse shaping applied to the transmit data can be selected in hardware mode or in host mode.

In hardware mode, the pulse shape is selected for all channels via the LEN[2:0] pins (Refer to [Table 5 on page 25](#)). This sets the pulse shape for all eight transmitters to one of the prestored line lengths. The CBLSEL pin in combination with the LEN[2:0] pins set the line impedance for all eight channels. The CBLSEL pin also selects between E1 120 Ω or E1 75 Ω modes, when the LEN pins are configured for E1 operation mode.

In host mode, the pulse shape for each channel can be set independently, during NRZ operation mode, for proper clock recovery and jitter attenuation. In RZ Mode each channel can be set to either T1/J1 or E1, when there is no Mclk present (Refer to [RZ Mode](#) (See Section 9.3 on page 25).

To select the standard pulse shapes, the channels are selected individually using the [Line Length Channel ID Register \(10h\)](#) (See Section 14.17 on page 38), then the LEN[3:0] bits in the [Line Length Data Register \(11h\)](#) (See Section 14.18 on page 39) are set for the desired line length for that channel. The LEN bits select the line type and im-

pedance for both the receiver and the transmitter of the addressed channel.

NOTE: In host mode the CBLSEL pin is not used.

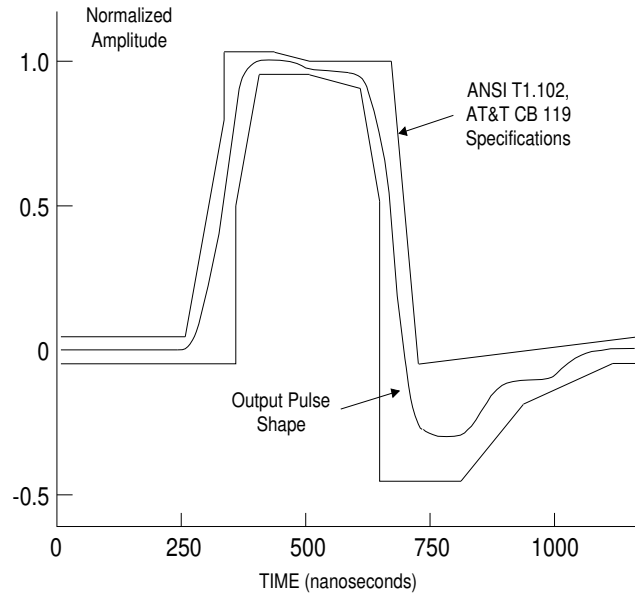


Figure 6. Pulse Mask at T1/J1 Interface

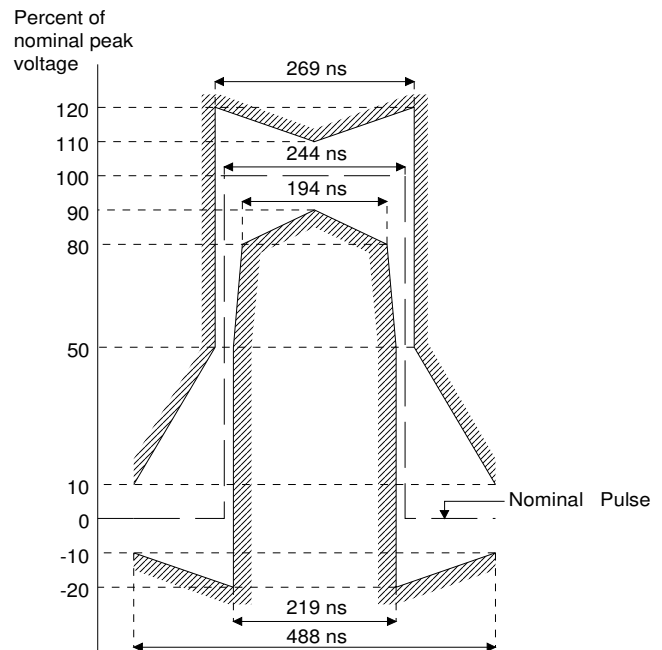


Figure 7. Pulse Mask at E1 Interface

The CS61884 also allows the user to customize the transmit pulse shapes to compensate for non-standard cables, transformers, or protection circuitry. For further information on the AWG Refer to **Arbitrary Waveform Generator** (See Section 15 on page 43).

For more information on the host mode registers, refer to **Register Descriptions** (See Section 14 on page 35).

9.1 Bipolar Mode

Bipolar mode provides transparent operation for applications in which the line coding function is performed by an external framing device. In this mode, the falling edge of TCLK samples NRZ data on TPOS/TNEG for transmission on TTIP/TRING.

9.2 Unipolar Mode

In unipolar mode, the CS61884 is configured such that transmit data is encoded using B8ZS, HDB3, or AMI line codes. This mode is activated by holding TNEG/UBS “High” for more than 16 TCLK cycles. Transmit data is input to the part via the TPOS/TDATA pin on the falling edge of TCLK. When operating the part in hardware mode, the CODEN pin is used to select between B8ZS/HDB3 or AMI encoding. During host mode operation, the line coding is selected via the **Global Control Register (0Fh)** (See Section 14.16 on page 38).

NOTE: The encoders/decoders are selected for all eight channels in both hardware and host mode.

9.3 RZ Mode

In RZ mode, the internal pulse shape circuitry is bypassed and RZ data driven into TPOS/TNEG is transmitted on TTIP/TRING. In this mode, the pulse width of the transmitter output is determined by the width of the RZ signal input to TPOS/TNEG. This mode is entered when MCLK does not exist and TCLK is held “High” for at least 12 μ sec.

9.4 Transmitter Powerdown / High-Z

The transmitters can be forced into a high impedance, low power state by holding TCLK of the appropriate channel low for at least 12 μ s or 140 MCLK cycles. In hardware and host mode, the TXOE pin forces all eight transmitters into a high impedance state within 1 μ s.

In host mode, each transmitter is individually controllable using the **Output Disable Register (12h)** (See Section 14.19 on page 39). The TXOE pin can be used in host mode, but does not effect the contents of the Output Enable Register. This feature is useful in applications that require redundancy.

9.5 Transmit All Ones (TAOS)

When TAOS is activated, continuous ones are transmitted on TTIP/TRING using MCLK as the transmit timing reference. In this mode, the TPOS and TNEG inputs are ignored.

In hardware mode, TAOS is activated by pulling TCLK “High” for more than 16 MCLK cycles.

Table 5. Hardware Mode Line Length Configuration Selection

| LEN[2:0] | Transmit Pulse Configuration | Line Z | Operation |
|----------|------------------------------|----------------------------|-----------|
| 000 | E1 3.0V / E1 2.37V | 120 Ω / 75 Ω | E1 |
| 001 | DS1, Option A (undershoot) | 100 Ω | T1/J1 |
| 010 | DS1, Option A (0 dB) | 100 Ω | T1/J1 |
| 011 | DSX-1: 0-133 ft. (0.6dB) | 100 Ω | T1/J1 |
| 100 | DSX-1: 133-266 ft. (1.2dB) | 100 Ω | T1/J1 |
| 101 | DSX-1: 266-399 ft. (1.8dB) | 100 Ω | T1/J1 |
| 110 | DSX-1: 399-533 ft. (2.4dB) | 100 Ω | T1/J1 |
| 111 | DSX-1: 533-655 ft. (3.0dB) | 100 Ω | T1/J1 |

In host mode, TAOS is generated for a particular channel by asserting the associated bit in the **TAOS Enable Register (03h)** (See Section 14.4 on page 35).

Since MCLK is the reference clock, it should be of adequate stability.

9.6 Automatic TAOS

While a given channel is in the LOS condition, if the corresponding bit in the **Automatic TAOS Register (0Eh)** (See Section 14.15 on page 37) is set, the device will drive that channel's TTIP and TRING with the all ones pattern. This function is only available in host mode. Refer to **Loss-of-Signal (LOS)** (See Section 10.5 on page 27).

9.7 Driver Failure Monitor

In host mode, the Driver Failure Monitor (DFM) function monitors the output of each channel and sets a bit in the **DFM Status Register (05h)** (See Section 14.6 on page 35) if a secondary short circuit is detected between TTIP and TRING. This generates an interrupt if the respective bit in the **DFM Interrupt Enable Register (07h)** (See Section 14.8 on page 36) is also set. Any change in the **DFM Status Register (05h)** (See Section 14.6 on page 35) will result in the corresponding bit in the **DFM Interrupt Status Register (09h)** (See Section 14.10 on page 36) being set. The interrupt is cleared by reading the **DFM Interrupt Status Register (09h)** (See Section 14.10 on page 36). This feature works in all modes of operation E1 75 Ω , E1 120 Ω and T1/J1 100 Ω .

9.8 Driver Short Circuit Protection

The CS61884 provides driver short circuit protection when current on the secondary exceeds 50 mA RMS during E1/T1/J1 operation modes.

10. RECEIVER

The CS61884 contains eight identical receivers that utilize an internal matched impedance technique that provides for the use of a common set of exter-

nal components for 100 Ω (T1/J1), 120 Ω (E1), and 75 Ω (E1) operation (Refer to [Figure 17 on page 51](#)). This feature enables the use of a one stuffing option for all E1/T1/J1 line impedances. The appropriate E1/T1/J1 line matching is selected via the LEN[2:0] and the CBLSEL pins in hardware mode, or via the **Line Length Channel ID Register (10h)** (See Section 14.17 on page 38) and bits[3:0] of the **Line Length Data Register (11h)** (See Section 14.18 on page 39) in host mode. The receivers can also be configured to use different external resistors to match the line impedance for E1 75 Ω , E1 120 Ω or T1/J1 100 Ω modes (Refer to [Figure 18 on page 52](#)).

The CS61884 receiver provides all of the circuitry to recover both data and clock from the data signal input on RTIP and RRING. The matched impedance receiver is capable of recovering signals with 12 dB of attenuation (referenced to 2.37 V or 3.0V nominal) while providing superior return loss. In addition, the timing recovery circuit along with the jitter attenuator provide jitter tolerance that far exceeds jitter specifications (Refer to [Figure 20 on page 58](#)).

The recovered data and clock is output from the CS61884 on RPOS/RNEG and RCLK. These pins output the data in one of three formats: bipolar, unipolar, or RZ. The CLKE pin is used to configure RPOS/RNEG, so that data is valid on either the rising or falling edge of RCLK.

10.1 Bipolar Output Mode

Bipolar mode provides a transparent clock/data recovery for applications in which the line decoding is performed by an external framing device. The recovered clock and data are output on RCLK, RNEG/BPV, and RPOS/RDATA.

10.2 Unipolar Output Mode

In unipolar mode, the CS61884 decodes the recovered data with either B8ZS, HDB3 or AMI line decoding. The decoded data is output on the

RPOS/RDATA pin. When bipolar violations are detected by the decoder, the RNEG/BPV pin is asserted “High”. This pin is driven “high” one RCLK period for every bipolar violation that is not part of the zero substitution rules. Unipolar mode is entered by holding the TNEG pin “High” for more than 16 MCLK cycles.

In hardware mode, the B8ZS/HDB3/AMI encoding/Decoding is activated via the CODEN pin. In host mode, the **Global Control Register (0Fh)** (See Section 14.16 on page 38) is used to select the encoding/decoding for all channels.

10.3 RZ Output Mode

In this mode the RTIP and RRING inputs are sliced to data values that are output on RPOS and RNEG. This mode is used in applications that have clock recovery circuitry external to the LIU. To support external clock recovery, the RPOS and RNEG outputs are XORed and output on an edge of RCLK. This mode is entered when MCLK is tied high.

NOTE: The valid RCLK edge of the RPOS/RNEG data is controlled by the CLKE pin.

10.4 Receiver Powerdown/High-Z

All eight receivers are powered down when MCLK is held low. In addition, this will force the RCLK, RPOS, and RNEG outputs into a high impedance state.

10.5 Loss-of-Signal (LOS)

The CS61884 makes use of both analog and digital LOS detection circuitry that is compliant to the latest specifications. During T1/J1 operation ANSI T1.231 is supported and in E1 operation mode, either ITU G.775 or ETSI 300 233 is supported. The LOS condition in E1 mode is changed from ITU G.775 to ETSI 300 233 in the **LOS/AIS Mode Enable Register (0Dh)** (See Section 14.14 on page 37).

The LOS detector increments a counter each time a zero is received, and resets the counter each time a

one “mark” is received. Depending on LOS detection mode, the LOS signal is set when a certain number of consecutive zeros are received. In Clock/Data recovery mode, this forces the recovered clock to be replaced by MCLK at the RCLK output. In addition the RPOS/RNEG outputs are forced “high” for the length of the LOS period except when local and analog loopback are enabled. Upon exiting LOS, the recovered clock replaces MCLK on the RCLK output. In Data recovery mode, RCLK is not replaced by MCLK when LOS is active. The LOS detection modes are summarized below.

NOTE: T1.231, G.775 and ETSI 300 233 are all available in host mode, but in hardware mode only ETSI 300 233 and T1.231 are available.

ANSI T1.231 (T1/J1 Mode Only) - LOS is detected if the receive signal is less than 200 mV for a period of 176 continuous pulse periods. The channel exits the LOS condition when the pulse density exceeds 12.5% over 176 pulse periods since the receipt of the last pulse. An incoming signal with a pulse amplitude exceeding 250 mV will cause a pulse transition on the RPOS/RDATA or RNEG outputs.

ITU G.775 (E1 Mode Only) - LOS is declared when the received signal level is less than 200 mV for 32 consecutive pulse periods (typical). The device exits LOS when the received signal achieves 12.5% ones density with no more than 15 consecutive zeros in a 32 bit sliding window and the signal level exceeds 250 mV.

ETSI 300 233 (E1 Host Mode Only) - The LOS indicator becomes active when the receive signal level drops below 200 mV for more than 2048 pulse periods (1 msec). The channel exits the LOS state when the input signal exceeds 250 mV and has transitions for more than 32 pulse periods (16 μ sec). This LOS detection method can only be selected while in host mode.

During host mode operation, LOS is reported in the LOS Status Monitor Register. Both the LOS pins and the register bits reflect LOS status in host mode operation. The LOS pins and status bits are set high (indicating loss of signal) during reset, power-up, or channel powered-down.

10.6 Alarm Indication Signal (AIS)

The CS61884 detects all ones alarm condition per the relevant ANSI, ITU, and ETSI specifications. In general, AIS is indicated when the one's density of the receive signal exceeds that dictated by the relevant specification. This feature is only available in host mode (Refer to **LOS/AIS Mode Enable Register (0Dh)** (See Section 14.14 on page 37)).

ANSI T1.231 AIS (T1/J1 Mode) - The AIS condition is declared when less than 9 zeros are received within a sliding window of 8192 bits. This corresponds to a ones density of 99.9% over a period of 5.3 ms. The AIS condition is cleared when nine or more zeros are detected in a sliding window of 8192 bits.

ITU G.775 AIS (E1 Mode) - The AIS condition is declared when less than 3 zeros are received within two consecutive 512 bit windows. The AIS condition is cleared when 3 or more zeros are received in two consecutive 512 bit windows.

ETSI 300 233 (E1 Mode) - The AIS condition is declared when less than 3 zeros are received in a 512 bit window. The AIS condition is cleared when a 512 bit window is received containing 3 or more zeros.

11. JITTER ATTENUATOR

The CS61884 internal jitter attenuators can be switched into either the receive or transmit paths. Alternatively, it can be removed from both paths to reduce the propagation delay.

During Hardware mode operation, the location of the jitter attenuator for all eight channels are con-

trolled by the JASEL pin (Refer to **Table 6** for pin configurations). The jitter attenuator's FIFO length and corner frequency, can not be changed in hardware mode. The FIFO length and corner frequency are set to 32 bits and 1.25Hz for the E1 operational modes and to 32 bits and 3.78Hz in the T1/J1 operational modes.

Table 6. Jitter Attenuator Configurations

| PIN STATE | JITTER ATTENUATOR POSITON |
|-----------|---------------------------|
| LOW | Transmit Path |
| HIGH | Receive Path |
| OPEN | Disabled |

During host mode operation, the location of the jitter attenuator for all eight channels are set by bits 0 and 1 in the **Global Control Register (0Fh)** (See Section 14.16 on page 38). The GLOBAL CONTROL REGISTER (0Fh) also configures the jitter attenuator's FIFO length (bit 3) and corner frequency (bit 2).

The attenuator consists of a 64-bit FIFO, a narrow-band monolithic PLL, and control logic. The jitter attenuator requires no external crystal. Signal jitter is absorbed in the FIFO which is designed to neither overflow nor underflow.

If overflow or underflow is imminent, the jitter transfer function is altered to ensure that no bit-errors occur. A configuration option is provided to reduce the jitter attenuator FIFO length from 64 bits to 32 bits in order to reduce propagation delay. The jitter attenuator -3 dB knee frequency depends on the settings of the Jitter Attenuator FIFO length and the Jitter Attenuator Corner Frequency bits 2 and 3, in the **Global Control Register (0Fh)** (See Section 14.16 on page 38)). Setting the lowest corner frequency guarantees jitter attenuation compliance to European specifications TBR 12/13 and ETSI ETS 300 011 in E1 mode. The jitter attenuator is also compliant with ITU-T G.735, G.742, G.783 and AT&T Pub. 62411 (Refer to **Figure 19** on page 58 and **Figure 20** on page 58).

12. OPERATIONAL SUMMARY

A brief summary of the CS61884 operations in hardware and host mode is provided in [Table 7](#).

Table 7. Operational Summary

| MCLK | TCLK | LOOP | Receive Mode | Transmit Mode | Loopback |
|--------|--------|------|--------------------|------------------|-----------------|
| Active | Active | Open | RCLK/Data Recovery | Unipolar/Bipolar | Disabled |
| Active | Active | L | RCLK/Data Recovery | Unipolar/Bipolar | Remote Loopback |
| Active | Active | H | RCLK/Data Recovery | Unipolar/Bipolar | Analog Loopback |
| Active | L | X | RCLK/Data Recovery | Power Down | Disabled |
| Active | H | Open | RCLK/Data Recovery | TAOS | Disabled |
| Active | H | L | RCLK/Data Recovery | Unipolar/Bipolar | Remote Loopback |
| Active | H | H | RCLK/Data Recovery | TAOS | Analog Loopback |
| L | Active | X | Power Down | Unipolar/Bipolar | Disabled |
| L | H | X | Power Down | RZ Data | Disabled |
| L | L | X | Power Down | Power Down | Disabled |
| H | Active | Open | Data Recovery | Unipolar/Bipolar | Disabled |
| H | Active | L | Data Recovery | RZ Data | Remote Loopback |
| H | Active | H | Data Recovery | Unipolar/Bipolar | Analog Loopback |
| H | L | Open | Data Recovery | Power Down | Disabled |
| H | L | L | Data Recovery | RZ Data | Remote Loopback |
| H | L | H | Data Recovery | Power Down | Disabled |
| H | H | Open | Data Recovery | RZ Data | Disabled |
| H | H | L | Data Recovery | RZ Data | Remote Loopback |
| H | H | H | Data Recovery | RZ Data | Analog Loopback |

12.1 Loopbacks

The CS61884 provides three loopback modes for each port. Analog Loopback connects the transmit signal on TTIP and TRING to RTIP and RRING. Digital Loopback Connects the output of the Encoder to the input of the Decoder (through the Jitter Attenuator if enabled). Remote Loopback connects the output of the Clock and Data Recovery block to the input of the Pulse Shaper block. (Refer to detailed descriptions below.) In hardware mode, the LOOP[7:0] pins are used to activate Analog or Remote loopback for each channel. In host mode, the Analog, Digital and Remote Loopback registers are used to enable these functions (Refer to the [Analog Loopback Register \(01h\)](#) (See Section 14.2 on page 35), [Remote Loopback Register \(02h\)](#) (See Section 14.3 on page 35), and [Digital Loopback Reset Register \(0Ch\)](#) (See Section 14.13 on page 37).

12.2 Analog Loopback

In Analog Loopback, the output of the TTIP/TRING driver is internally connected to the input of the RTIP/RRING receiver so that the data on TPOS/TNEG and TCLK appears on the RPOS/RNEG and RCLK outputs. In this mode the RTIP and RRING inputs are ignored. Refer to [Figure 8 on page 30](#). In hardware mode, Analog Loopback is selected by driving LOOP[7:0] high. In host mode, Analog Loopback is selected for a given channel using the appropriate bit in the [Analog Loopback Register \(01h\)](#) (See Section 14.2 on page 35).

NOTE: The simultaneous selection of Analog and Remote loopback modes is not valid. A TAOS request overrides the data on TPOS and TNEG during Analog Loopback. Refer to [Figure 9 on page 30](#).

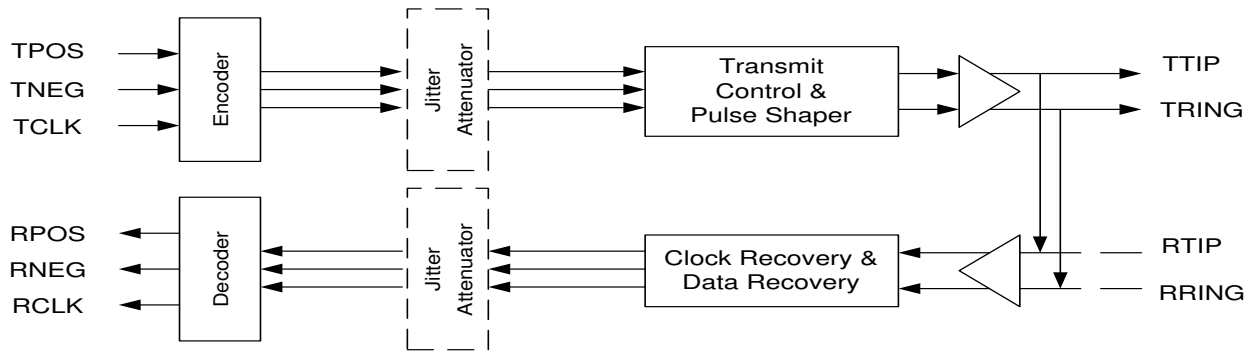


Figure 8. Analog Loopback Block Diagram

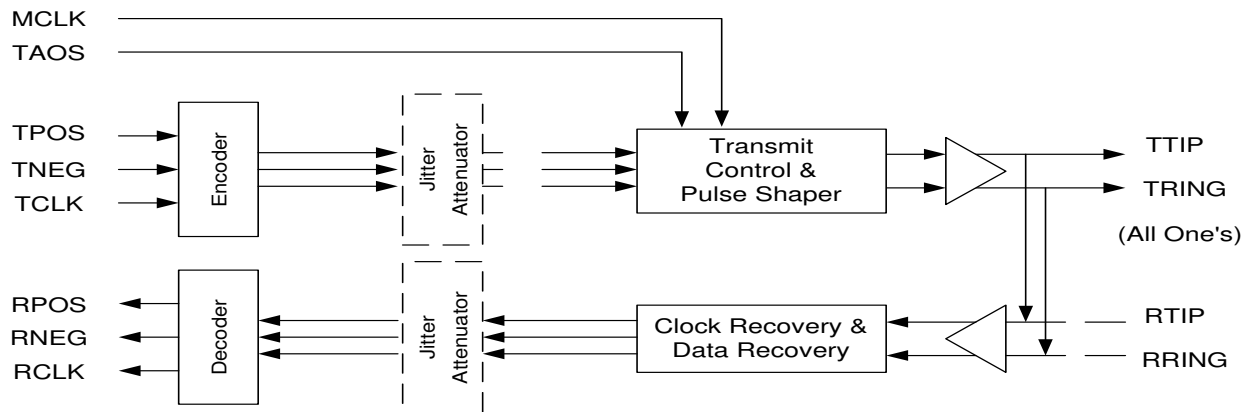


Figure 9. Analog Loopback with TAOS Block Diagram

12.3 Digital Loopback

Digital Loopback causes the TCLK, TPOS, and TNEG (or TDATA) inputs to be looped back through the jitter attenuator (if enabled) to the RCLK, RPOS, and RNEG (or RDATA) outputs. The receive line interface is ignored, but data at TPOS and TNEG (or TDATA) continues to be transmitted to the line interface at TTIP and TRING (Refer to [Figure 10 on page 31](#)).

Digital Loopback is only available during host mode. It is selected using the appropriate bit in the [Digital Loopback Reset Register \(0Ch\)](#) (See Section 14.13 on page 37).

NOTE: TAOS can also be used during the Digital Loopback operation for the selected channel (Refer to [Figure 11 on page 31](#)).

12.4 Remote Loopback

In remote loopback, the RPOS/RNEG and RCLK outputs are internally input to the transmit circuits for output on TTIP/TRING. In this mode the TCLK, TPOS and TNEG inputs are ignored. (Refer to [Figure 12 on page 31](#)). In hardware mode, Remote Loopback is selected by driving the LOOP pin for a certain channel low. In host mode, Remote Loopback is selected for a given channel by writing a one to the appropriate bit in the [Remote Loopback Register \(02h\)](#) (See Section 14.3 on page 35).

NOTE: In hardware mode, Remote Loopback overrides TAOS for the selected channel. In host mode, TAOS overrides Remote Loopback.

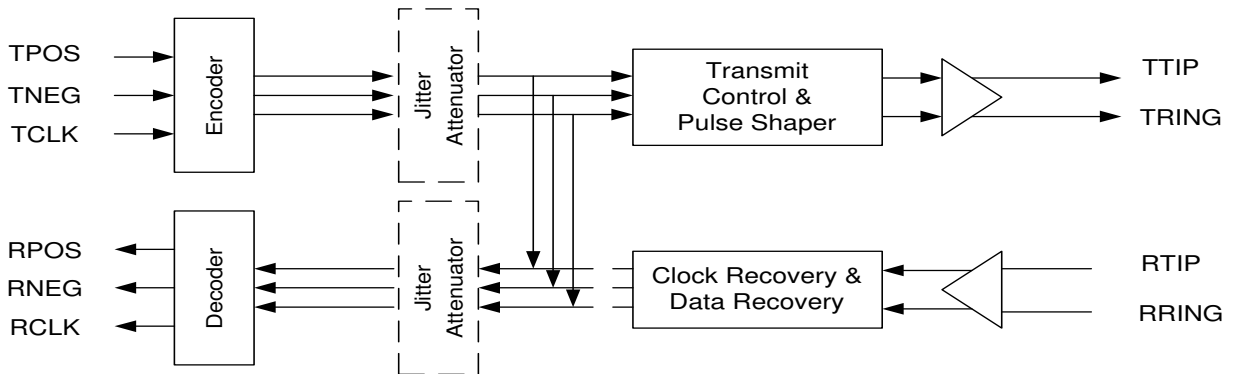


Figure 10. Digital Loopback Block Diagram

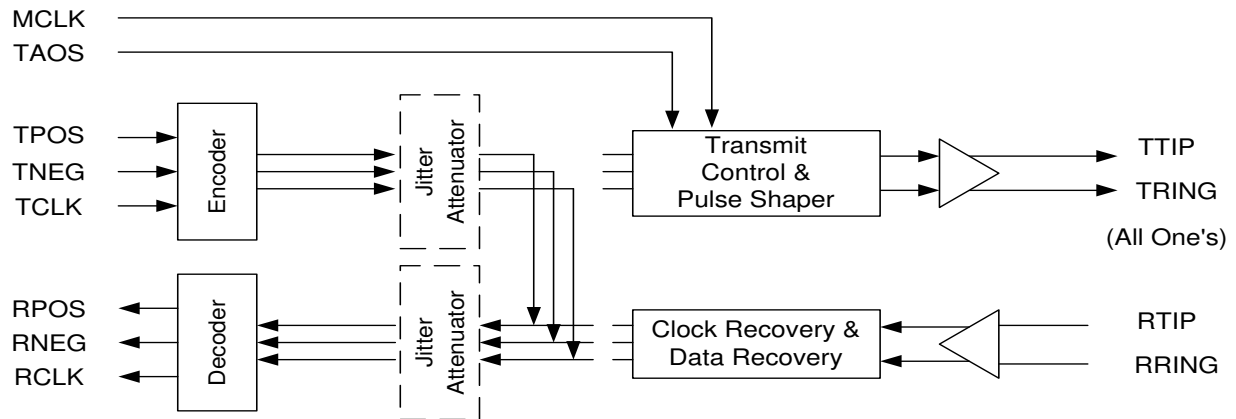


Figure 11. Digital Loopback with TAOS

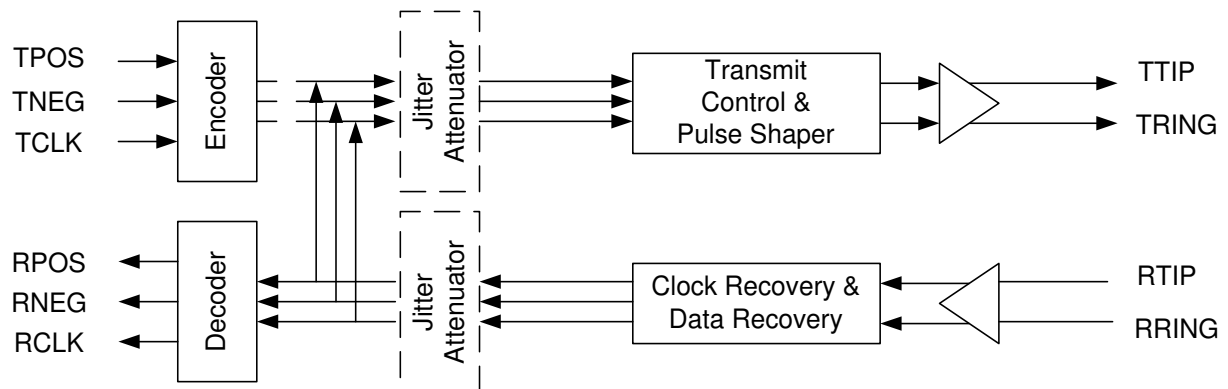


Figure 12. Remote Loopback Block Diagram

13. HOST MODE

Host mode allows the CS61884 to be configured and monitored using an internal register set. (Refer to [Table 1, “Operation Mode Selection,” on page 10](#)). The term, “Host mode” applies to both Parallel Host and Serial Host modes.

All of the internal registers are available in both Serial and Parallel Host mode; the only difference is in the functions of the interface pins, which are described in [Table 8](#).

Serial port operation is compatible with the serial ports of most microcontrollers. Parallel port operation can be configured to be compatible with 8-bit microcontrollers from Motorola or Intel, with both multiplexed or non-multiplexed address/data buses. (Refer to [Table 9 on page 34](#) for host mode registers).

13.1 SOFTWARE RESET

A software reset can be forced by writing the [Software Reset Register \(0Ah\)](#) (See Section 14.11 on page 36). A software reset initializes all registers to their default settings and initializes all internal state machines.

13.2 Serial Port Operation

Serial port host mode operation is selected when the MODE pin is left open or set to VCC/2. In this mode, the CS61884 register set is accessed by setting the chip select (\overline{CS}) pin low and communicating over the SDI, SDO, and SCLK pins. Timing over the serial port is independent of the transmit and receive system timing. [Figure 13](#) illustrates the format of serial port data transfers.

A read or write is initiated by writing an address/command byte (ACB) to SDI. Only the ADR0-ADR4 bits are valid; bits ADR5-ADR6 are do not cares. During a read cycle, the register data addressed by the ACB is output on SDO on the next eight SCLK clock cycles. During a write cycle, the data byte immediately follows the ACB.

Data is written to and read from the serial port in LSB first format. When writing to the port, SDI data is sampled by the device on the rising edge of SCLK. The valid clock edge of the data on SDO is controlled by the CLKE pin. When CLKE is low, data on SDO is valid on the falling edge of SCLK. When CLKE is high, data on SDO is valid on the raising edge of SCLK. The SDO pin is Hi-Z when not transmitting. If the host processor has a bidirectional I/O port, SDI and SDO may be tied together.

Table 8. Host Control Signal Descriptions

| HOST CONTROL SIGNAL DESCRIPTIONS | | | | |
|----------------------------------|-------|-----------|-----------------|-----------------|
| PIN NAME | PIN # | HARDWARE | SERIAL | PARALLEL |
| MODE | 11 | LOW | VDD/2 | HIGH |
| MUX | 43 | BITSEN0 | - | MUX |
| CODEN/MOT/INTL | 88 | CODEN | - | MOT/INTL |
| ADDR [4] | 12 | GND | - | ADDR[4] |
| ADDR[3:0] | 13-16 | ADDR[3:0] | - | ADDR [3:0] |
| LOOP[7:0], DATA[7:0] | 28-21 | LOOP[7:0] | - | DATA[7:0] |
| INT | 82 | Pulled Up | INT | INT |
| SDO/ACK/RDY | 83 | NC | SDO | ACK/RDY |
| LEN0/SDI/DS/WR | 84 | LEN0 | SDI | DS/WR |
| LEN1/R/W/RD | 85 | LEN1 | - | R/W/RD |
| LEN2/SCLK/AS/ALE | 86 | LEN2 | SCLK | AS/ALE |
| JASEL/ \overline{CS} | 87 | JASEL | \overline{CS} | \overline{CS} |

As illustrated in [Figure 13](#), the ACB consists of a R/\overline{W} bit, address field, and two reserved bits. The R/\overline{W} bit specifies if the current register access is a read ($R/\overline{W} = 1$) or a write ($R/\overline{W} = 0$) operation. The address field specifies the register address from 0x00 to 0x1f.

13.3 Parallel Port Operation

Parallel port host mode operation is selected when the MODE pin is high. In this mode, the CS61884 register set is accessed using an 8-bit, multiplexed bidirectional address/data bus D[7:0]. Timing over the parallel port is independent of the transmit and receive system timing.

The device is compatible with both Intel and Motorola bus formats. The Intel bus format is selected when the $\overline{MOT}/INTL$ pin is high and the Motorola bus format is selected when the $\overline{MOT}/INTL$ pin is low. In either mode, the interface can have the address and data multiplexed over the same 8-bit bus or on separate busses. This operation is controlled with the MUX pin; MUX = 1 means that the parallel port has its address and data multiplexed over the same bus; MUX = 0 defines a non-multiplexed bus. The timing for the different modes are shown in [Figure 26](#), [Figure 27](#), [Figure 28](#), [Figure 29](#), [Figure 30](#), [Figure 31](#), [Figure 32](#) and [Figure 33](#).

Non-multiplexed Intel and Motorola modes are shown in [Figure 30](#), [Figure 31](#), [Figure 32](#) and [Figure 33](#). The \overline{CS} pin initiates the cycle, followed by the \overline{DS} , \overline{RD} or \overline{WR} pin. Data is latched into or out of the part using the rising edge of the \overline{DS} , \overline{WR} or \overline{RD} pin. Raising \overline{CS} ends the cycle.

Multiplexed Intel and Motorola modes are shown in [Figure 26](#), [Figure 27](#), [Figure 28](#) and [Figure 29](#). A read or write is initiated by writing an address byte to D[7:0]. The device latches the address on the falling edge of $ALE(\overline{AS})$. During a read cycle, the register data is output during the later portion of the \overline{RD} or \overline{DS} pulses. The read cycle is terminated and the bus returns to a high impedance state as \overline{RD} transitions high in Intel timing or \overline{DS} transitions high in Motorola timing. During a write cycle, valid write data must be present and held stable during the \overline{WR} or \overline{DS} pulses.

In Intel mode, the RDY output pin is normally in a high impedance state; it pulses low once to acknowledge that the chip has been selected, and high again to acknowledge that data has been written or read. In Motorola mode, the \overline{ACK} pin performs a similar function; it drives high to indicate that the address has been received by the part, and goes low again to indicate that data has been written or read.

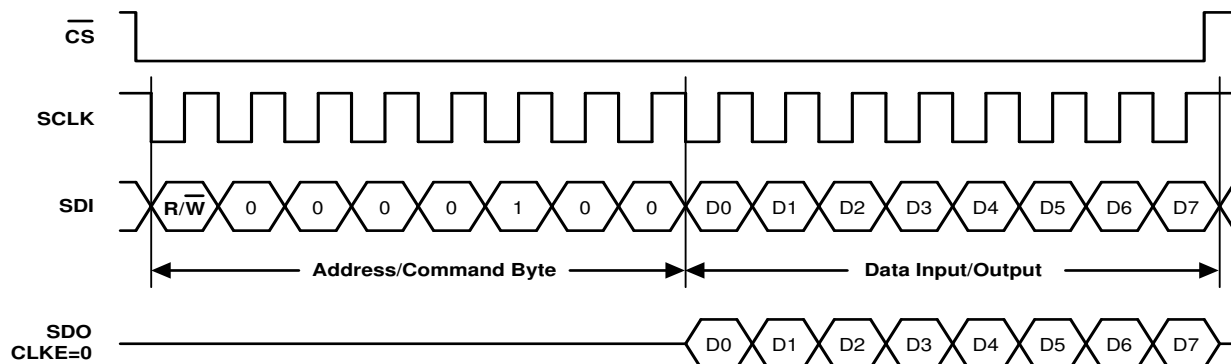


Figure 13. Serial Read/Write Format (SPOL = 0)

13.4 Register Set

The register set available during host mode operations are presented in [Table 9](#). While the upper

three bits of the parallel address are don't cares on the CS61884, they should be set to zero for proper operation.

Table 9. Host Mode Register Set

| REGISTERS | | | BITS | | | | | | | |
|-----------|-------------------------------|------|---|------------------|--------|---------------------|----------|------------|-------------|--------|
| ADDR | NAME | TYPE | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 00h | Revision/IDCODE | R | IDCODE Refer to Device ID Register (IDR) on page 48 | | | | | | | |
| 01h | Analog Loopback | R/W | ALBK 7 | ALBK 6 | ALBK 5 | ALBK 4 | ALBK 3 | ALBK 2 | ALBK 1 | ALBK 0 |
| 02h | Remote Loopback | R/W | RLBK 7 | RLBK 6 | RLBK 5 | RLBK 4 | RLBK 3 | RLBK 2 | RLBK 1 | RLBK 0 |
| 03h | TAOS Enable | R/W | TAOE 7 | TAOE 6 | TAOE 5 | TAOE 4 | TAOE 3 | TAOE 2 | TAOE 1 | TAOE 0 |
| 04h | LOS Status | R | LOSS 7 | LOSS 6 | LOSS 5 | LOSS 4 | LOSS 3 | LOSS 2 | LOSS 1 | LOSS 0 |
| 05h | DFM Status | R | DFMS 7 | DFMS 6 | DFMS 5 | DFMS 4 | DFMS 3 | DFMS 2 | DFMS 1 | DFMS 0 |
| 06h | LOS Interrupt Enable | R/W | LOSE 7 | LOSE 6 | LOSE 5 | LOSE 4 | LOSE 3 | LOSE 2 | LOSE 1 | LOSE 0 |
| 07h | DFM Interrupt Enable | R/W | DFME 7 | DFME 6 | DFME 5 | DFME 4 | DFME 3 | DFME 2 | DFME 1 | DFME 0 |
| 08h | LOS Interrupt Status | R | LOSI 7 | LOSI 6 | LOSI 5 | LOSI 4 | LOSI 3 | LOSI 2 | LOSI 1 | LOSI 0 |
| 09h | DFM Interrupt Status | R | DFMI 7 | DFMI 6 | DFMI 5 | DFMI 4 | DFMI 3 | DFMI 2 | DFMI 1 | DFMI 0 |
| 0Ah | Software Reset | R/W | SRES 7 | SRES 6 | SRES 5 | SRES 4 | SRES 3 | SRES 2 | SRES 1 | SRES 0 |
| 0Bh | Performance Monitor | R/W | RSVD | RSVD | RSVD | RSVD | A3 | A2 | A1 | A0 |
| 0Ch | Digital Loopback | R/W | DLBK 7 | DLBK 6 | DLBK 5 | DLBK 4 | DLBK 3 | DLBK 2 | DLBK 1 | DLBK 0 |
| 0Dh | LOS/AIS Mode Enable | R/W | LAME 7 | LAME 6 | LAME 5 | LAME 4 | LAME 3 | LAME 2 | LAME 1 | LAME 0 |
| 0Eh | Automatic TAOS | R/W | ATAO 7 | ATAO 6 | ATAO 5 | ATAO 4 | ATAO 3 | ATAO 2 | ATAO 1 | ATAO 0 |
| 0Fh | Global Control | R/W | AI | Raisen | RSVD | Coden | FIFO | JACF | JASEL [1:0] | |
| 10h | Line Length Channel ID | R/W | RSVD | RSVD | RSVD | RSVD | RSVD | Channel ID | | |
| 11h | Line Length Data | R/W | RSVD | RSVD | RSVD | IN_EX | LEN[3:0] | | | |
| 12h | Output Disable | R/W | OENB 7 | OENB 6 | OENB 5 | OENB 4 | OENB 3 | OENB 2 | OENB 1 | OENB 0 |
| 13h | AIS Status | R | AISS 7 | AISS 6 | AISS 5 | AISS 4 | AISS 3 | AISS 2 | AISS 1 | AISS 0 |
| 14h | AIS Interrupt Enable | R/W | AISE 7 | AISE 6 | AISE 5 | AISE 4 | AISE 3 | AISE 2 | AISE 1 | AISE 0 |
| 15h | AIS Interrupt Status | R | AISI 7 | AISI 6 | AISI 5 | AISI 4 | AISI 3 | AISI 2 | AISI 1 | AISI 0 |
| 16h | AWG Broadcast | R/W | AWGB 7 | AWGB 6 | AWGB 5 | AWGB 4 | AWGB 3 | AWGB 2 | AWGB 1 | AWGB 0 |
| 17h | AWG Phase Address | R/W | Channel Address [2:0] | | | Phase Address [4:0] | | | | |
| 18h | AWG Phase Data | R/W | RSVD | Sample Data[6:0] | | | | | | |
| 19h | AWG Enable | R/W | AWGN 7 | AWGN 6 | AWGN 5 | AWGN 4 | AWGN 3 | AWGN 2 | AWGN 1 | AWGN 0 |
| 1Ah | AWG Overflow Interrupt Enable | R/W | AWGE 7 | AWGE 6 | AWGE 5 | AWGE 4 | AWGE 3 | AWGE 2 | AWGE 1 | AWGE 0 |
| 1Bh | AWG Overflow Interrupt Status | R | AWGI 7 | AWGI 6 | AWGI 5 | AWGI 4 | AWGI 3 | AWGI 2 | AWGI 1 | AWGI 0 |
| 1Ch | RESERVED | R/W | RSVD 6 | RSVD 5 | RSVD 4 | RSVD 3 | RSVD 2 | RSVD 1 | RSVD 0 | RSVD 6 |
| 1Dh | RESERVED | R | RSVD 6 | RSVD 5 | RSVD 4 | RSVD 3 | RSVD 2 | RSVD 1 | RSVD 0 | RSVD 6 |
| 1Eh | BITS Clock Enable | R/W | BITS 7 | BITS 6 | BITS 5 | BITS 4 | BITS 3 | BITS 2 | BITS 1 | BITS 0 |
| 1Fh | RESERVED | R/W | RSVD 7 | RSVD 6 | RSVD 5 | RSVD 4 | RSVD 3 | RSVD 2 | RSVD 1 | RSVD 0 |

14. REGISTER DESCRIPTIONS

14.1 Revision/IDcode Register (00h)

| BIT | NAME | Description |
|-------|----------|---|
| [7:4] | REVI 7-4 | Bits [7:4] are taken from the least-significant nibble of the Device IDCode, which are 0100. (Refer to Device ID Register (IDR) (See Section 16.3 on page 48). |
| [3:0] | REVI 3-0 | Bits [3:0] are the revision bits from the JTAG IDCODE register, CS61884 Revision A = 0000. These bits are subject to change with the revision of the device (Refer to Device ID Register (IDR) (See Section 16.3 on page 48). |

14.2 Analog Loopback Register (01h)

| BIT | NAME | Description |
|-------|----------|--|
| [7:0] | ALBK 7-0 | Enables analog loopbacks. A “1” in bit n enables the loopback for channel n. Refer to Analog Loopback (See Section 12.2 on page 29) for a complete explanation. Register bits default to 00h after power-up or reset. |

14.3 Remote Loopback Register (02h)

| BIT | NAME | Description |
|-------|----------|--|
| [7:0] | RLBK 7-0 | Enables remote loopbacks. A “1” in bit n enables the loopback for channel n. Refer to Remote Loopback (See Section 12.4 on page 30) for a complete explanation. Register bits default to 00h after power-up or reset. |

14.4 TAOS Enable Register (03h)

| BIT | NAME | Description |
|-------|----------|--|
| [7:0] | TAOE 7-0 | A “1” in bit n of this register turns on the TAOS generator in channel n. Register bits default to 00h after power-up or reset. |

14.5 LOS Status Register (04h)

| BIT | NAME | Description |
|-------|----------|---|
| [7:0] | LOSS 7-0 | Register bit n is read as “1” when LOS is detected on channel n. Register bits default to 00h after power-up or reset. |

14.6 DFM Status Register (05h)

| BIT | NAME | Description |
|-------|----------|--|
| [7:0] | DFMS 7-0 | Driver Failure Monitor. The DFM will set bit n to “1” when it detects a short circuit in channel n. Register bits default to 00h after power-up or reset. |

14.7 LOS Interrupt Enable Register (06h)

| BIT | NAME | Description |
|-------|----------|---|
| [7:0] | LOSE 7-0 | Any change in a LOS Status Register bits will cause the INT pin to go low if corresponding bit in this register is set to "1". Register bits default to 00h after power-up or reset. |

14.8 DFM Interrupt Enable Register (07h)

| BIT | NAME | Description |
|-------|----------|--|
| [7:0] | DFME 7-0 | Enables interrupts for failures detected by the DFM. Any change in a DFM Status Register bit will cause an interrupt if the corresponding bit is set to "1" in this register. Register bits default to 00h after power-up or reset. |

14.9 LOS Interrupt Status Register (08h)

| BIT | NAME | Description |
|-------|----------|--|
| [7:0] | LOSI 7-0 | Bit n of this register is set to "1" to indicate a status change in bit n of the LOS Status Register. The bits in this register indicate a change in status since the last cleared LOS interrupt. Register bits default to 00h after power-up or reset. |

14.10 DFM Interrupt Status Register (09h)

| BIT | NAME | Description |
|-------|----------|--|
| [7:0] | DFMI 7-0 | Bit n of this register is set to "1" to indicate a status change in bit n of the DFM Status Register. The bits in this register indicate a change in status since the last cleared DFM interrupt. Register bits default to 00h after power-up or reset. |

14.11 Software Reset Register (0Ah)

| BIT | NAME | Description |
|-------|----------|--|
| [7:0] | SRES 7-0 | Writing to this register initializes all registers to their default settings. Register bits default to 00h after power-up or reset. |

14.12 Performance Monitor Register (0Bh)

| BIT | NAME | Description |
|-------|----------|---|
| [7:4] | RSVD 7-4 | RESERVED (These bits must be set to 0.) |

(Continued)

| BIT | NAME | Description | |
|-------|---------------|---|---------------------|
| [3:0] | A[3:0] | The G.772 Monitor is directed to a given channel based on the state of the four least significant bits of this register. Register bits default to 00h after power-up or reset. The following table shows the settings needed to select a specific channel's receiver or transmitter to perform G.772 monitoring. | |
| | | A[3:0] | Channel Selection |
| | | 0000 | Monitoring Disabled |
| | | 0001 | RX Channel #1 |
| | | 0010 | RX Channel #2 |
| | | 0011 | RX Channel #3 |
| | | 0100 | RX Channel #4 |
| | | 0101 | RX Channel #5 |
| | | 0110 | RX Channel #6 |
| | | 0111 | RX Channel #7 |
| | | 1000 | Monitoring Disabled |
| | | 1001 | TX Channel #1 |
| | | 1010 | TX Channel #2 |
| | | 1011 | TX Channel #3 |
| | | 1100 | TX Channel #4 |
| | | 1101 | TX Channel #5 |
| | | 1110 | TX Channel #6 |
| 1111 | TX Channel #7 | | |

14.13 Digital Loopback Reset Register (0Ch)

| BIT | NAME | Description |
|-------|----------|--|
| [7:0] | DLBK 7-0 | Setting register bit n to "1" enables the digital loopback for channel n. Refer to Digital Loopback (See Section 12.3 on page 30) for a complete explanation. Register bits default to 00h after power-up or reset. |

14.14 LOS/AIS Mode Enable Register (0Dh)

| BIT | NAME | Description |
|-------|----------|--|
| [7:0] | LAME 7-0 | T1/J1 MODE - These bits are "Do Not Care", T1.231 Compliant LOS/AIS already used. E1 Mode - Setting bit n to "1" enables ETSI 300 233 compliant LOS/AIS for channel n; setting bit n to "0" enables ITU G.775 compliant LOS/AIS for channel n. Register bits default to 00h after power-up or reset. |

14.15 Automatic TAOS Register (0Eh)

| BIT | NAME | Description |
|-------|----------|--|
| [7:0] | ATAO 7-0 | Setting bit n to "1" enables automatic TAOS generation on channel n when LOS is detected. Register bits default to 00h after power-up or reset. |

14.16 Global Control Register (0Fh)

| BIT | NAME | Description | | | | | | | | | | | | | | | |
|------------|---------------------------|--|---------|---------|------------|--------|------------|----------|---|---|---------------|---|---|----------|---|---|--------------|
| | | This register is the global control for the AWG Auto-Increment, Automatic AIS insertion, encoding/decoding and the jitter attenuators location, FIFO length and corner frequency for all eight channels. Register bits default to 00h after power-up or reset. | | | | | | | | | | | | | | | |
| [7] | AWG Auto-Increment | The AWG Auto-Increment bit indicates whether to auto-increment the AWG Phase Address Register (17h) (See Section 14.24 on page 40) after each access. Thus, when this bit is set, the phase samples address portion of the address register increments after each read or write access. This bit must be set before any bit in the AWG Enable register is set, if this function is required. | | | | | | | | | | | | | | | |
| [6] | RAISEN | On LOS, this bit controls the automatic AIS insertion into all eight receiver paths. 0 = Disabled 1 = Enabled | | | | | | | | | | | | | | | |
| [5] | RSVD | RESERVED (This bit must be set to 0.) | | | | | | | | | | | | | | | |
| [4] | $\overline{\text{CODEN}}$ | Line encoding/decoding Selection 0 = B8ZS/HDB3 (T1/J1/E1 respectively) 1 = AMI | | | | | | | | | | | | | | | |
| [3] | FIFO LENGTH | Jitter Attenuator FIFO length Selection 0 = 32 bits 1 = 64 bits | | | | | | | | | | | | | | | |
| [2] | JACF | Jitter Attenuator Corner Frequency Selection <table style="display: inline-table; border: none;"> <tr> <td>E1</td> <td>T1/J1</td> </tr> <tr> <td>0 = 1.25Hz</td> <td>3.78Hz</td> </tr> <tr> <td>1 = 2.50Hz</td> <td>7.56Hz</td> </tr> </table> | E1 | T1/J1 | 0 = 1.25Hz | 3.78Hz | 1 = 2.50Hz | 7.56Hz | | | | | | | | | |
| E1 | T1/J1 | | | | | | | | | | | | | | | | |
| 0 = 1.25Hz | 3.78Hz | | | | | | | | | | | | | | | | |
| 1 = 2.50Hz | 7.56Hz | | | | | | | | | | | | | | | | |
| [1:0] | JASEL [1:0] | These bits select the position of the Jitter Attenuator. <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>JASEL 1</th> <th>JASEL 0</th> <th>POSITION</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Disabled</td> </tr> <tr> <td>0</td> <td>1</td> <td>Transmit Path</td> </tr> <tr> <td>1</td> <td>0</td> <td>Disabled</td> </tr> <tr> <td>1</td> <td>1</td> <td>Receive Path</td> </tr> </tbody> </table> | JASEL 1 | JASEL 0 | POSITION | 0 | 0 | Disabled | 0 | 1 | Transmit Path | 1 | 0 | Disabled | 1 | 1 | Receive Path |
| JASEL 1 | JASEL 0 | POSITION | | | | | | | | | | | | | | | |
| 0 | 0 | Disabled | | | | | | | | | | | | | | | |
| 0 | 1 | Transmit Path | | | | | | | | | | | | | | | |
| 1 | 0 | Disabled | | | | | | | | | | | | | | | |
| 1 | 1 | Receive Path | | | | | | | | | | | | | | | |

14.17 Line Length Channel ID Register (10h)

| BIT | NAME | Description |
|-------|----------|--|
| [7:3] | RSVD 7-3 | RESERVED (These bits must be set to 0.) |
| [2:0] | LLID 2-0 | The value written to these bits specify the LIU channel for which the Pulse Shape Configuration Data (register 11h) applies. For example, writing a value of a binary 000 to the 3-LSBs will select channel 0. The pulse shape configuration data for the channel specified in this register are written or read through the Line Length Data Register (11h). Register bits default to 00h after power-up or reset. |

14.18 Line Length Data Register (11h)

| BIT | NAME | Description | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-----------|----------------|---|----------------------|----------------|-----------------------|----------------------|------|----|-----------|----|------|-------|---------------------------------|----|------|-------|--------------------------|----|------|-------|------------------------|----|------|-------|--------------------------|----|------|-------|--------------------------|----|------|-------|--------------------------|----|------|-------|--------------------------|----|------|----|-----------|----|
| | | The value written to the 4-LSBs of this register specifies whether the device is operating in either T1/J1 or E1 modes and the associated pulse shape as shown below is being transmitted. Register bits default to 00h after power-up or reset. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| [7:5] | RSVD | RESERVED (These bits must be set to 0.) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| [4] | INT_EXTB | This bit specifies the use of internal (Int_ExtB = 1) or external (Int_ExtB = 0) receiver line matching. The line impedance for both the receiver and transmitter are chosen through the LEN [3:0] bits in this register. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| [3:0] | LEN[3:0] | These bits setup the line impedance for both the receiver and the transmitter path and the desired pulse shape for a specific channel. The channel is selected with the Line Length Channel ID register (0x10). The following table shows the available transmitter pulse shapes. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | <table border="1"> <thead> <tr> <th>LEN [3:0]</th> <th>Operation Mode</th> <th>Line Length Selection</th> <th>Phase Samples per UI</th> </tr> </thead> <tbody> <tr> <td>0000</td> <td>E1</td> <td>120Ω 3.0V</td> <td>12</td> </tr> <tr> <td>0001</td> <td>T1/J1</td> <td>100Ω DS1, Option A (undershoot)</td> <td>14</td> </tr> <tr> <td>0010</td> <td>T1/J1</td> <td>100Ω DS1, Option A (0dB)</td> <td>14</td> </tr> <tr> <td>0011</td> <td>T1/J1</td> <td>100Ω 0 - 133Ft (0.6dB)</td> <td>13</td> </tr> <tr> <td>0100</td> <td>T1/J1</td> <td>100Ω 133 - 266Ft (1.2dB)</td> <td>13</td> </tr> <tr> <td>0101</td> <td>T1/J1</td> <td>100Ω 266 - 399Ft (1.2dB)</td> <td>13</td> </tr> <tr> <td>0110</td> <td>T1/J1</td> <td>100Ω 399 - 533Ft (2.4dB)</td> <td>13</td> </tr> <tr> <td>0111</td> <td>T1/J1</td> <td>100Ω 533 - 655Ft (3.0dB)</td> <td>13</td> </tr> <tr> <td>1000</td> <td>E1</td> <td>75Ω 2.37V</td> <td>12</td> </tr> </tbody> </table> | LEN [3:0] | Operation Mode | Line Length Selection | Phase Samples per UI | 0000 | E1 | 120Ω 3.0V | 12 | 0001 | T1/J1 | 100Ω DS1, Option A (undershoot) | 14 | 0010 | T1/J1 | 100Ω DS1, Option A (0dB) | 14 | 0011 | T1/J1 | 100Ω 0 - 133Ft (0.6dB) | 13 | 0100 | T1/J1 | 100Ω 133 - 266Ft (1.2dB) | 13 | 0101 | T1/J1 | 100Ω 266 - 399Ft (1.2dB) | 13 | 0110 | T1/J1 | 100Ω 399 - 533Ft (2.4dB) | 13 | 0111 | T1/J1 | 100Ω 533 - 655Ft (3.0dB) | 13 | 1000 | E1 | 75Ω 2.37V | 12 |
| LEN [3:0] | Operation Mode | Line Length Selection | Phase Samples per UI | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0000 | E1 | 120Ω 3.0V | 12 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0001 | T1/J1 | 100Ω DS1, Option A (undershoot) | 14 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0010 | T1/J1 | 100Ω DS1, Option A (0dB) | 14 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0011 | T1/J1 | 100Ω 0 - 133Ft (0.6dB) | 13 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0100 | T1/J1 | 100Ω 133 - 266Ft (1.2dB) | 13 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0101 | T1/J1 | 100Ω 266 - 399Ft (1.2dB) | 13 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0110 | T1/J1 | 100Ω 399 - 533Ft (2.4dB) | 13 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0111 | T1/J1 | 100Ω 533 - 655Ft (3.0dB) | 13 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1000 | E1 | 75Ω 2.37V | 12 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

14.19 Output Disable Register (12h)

| BIT | NAME | Description |
|-------|----------|--|
| [7:0] | OENB 7-0 | Setting bit n of this register to “1” High-Z the TX output driver on channel n of the device. Register bits default to 00h after power-up or reset. |

14.20 AIS Status Register (13h)

| BIT | NAME | Description |
|-------|----------|---|
| [7:0] | AISS 7-0 | A “1” in bit position n indicates that the receiver has detected an AIS condition on channel n, which generates an interrupt on the INT pin. Register bits default to 00h after power-up or reset. |

14.21 AIS Interrupt Enable Register (14h)

| BIT | NAME | Description |
|-------|----------|---|
| [7:0] | AISE 7-0 | This register enables changes in the AIS Status register to be reflected in the AIS Interrupt Status register, thus causing an interrupt on the INT pin. Register bits default to 00h after power-up or reset. |

14.22 AIS Interrupt Status Register (15h)

| BIT | NAME | Description |
|-------|----------|---|
| [7:0] | AISI 7-0 | Bit n is set to "1" to indicate a change of status of bit n in the AIS Status Register. The bits in this register indicate which channel changed in status since the last cleared AIS interrupt. Register bits default to 00h after power-up or reset. |

14.23 AWG Broadcast Register (16h)

| BIT | NAME | Description |
|-------|----------|---|
| [7:0] | AWGB 7-0 | Setting bit n to "1" causes the phase data in the AWG Phase Data Register to be written to the corresponding channel or channels simultaneously. (Refer to Arbitrary Waveform Generator (See Section 15 on page 43). Register bits default to 00h after power-up or reset. |

14.24 AWG Phase Address Register (17h)

| BIT | NAME | Description |
|-------|---------|--|
| [7:5] | AWGA | These bits specify the target channel 0-7. (Refer to Arbitrary Waveform Generator (See Section 15 on page 43). Register bits default to 00h after power-up or reset. |
| [4:0] | PA[4:0] | These bits specify 1 of 24 (E1) or 26/28 (T1/J1) phase sample address locations of the AWG, that the phase data in the AWG Phase Data Register is written to or read from. The other locations in each channel's phase sample addresses are not used, and should not be accessed. Register bits default to 00h after power-up or reset. |

14.25 AWG Phase Data Register (18h)

| BIT | NAME | Description |
|-------|------------|--|
| [7] | RSVD | RESERVED (This bit must be set to 0.) |
| [6:0] | AWGD [6:0] | These bits are used for the pulse shape data that will be written to the AWG phase location specified by the AWG Phase Address Register. The value written to or read from this register will be written to or read from the AWG phase sample location specified by the AWG Phase Address register. A software reset through the Software Reset Register does not effect the contents of this register. The data in each phase is a 7-bit 2's complement number (the maximum positive value is 3Fh and the maximum negative value is 40h). (Refer to Arbitrary Waveform Generator (See Section 15 on page 43). Register bits default to 00h after power-up. |

14.26 AWG Enable Register (19h)

| BIT | NAME | Description |
|-------|----------|--|
| [7:0] | AWGN 7-0 | The AWG enable register is used for selecting the source of the customized transmission pulse-shape. Setting bit n to "1" in this register selects the AWG as the source of the output pulse shape for channel n. When bit n is set to "0" the pre-programmed pulse shape in the ROM is selected for transmission on channel n. (Refer to Arbitrary Waveform Generator (See Section 15 on page 43). Register bits default to 00h after power-up or reset. |

14.27 AWG Overflow Interrupt Enable Register (1Ah)

| BIT | NAME | Description |
|-------|----------|---|
| [7:0] | AWGE 7-0 | This register enables changes in the overflow status to be reflected in the AWG Interrupt Status register, thus causing as interrupt on the INT pin. Interrupts are maskable on a per-channel basis. Register bits default to 00h after power-up or reset. |

14.28 AWG Overflow Interrupt Status Register (1Bh)

| BIT | NAME | Description |
|-------|----------|---|
| [7:0] | AWGI 7-0 | The bits in this register indicate a change in status since the last AWG overflow interrupt. An AWG overflow occurs when invalid phase data are entered, such that a sample-by-sample addition of UI0 and UI1 results in values that exceed the arithmetic range of the 7-bit representation. Reading this register clears the interrupt, which deactivates the INT pin. Register bits default to 00h after power-up or reset. |

14.29 Reserved Register (1Ch)

| BIT | NAME | Description |
|-------|----------|--|
| [7:0] | RSVD 7-0 | RESERVED (These bits must be set to zero.) |

14.30 Reserved Register (1Dh)

| BIT | NAME | Description |
|-------|----------|--|
| [7:0] | RSVD 7-0 | RESERVED (These bits must be set to zero.) |

14.31 Bits Clock Enable Register (1Eh)

| BIT | NAME | Description |
|-------|----------|--|
| [7:0] | BITS 7-0 | Setting a "1" to bit n in this register changes channel n to a stand-alone timing recovery unit used for G.703 clock recovery. (Refer to BUILDING INTEGRATED TIMING SYSTEMS (BITS) CLOCK MODE (See Section 8 on page 23) for a better description of the G.703 clock recovery function). Register bits default to 00h after power-up or reset. |

14.32 Reserved Register (1Fh)

| BIT | NAME | Description |
|-------|----------|--|
| [7:0] | RSVD 7-0 | RESERVED (These bits must be set to zero.) |

14.33 Status Registers

The following Status registers are read-only: **LOS Status Register (04h)** (See Section 14.5 on page 35), **DFM Status Register (05h)** (See Section 14.6 on page 35) and **AIS Status Register (13h)** (See Section 14.20 on page 39). The CS61884 generates an interrupt on the $\overline{\text{INT}}$ pin any time an unmasked status register bit changes.

14.33.1 Interrupt Enable Registers

The Interrupt Enable registers: **LOS Interrupt Enable Register (06h)** (See Section 14.7 on page 36), **DFM Interrupt Enable Register (07h)** (See Section 14.8 on page 36), **AIS Interrupt Enable Register (14h)** (See Section 14.21 on page 39) and **AWG Overflow Interrupt Enable Register (1Ah)** (See Section 14.27 on page 41), enable changes in status register state to cause an interrupt

on the $\overline{\text{INT}}$ pin. Interrupts are maskable on a per channel basis. When an Interrupt Enable register bit is 0, the corresponding Status register bit is disabled from causing an interrupt on the $\overline{\text{INT}}$ pin.

NOTE: Disabling an interrupt has no effect on the status reflected in the associated status register.

14.33.2 Interrupt Status Registers

The following interrupt status registers: **LOS Interrupt Status Register (08h)** (See Section 14.9 on page 36), **DFM Interrupt Status Register (09h)** (See Section 14.10 on page 36), **AIS Interrupt Status Register (15h)** (See Section 14.22 on page 40) and **AWG Overflow Interrupt Status Register (1Bh)** (See Section 14.28 on page 41), indicate a change in status of the corresponding status registers in host mode. Reading these registers clears the interrupt, which deactivates the $\overline{\text{INT}}$ pin.

15. ARBITRARY WAVEFORM GENERATOR

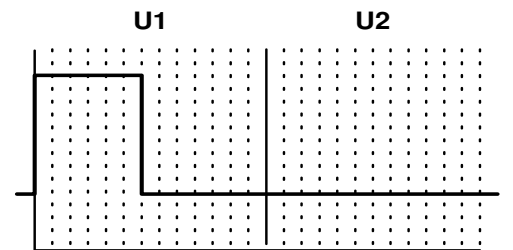
Using the Arbitrary Waveform Generator (AWG) allows the user to customize the transmit pulse shapes to compensate for nonstandard cables, transformers, protection circuitry, or to reduce power consumption by reducing the output pulse amplitude. A channel is configured for a custom pulse shape by storing data representing the pulse shape into the 24/26/28 phase sample locations and then enabling the AWG for that channel. Each channel has a separate AWG, so all eight channels can have a different customized pulse shape. The microprocessor interface, is used to read from or write to the AWG, while the device is in host mode.

In the AWG RAM, the pulse shape is divided into two unit intervals (UI). For E1 mode, there are 12 sample phases in each UI, while in T1/J1 mode, the number of sample phases per UI are either 13 or 14. The first UI is for the main part of the pulse and the second UI is for the “tail” of the pulse (Refer to [Figure 14](#)). A complete pulse-shape is represented by 24 phase samples in E1 mode or 26/28 phase samples in T1/J1 mode. In E1 mode, data written in the first UI represents a valid pulse shape, while data in the second UI is ignored and should be set to zero.

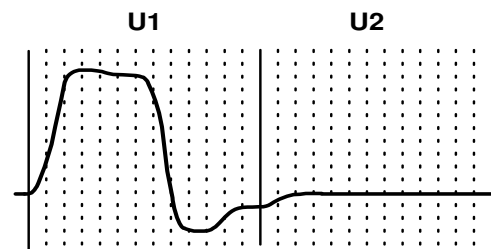
The mode of operation is selected using the [Line Length Channel ID Register \(10h\)](#) (See Section 14.17 on page 38) and the [Line Length Data Register \(11h\)](#) (See Section 14.18 on page 39). A phase sample, or cell, is accessed by first loading the channel address and the phase sample address into the [AWG Phase Address Register \(17h\)](#) (See Section 14.24 on page 40), and then reading or writing the [AWG Phase Data Register \(18h\)](#) (See Section 14.25 on page 40). The upper locations in each channel’s address space are not used; reading and writing to these registers produces undefined results.

The data in each phase sample is a 7-bit two’s complement number with a maximum positive value of 0x3f, and a maximum negative value of 0x40. The terms “positive” and “negative” are defined for a positive going pulse only. The pulse generation circuitry automatically inverts the pulse for negative going pulses. The data stored in the lowest phase address corresponds to the first phase sample that will be transmitted in time. When the mode of operation calls for only 24/26 phase samples if the phase samples that are not used (25 through 28) are written to, they are ignored and don’t effect the shape of the customized pulse shape.

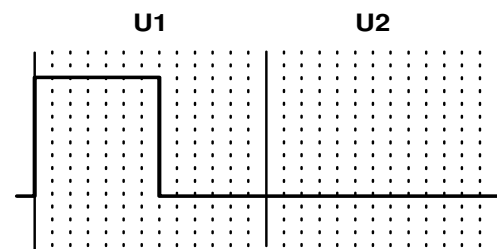
The following procedure describes how to enable and write data into the AWG to produce customized pulse shapes to be transmitted for a specific



E1 AWG Example



DSX-1 (54% duty cycle) AWG Example



DSX-1 (50% duty cycle) AWG Example

Figure 14. Arbitrary Waveform UI

channel or channels. To enable the AWG function for a specific channel or channels the corresponding bit(s) in the **AWG Enable Register (19h)** (See Section 14.26 on page 40) must be set to “1”. When the corresponding bit(s) in the AWG Enable Register are set to “0” pre-programmed pulse shapes are selected for transmission.

In order to access and write data for a customized pulse shape to a specific channel or channels, the following steps are required. First the desired channel and phase sample addresses must be written to the **AWG Phase Data Register (18h)** (See Section 14.25 on page 40). Once the channel and phase sample address have been selected, the actual phase sample data may be entered into the AWG Phase Data Register at the selected phase sample address selected by the lower five bits of the **AWG Phase Address Register (17h)** (See Section 14.24 on page 40)).

To change the phase sample address of the selected channel the user may use either of the following steps. First, the user can re-write the phase sample address to the AWG Phase Address Register or set the Auto-Increment bit (Bit 7) in the **Global Control Register (0Fh)** (See Section 14.16 on page 38)) to “1”. When this bit is set to “1” only the first phase sample address (00000 binary) needs to be written to the **AWG Phase Address Register (17h)** (See Section 14.24 on page 40), and each subsequent access (read or write) to the **AWG Phase Data Register (18h)** (See Section 14.25 on page 40) will automatically increment the phase sample address. The channel address, however, remains unaffected by the Auto-Increment mode. Since the number of phase samples forming the customized pulse shape varies with the mode of operation (E1/T1/J1), the **AWG Phase Address Register (17h)** (See Section 14.24 on page 40) needs to be re-written in order to re-start the phase sample address sequence from zero.

The AWG Broadcast function allows the same data to be written to different channels simultaneously. This is done with the use of the **AWG Broadcast Register (16h)** (See Section 14.23 on page 40)), each bit in the AWG Broadcast Register corresponds to a different channel (bit 0 is channel 0, and bit 3 is channel 3 & etc.).

To write the same pulse shaping data to multiple channels, simple set the corresponding bit to “1” in the **AWG Broadcast Register (16h)** (See Section 14.23 on page 40). This function only requires that one of the eight channel addresses be written to the **AWG Phase Address Register (17h)** (See Section 14.24 on page 40). During an AWG read sequence, the bits in the AWG Broadcast Register are ignored. During an AWG write sequence, the selected channel or channels are specified by both the channel address specified by the upper bits of the **AWG Phase Address Register (17h)** (See Section 14.24 on page 40) and the selected channel or channels in the **AWG Broadcast Register (16h)** (See Section 14.23 on page 40).

During a multiple channel write the first channel that is written to, is the channel that was address by the AWG Phase Address Register. This channel’s bit in the AWG Broadcast Register can be set to either “1” or “0”. For a more descriptive explanation of how to use the AWG refer to the “How To Use The CS61880/CS61884 Arbitrary Waveform Generator” application note AN204.

16. JTAG SUPPORT

The CS61884 supports the IEEE Boundary Scan Specification as described in the IEEE 1149.1 standards. A Test Access Port (TAP) is provided that consists of the TAP controller, the instruction register (IR), by-pass register (BPR), device ID register (IDR), the boundary scan register (BSR), and the 5 standard pins ($\overline{\text{TRST}}$, TCK, TMS, TDI, and TDO). A block diagram of the test access port is shown in Figure 15. The test clock input (TCK) is used to sample input data on TDI, and shift output data through TDO. The TMS input is used to step the TAP controller through its various states.

The instruction register is used to select test execution or register access. The by-pass register provides a direct connection between the TDI input and the TDO output. The device identification register contains an 32-bit device identifier.

The Boundary Scan Register is used to support testing of IC inter-connectivity. Using the Boundary Scan Register, the digital input pins can be sampled

and shifted out on TDO. In addition, this register can also be used to drive digital output pins to a user defined state.

16.1 TAP Controller

The TAP Controller is a 16 state synchronous state machine clocked by the rising edge of TCK. The TMS input governs state transitions as shown in Figure 16. The value shown next to each state transition in the diagram is the value that must be on TMS when it is sampled by the rising edge of TCK.

16.1.1 JTAG Reset

TRST resets all JTAG circuitry.

16.1.2 Test-Logic-Reset

The test-logic-reset state is used to disable the test logic when the part is in normal mode of operation. This state is entered by asynchronously asserting $\overline{\text{TRST}}$ or forcing TMS High for 5 TCK periods.

16.1.3 Run-Test-Idle

The run-test-idle state is used to run tests.

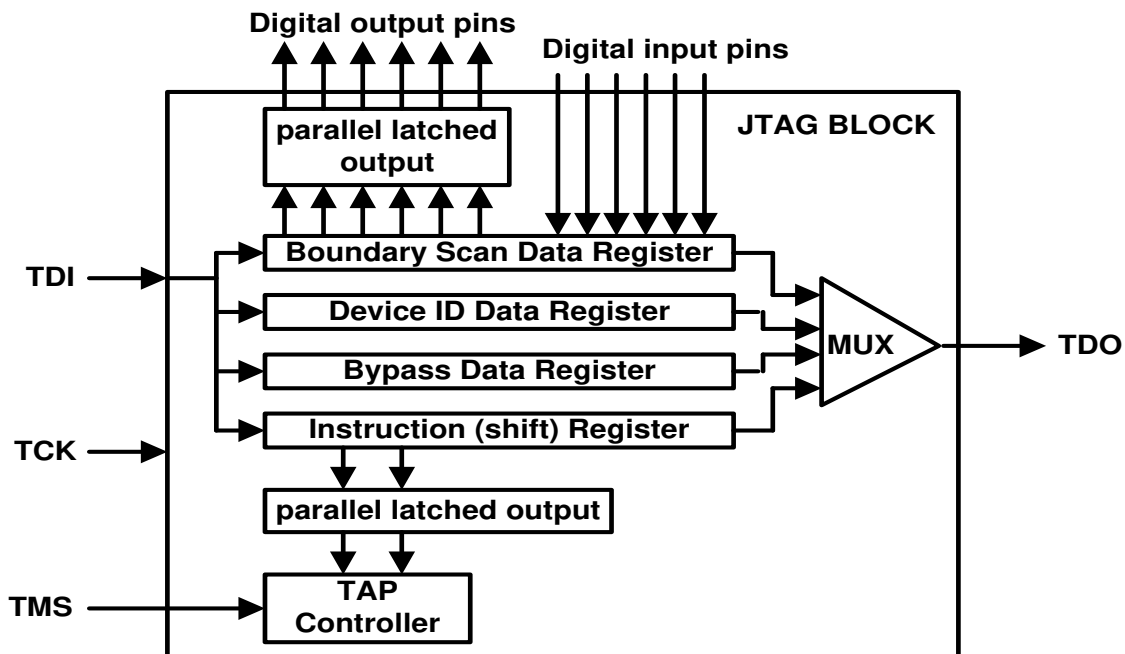


Figure 15. Test Access Port Architecture

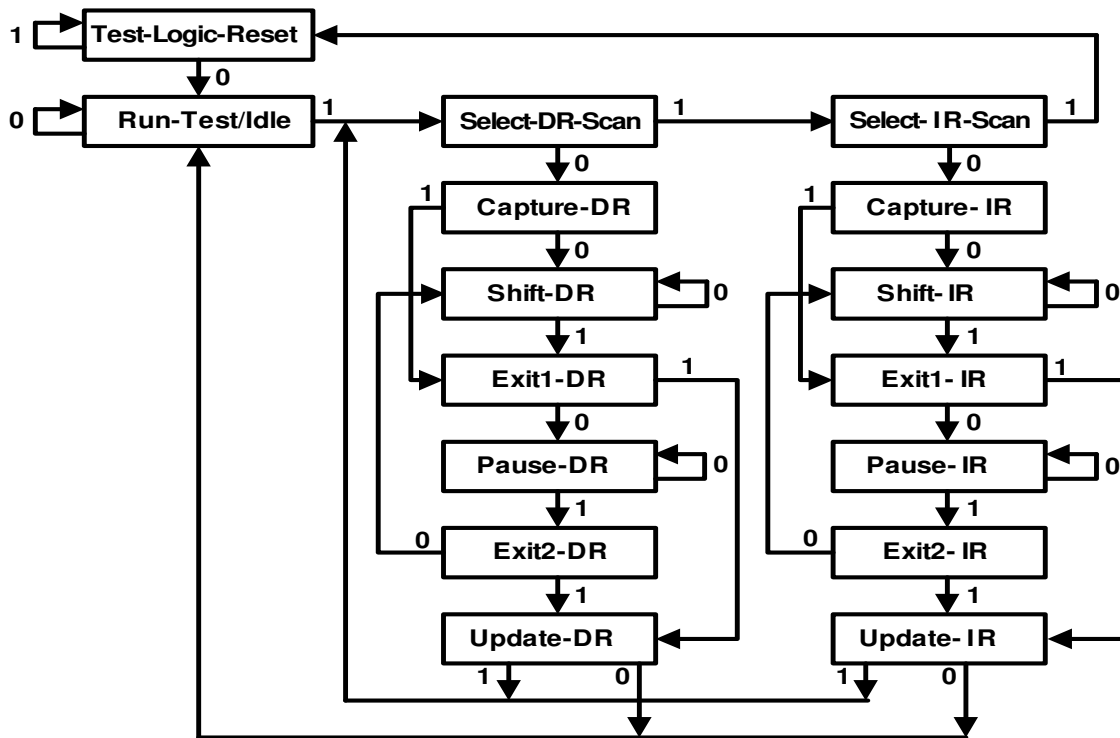


Figure 16. TAP Controller State Diagram

16.1.4 *Select-DR-Scan*

This is a temporary controller state.

16.1.5 *Capture-DR*

In this state, the Boundary Scan Register captures input pin data if the current instruction is EXTEST or SAMPLE/PRELOAD.

16.1.6 *Shift-DR*

In this controller state, the active test data register connected between TDI and TDO, as determined by the current instruction, shifts data out on TDO on each rising edge of TCK.

16.1.7 *Exit1-DR*

This is a temporary state. The test data register selected by the current instruction retains its previous value.

16.1.8 *Pause-DR*

The pause state allows the test controller to temporarily halt the shifting of data through the current test data register.

16.1.9 *Exit2-DR*

This is a temporary state. The test data register selected by the current instruction retains its previous value.

16.1.10 *Update-DR*

The Boundary Scan Register is provided with a latched parallel output to prevent changes while data is shifted in response to the EXTEST and SAMPLE/PRELOAD instructions. When the TAP controller is in this state and the Boundary Scan Register is selected, data is latched into the parallel output of this register from the shift-register path on the falling edge of TCK. The data held at the latched parallel output changes only in this state.

16.1.11 Select-IR-Scan

This is a temporary controller state. The test data register selected by the current instruction retains its previous state.

16.1.12 Capture-IR

In this controller state, the instruction register is loaded with a fixed value of “01” on the rising edge of TCK. This supports fault-isolation of the board-level serial test data path.

16.1.13 Shift-IR

In this state, the shift register contained in the instruction register is connected between TDI and TDO and shifts data one stage towards its serial output on each rising edge of TCK.

16.1.14 Exit1-IR

This is a temporary state. The test data register selected by the current instruction retains its previous value.

16.1.15 Pause-IR

The pause state allows the test controller to temporarily halt the shifting of data through the instruction register.

16.1.16 Exit2-IR

This is a temporary state. The test data register selected by the current instruction retains its previous value.

16.1.17 Update-IR

The instruction shifted into the instruction register is latched into the parallel output from the shift-register path on the falling edge of TCK. When the new instruction has been latched, it becomes the current instruction. The test data registers selected

by the current instruction retain their previous value.

16.2 Instruction Register (IR)

The 3-bit Instruction register selects the test to be performed and/or the data register to be accessed. The valid instructions are shifted in LSB first and are listed in [Table 10](#):

Table 10. JTAG Instructions

| IR CODE | INSTRUCTION |
|---------|----------------|
| 000 | EXTEST |
| 100 | SAMPLE/PRELOAD |
| 110 | IDCODE |
| 111 | BYPASS |

16.2.1 EXTEST

The EXTEST instruction allows testing of off-chip circuitry and board-level interconnect. EXTEST connects the BSR to the TDI and TDO pins.

16.2.2 SAMPLE/PRELOAD

The SAMPLE/PRELOAD instruction samples all device inputs and outputs. This instruction places the BSR between the TDI and TDO pins. The BSR is loaded with samples of the I/O pins by the Capture-DR state.

16.2.3 IDCODE

The IDCODE instruction connects the device identification register to the TDO pin. The device identification code can then be shifted out TDO using the Shift-DR state.

16.2.4 BYPASS

The BYPASS instruction connects a one TCK delay register between TDI and TDO. The instruction is used to bypass the device.

16.3 Device ID Register (IDR)

Revision section: 0h = Rev A, 1h = Rev B and so on. The device Identification Code [27 - 12] is derived from the last three digits of the part number (884). The LSB is a constant 1, as defined by IEEE 1149.1.

| CS61884 IDCODE REGISTER(IDR) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|------------------------------|----|----|----|------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|-------------------|----|----|----|---|----|---|---|----|---|---|---|---|---|
| REVISION | | | | DEVICE IDCODE REGISTER | | | | | | | | | | | | | | MANUFACTURER CODE | | | | | | | | | | | | | |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0h | | | | 0h | | | | 8h | | | | 8h | | | | 4h | | | | 0h | | | 0h | | | 9h | | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 |

17. BOUNDARY SCAN REGISTER (BSR)

The BSR is a shift register that provides access to the digital I/O pins. The BSR is used to read and write the device pins to verify interchip connectivity. Each pin has a corresponding scan cell in the register. The pin to scan cell mapping is given in the BSR description shown in [Table 11](#).

NOTE: Data is shifted LSB first into the BSR register.

Table 11. Boundary Scan Register

| BSR Bit | Pin Name | Cell Type | Bit Symbol |
|---------|----------|-----------|------------|
| 0 | LOS7 | O | LOS7 |
| 1 | RNEG7 | O | RNEG7 |
| 2 | RPOS7 | O | RPOS7 |
| 3 | RCLK7 | O | RCLK7 |
| 4 | - | Note 2 | HIZ7_B |
| 5 | TNEG7 | I | TNEG7 |
| 6 | TPOS7 | I | TPOS7 |
| 7 | TCLK7 | I | TCLK7 |
| 8 | LOS6 | O | LOS6_B |
| 9 | RNEG6 | O | RNEG6 |
| 10 | RPOS6 | O | RPOS6 |
| 11 | RCLK6 | O | RCLK6 |
| 12 | - | Note 2 | HIZ6_B |
| 13 | TNEG6 | I | TNEG6 |
| 14 | TPOS6 | I | TPOS6 |
| 15 | TCLK6 | I | TCLK6 |
| 16 | MCLK | I | MCLK |
| 17 | MODE | I | MODE_TRI |
| 18 | MODE | I | MODE_IN |
| 19 | ADDR4 | I | ADDR4 |
| 20 | ADDR3 | I | ADDR3 |
| 21 | ADDR2 | I | ADDR2 |
| 22 | ADDR1 | I | ADDR1 |
| 23 | ADDR0 | I | ADDR0 |
| 24 | LOOP0/D0 | I | LPT0 |
| 25 | LOOP0/D0 | I | LPI0 |
| 26 | LOOP0/D0 | O | LPO0 |
| 27 | LOOP1/D1 | I | LPT1 |

Table 11. Boundary Scan Register (Continued)

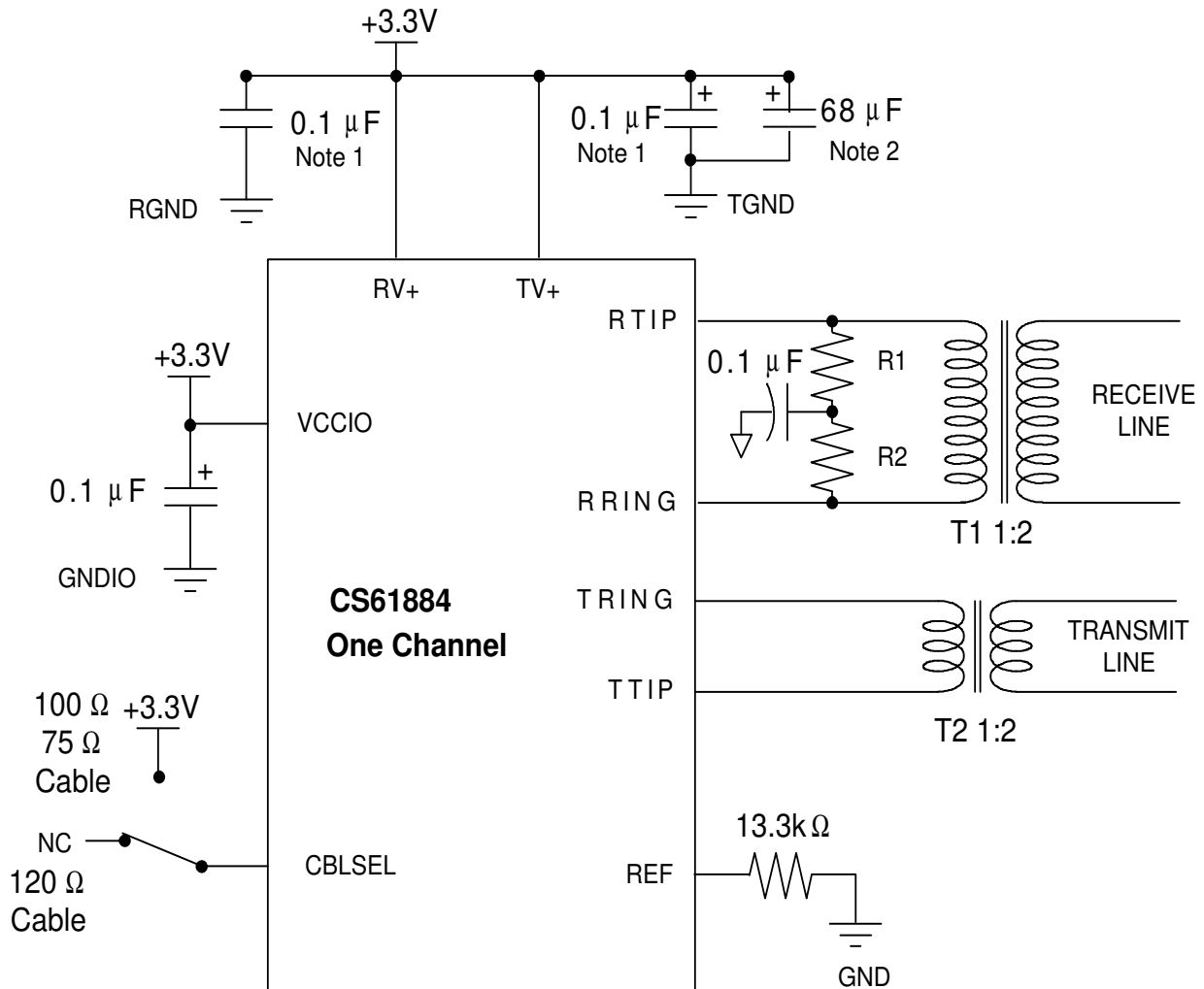
| BSR Bit | Pin Name | Cell Type | Bit Symbol |
|----------------|-----------------|------------------|-------------------|
| 28 | LOOP1/D1 | I | LPI1 |
| 29 | LOOP1/D1 | O | LPO1 |
| 30 | LOOP2/D2 | I | LPT2 |
| 31 | LOOP2/D2 | I | LPI2 |
| 32 | LOOP2/D2 | O | LPO2 |
| 33 | LOOP3/D3 | I | LPT3 |
| 34 | LOOP3/D3 | I | LPI3 |
| 35 | LOOP3/D3 | O | LPO3 |
| 36 | LOOP4/D4 | I | LPT4 |
| 37 | LOOP4/D4 | I | LPI4 |
| 38 | LOOP4/D4 | O | LPO4 |
| 39 | LOOP5/D5 | I | LPT5 |
| 40 | LOOP5/D5 | I | LPI5 |
| 41 | LOOP5/D5 | O | LPO5 |
| 42 | LOOP6/D6 | I | LPT6 |
| 43 | LOOP6/D6 | I | LPI6 |
| 44 | LOOP6/D6 | O | LPO6 |
| 45 | LOOP7/D7 | I | LPT7 |
| 46 | LOOP7/D7 | I | LPI7 |
| 47 | LOOP7/D7 | O | LPO7 |
| 48 | - | Note 1 | LPOEN |
| 49 | TCLK1 | I | TCLK1 |
| 50 | TPOS1 | I | TPOS1 |
| 51 | TNEG1 | I | TNEG1 |
| 52 | RCLK1 | O | RCLK1 |
| 53 | RPOS1 | O | RPOS1 |
| 54 | RNEG1 | O | RNEG1 |
| 55 | - | Note 2 | HIZ1_B |
| 56 | LOS1 | O | LOS1 |
| 57 | TCLK0 | I | TCLK0 |
| 58 | TPOS0 | I | TPOS0 |
| 59 | TNEG0 | I | TNEG0 |
| 60 | RCLK0 | O | RCLK0 |
| 61 | RPOS0 | O | RPOS0 |
| 62 | RNEG0 | O | RNEG0 |
| 63 | - | Note 2 | HIZ0_B |
| 64 | LOS0 | O | LOS0 |
| 65 | MUX | I | MUX |
| 66 | LOS3 | O | LOS3 |
| 67 | RNEG3 | O | RNEG3 |
| 68 | RPOS3 | O | RPOS3 |
| 69 | RCLK3 | O | RCLK3 |
| 70 | - | Note 2 | HIZ3_B |
| 71 | TNEG3 | I | TNEG3 |
| 72 | TPOS3 | I | TPOS3 |

Table 11. Boundary Scan Register (Continued)

| BSR Bit | Pin Name | Cell Type | Bit Symbol |
|----------------|-----------------|------------------|-------------------|
| 73 | TCLK3 | I | TCLK3 |
| 74 | LOS2 | O | LOS2 |
| 75 | RNEG2 | O | RNEG2 |
| 76 | RPOS2 | O | RPOS2 |
| 77 | RCLK2 | O | RCLK2 |
| 78 | - | Note 2 | HIZ2_B |
| 79 | TNEG2 | I | TNEG2 |
| 80 | TPOS2 | I | TPOS2 |
| 81 | TCLK2 | I | TCLK2 |
| 82 | INT_B | O | INT_B |
| 83 | RDY | O | RDYOUT |
| 84 | - | Note 3 | RDYOEN |
| 85 | WR_B | I | WR_B |
| 86 | RD_B | I | RD_B |
| 87 | ALE | I | ALE |
| 88 | CS_B | I | CS_B |
| 89 | CS_B | I | CS_B_TRI |
| 90 | INTL | I | INTL |
| 91 | CBLSEL | I | CBLSEL_TRI |
| 92 | CBLSEL | I | CBLSEL_IN |
| 93 | TCLK5 | I | TCLK5 |
| 94 | TPOS5 | I | TPOS5 |
| 95 | TNEG5 | I | TNEG5 |
| 96 | RCLK5 | O | RCLK5 |
| 97 | RPOS5 | O | RPOS5 |
| 98 | RNEG5 | O | RNEG5 |
| 99 | - | Note 2 | HIZ5_B |
| 100 | LOS5 | O | LOS5 |
| 101 | TCLK4 | I | TCLK4 |
| 102 | TPOS4 | I | TPOS4 |
| 103 | TNEG4 | I | TNEG4 |
| 104 | RCLK4 | O | RCLK4 |
| 105 | RPOS4 | O | RPOS4 |
| 106 | RNEG4 | O | RNEG4 |
| 107 | - | Note 2 | HIZ4_B |
| 108 | LOS4 | O | LOS4 |
| 109 | TXOE | I | TXOE |
| 110 | CLKE | I | CLKE |

Notes:

- 1) LPOEN controls the LOOP[7:0] pins. Setting LPOEN to “1” configures LOOP[7:0] as outputs. The output value driven on the pins are determined by the values written to LPO[7:0]. Setting LPOEN to “0” High-Z all the pins. In this mode, the input values driven to these LOOP[7:0] can be read via LPI[7:0].
- 2) HIZ_B controls the RPOSx, RNEGx, and RCLKx pins. When HIZ_B is High, the outputs are enabled; when HIZ_B is Low, the outputs are placed in a high impedance state (High-Z).
- 3) RDYOEN controls the ACK_B pin. Setting RDYOEN to “1” enables output on ACK_B. Setting ACKEN to “0” High - Z the ACK_B pin.

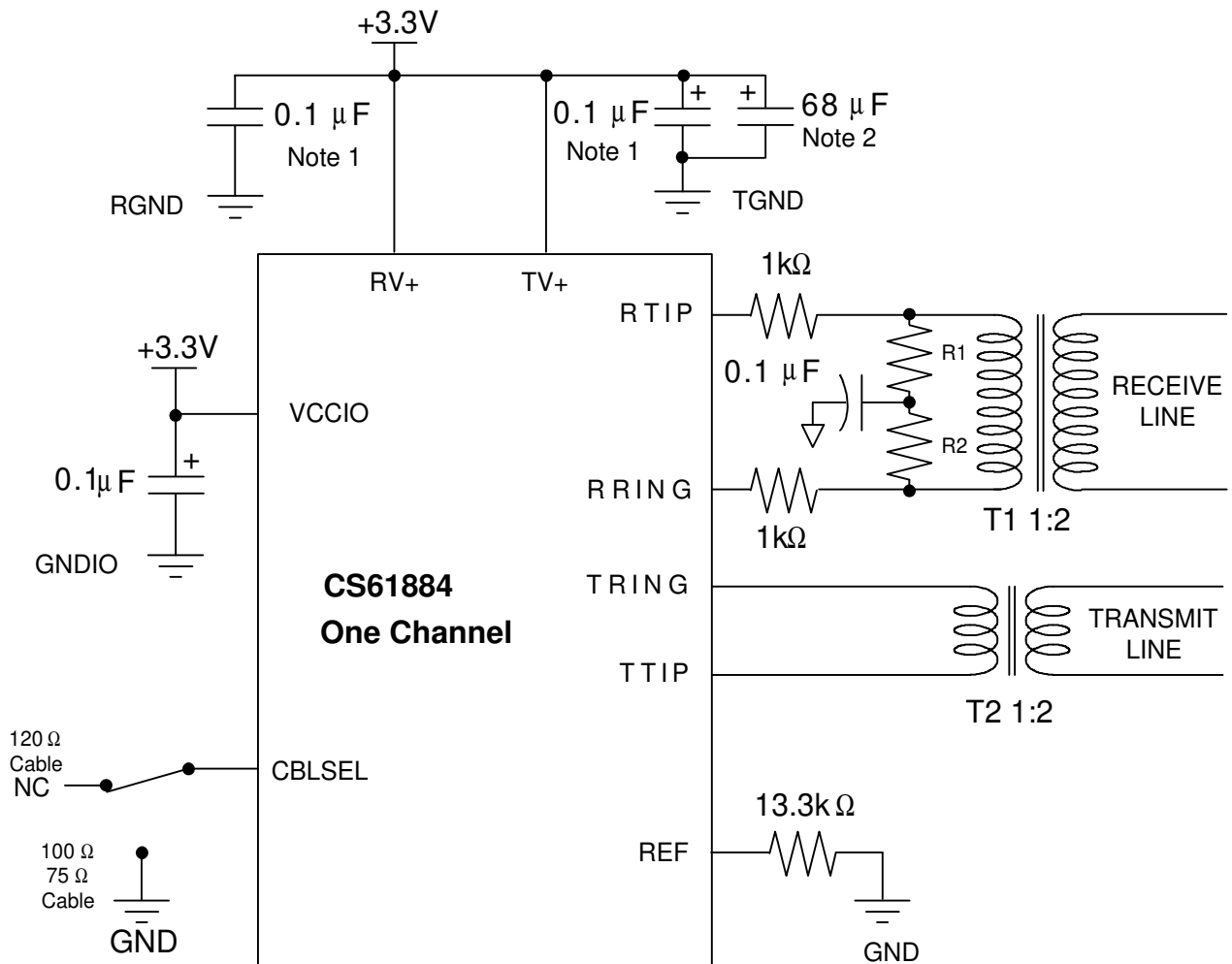
18. APPLICATIONS


| Component | T1/J1 100Ω Twisted Pair Cable | E1 75Ω Coaxial Cable | E1 120Ω Twisted Pair Cable |
|-----------|-------------------------------|----------------------|----------------------------|
| R1 (Ω) | 15 | 15 | 15 |
| R2 (Ω) | 15 | 15 | 15 |

Notes:1) Required Capacitor between each TV+, RV+, VCCIO and TGND, RGND, GNDIO respectively.

2) Common decoupling capacitor for all TVCC and TGND pins.

Figure 17. Internal RX/TX Impedance Matching



| Component | T1/J1 100Ω Twisted Pair Cable | E1 75Ω Coaxial Cable | E1 120Ω Twisted Pair Cable |
|-----------|-------------------------------|----------------------|----------------------------|
| R1 (Ω) | 12.5 | 9.31 | 15 |
| R2 (Ω) | 12.5 | 9.31 | 15 |

Notes: 1) Required Capacitor between each TV+, RV+, VCCIO and TGND, RGND, GNDIO respectively.

2) Common decoupling capacitor for all TVCC and TGND pins.

Figure 18. Internal TX, External RX Impedance Matching

18.1 Transformer specifications

Recommended transformer specifications are shown in [Table 12](#). Any transformer used with the CS61884 should meet or exceed these specifications.

Table 12. Transformer Specifications

| Descriptions | Specifications |
|------------------------------|--------------------------------|
| Turns Ratio Receive/Transmit | 1:2 |
| Primary Inductance | 1.5mH min. @ 772 kHz |
| Primary Leakage Inductance | 0.3 μ H max @ 772 kHz |
| Secondary leakage Inductance | 0.4 μ H max @ 772 kHz |
| Inter winding Capacitance | 18pF max, primary to secondary |
| ET-Constant | 16V - μ s min. |

18.2 Crystal Oscillator Specifications

When a reference clock signal is not available, a CMOS crystal oscillator may be used as the reference clock signal. The oscillator must have a mini-

imum symmetry of 40-60% and minimum stability of ± 100 ppm for both E1 and T1/J1 applications.

18.3 Designing for AT&T 62411

For information on requirements of the AT&T 62411 and the design of the appropriate system synchronizer, refer to Application Note AN012 “AT&T 62411 Design Considerations - Jitter and Synchronization” and Application Note AN011 “Jitter Testing Procedures for Compliance with AT&T 62411”.

18.4 Line Protection

Secondary protection components can be added to the line interface circuitry to provide lightning surge and AC power-cross immunity. For additional information on the different electrical safety standards and specific applications circuit recommendations, refer to Application Note AN034 “Secondary Line Protection for T1 and E1 Cards”.

19. CHARACTERISTICS AND SPECIFICATIONS

19.1 Absolute Maximum Ratings

CAUTION: Operations at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

| Parameter | Symbol | Min. | Max | Units | |
|---|------------------|-----------------|------------|--------|----|
| DC Supply (referenced to RGND = TGND = 0V) | RV+ TV+ | - - | 4.0 4.0 | V V | |
| DC Supply | VCCIO | -0.5 | 4.6 | V | |
| Input Voltage, Any Digital Pin except CBLSEL, MODE and LOOP(n) pins (referenced to GNDIO = 0V) | V _{IH} | GNDIO -0.5 | 5.3 | V | |
| Input Voltage CBLSEL, MODE & LOOP(n) Pins (referenced to GNDIO = 0V) | V _{IH} | GNDIO -0.5 | VCCIO +0.5 | V | |
| Input voltage, RTIP and RRING Pins | | TGND -0.5 | TV+ +0.5 | V | |
| ESD voltage, Any pin | Note 1 | 2k | - | V | |
| Input current, Any Pin | Note 2 | I _{IH} | -10 | +10 | mA |
| Maximum Power Dissipation, In package | P _p | - | 1.73 | W | |
| Ambient Operating Temperature | T _A | -40 | 85 | C | |
| Storage Temperature | T _{stg} | -65 | 150 | C | |

19.2 Recommended Operating Conditions

| Parameter | Symbol | Min. | Typ | Max | Units | |
|--|----------------|-------|-----|-------|-------|----|
| DC Supply | RV+, TV+ | 3.135 | 3.3 | 3.465 | V | |
| DC Supply | VCCIO | 3.135 | 3.3 | 3.465 | V | |
| Ambient operating Temperature | T _A | -40 | 25 | 85 | C | |
| Power Consumption, T1/J1 Mode, 100 Ω line load | Notes 3, 4, 5 | - | - | 970 | 1900 | mW |
| Power Consumption, E1 Mode, 75 Ω line load | Notes 3, 4, 5 | - | - | 810 | 1400 | mW |
| Power Consumption, E1 Mode, 120 Ω line load | Notes 3, 4, 5 | - | - | 750 | 1300 | mW |

- Notes:
- Human Body Model
 - Transient current of up to 100 mA will not cause SCR latch-up. Also TTIP, TRING, TV+ and TGND can withstand a continuous current of 100 mA.
 - Power consumption while driving line load over the full operating temperature and power supply voltage range. Includes all IC channels and loads. Digital inputs are within 10% of the supply rails and digital outputs are driving a 50pF capacitive load.
 - Typical consumption corresponds to 50% ones density for E1/T1/J1 modes and medium line length setting for T1/J1 mode at 3.3Volts.
 - Maximum consumption corresponds to 100% ones density for E1/T1/J1 modes and maximum line length settings for T1/J1 mode at 3.465Volts.
 - This specification guarantees TTL compatibility (V_{OH} = 2.4 V @ I_{OUT} = -400 μA).
 - Output drivers are TTL compatible.
 - Pulse amplitude measured at the output of the transformer across a 75 Ω load.
 - Pulse amplitude measured at the output of the transformer across a 120 Ω load.
 - Pulse amplitude measured at the output of the transformer across a 100 Ω load for all line length settings.

19.3 Digital Characteristics

(TA = -40°C to 85°C; TV+, RV+ = 3.3 V ±5%; GND = 0 V)

| Parameter | Symbol | Min. | Typ | Max | Units |
|---|------------------|----------------|-----------|---------------|-------|
| High-Level Input Voltage Note 6 | V _{IH} | 2.0 | - | - | V |
| Low-Level Input Voltage Note 6 | V _{IL} | - | - | 0.8 | V |
| LOOP[7:0] Low-Level Input Voltage | V _{IHL} | - | - | 1/3 VCCIO-0.2 | V |
| LOOP[7:0] Mid-Level Input Voltage | V _{IHM} | 1/3 VCCIO +0.2 | 1/2 VCCIO | 2/3 VCCIO-0.2 | V |
| LOOP[7:0] High-Level Input Voltage | V _{IHH} | 2/3 VCCIO +0.2 | - | - | V |
| High-Level Output Voltage I _{OUT} = -400 μA Notes 6, 7 | V _{OH} | 2.4 | - | - | V |
| Low-Level Output Voltage I _{OUT} = 1.6 mA Notes 6, 7 | V _{OL} | - | - | 0.4 | V |
| Input Leakage Current | | -10 | - | +10 | μA |
| Input leakage for LOOP pins | | -150 | - | +150 | μA |

19.4 Transmitter Analog Characteristics

(TA = -40°C to 85°C; TV+, RV+ = 3.3 V ±5%; GND = 0 V)

| Parameter | Min. | Typ | Max | Units | |
|---|---|--------|-------|-------|--------|
| Output Pulse Amplitudes Notes 8, 9, 10 | E1 75Ω | 2.14 | 2.37 | 2.6 | V |
| | E1 120Ω | 2.7 | 3.0 | 3.3 | V |
| | T1/J1 100Ω | 2.4 | 3.0 | 3.6 | V |
| Ratio of Positive to Negative pulses Notes 8, 9, 10 | T1/J1 100 Ω | 0.95 | - | 1.05 | |
| | E1, amplitude at center of pulse interval | 0.95 | - | 1.05 | |
| | E1, width at 50% of nominal amplitude | 0.95 | - | 1.05 | |
| Pulse Amplitude of a space | T1/J1 100 Ω | -0.15 | - | 0.15 | V |
| | E1 120 Ω | -0.3 | - | 0.3 | V |
| | E1 75 Ω | -0.237 | - | 0.237 | V |
| Power in 2 kHz band about 772 kHz Notes 11, 12 | (T1/J1 100 Ω only) | 12.6 | - | - | dBm |
| Power in 2 kHz band about 1.544 MHz (referenced to power in 2 kHz band at 772 kHz, T1/J1 100 Ω only) | Notes 11, 12 | -29 | - | - | dBm |
| Transmit Return Loss - E1 Notes 11, 12, 13 | 51 kHz to 102 kHz | - 14 | - 20 | - | dB |
| | 102 kHz to 2048 kHz | - 14 | - 19 | - | |
| | 2048 kHz to 3072 kHz | - 14 | - 18 | - | |
| Transmit Return Loss - T1/J1 Notes 11, 12, 13 | 51 kHz to 102 kHz | - 14 | - 19 | - | dB |
| | 102 kHz to 2048 kHz | - 14 | - 19 | - | |
| | 2048 kHz to 3072 kHz | - 14 | - 18 | - | |
| Jitter Added by the Transmitter Notes 11, 14 | 10 Hz - 8 kHz | - | 0.010 | 0.020 | UI |
| | 8 kHz - 40 kHz | - | 0.009 | 0.025 | |
| | 10 Hz - 40 kHz | - | 0.007 | 0.025 | |
| | Broad Band | - | 0.015 | 0.050 | |
| Transmitter Short Circuit Current per channel | | - | - | 50 | mA RMS |

19.5 Receiver Analog Characteristics

(TA = -40°C to 85°C; TV+, RV+ = 3.3 V ±5%; GND = 0 V))

| Parameter | Min. | Typ | Max | Units | |
|--|---------------------|------|------|-------|-----------|
| Allowable Cable Attenuation @ 1024kHz and 772kHz | - | - | - 12 | dB | |
| RTIP/RRING Input Impedance (Internal Line matching mode) Note 11 | T1/J1 100 Ω Load | 140 | - | Ω | |
| | E1 120Ω Load | 14k | - | | |
| | E1 75Ω Load | 50 | - | | |
| RTIP/RRING Input Impedance (External Line matching mode) Note 11 | T1/J1 100 Ω Load | 14K | - | Ω | |
| | E1 120Ω Load | 14k | - | | |
| | E1 75Ω Load | 14K | - | | |
| Receiver Dynamic Range | 0.5 | - | - | Vp | |
| Signal to Noise margin (Per G.703, O151 @ 6dB cable Atten). Note 11 | - | - 18 | - | dB | |
| Receiver Squelch Level | - | 150 | - | mV | |
| LOS Threshold | - | 200 | - | mV | |
| LOS Hysteresis | - | 50 | - | mV | |
| Data Decision Threshold Note 11 | E1 Modes | 41 | 50 | 59 | % of peak |
| Data Decision Threshold Note 11 | T1/J1 Modes | 56 | 65 | 74 | % of peak |
| Input Jitter Tolerance - E1 Notes 11, 15, 17 | 1 Hz - 1.8 Hz | 18 | - | - | UI |
| | 20 Hz - 2.4 kHz | 1.5 | - | - | |
| | 18 kHz - 100 kHz | 0.2 | - | - | |
| Input Jitter Tolerance - T1/J1 Notes 11, 15, 17 | 0.1 Hz - 1 Hz | 138 | - | - | UI |
| | 4.9 Hz - 300 kHz | 28 | - | - | |
| | 10kHz - 100 kHz | 0.4 | - | - | |
| Input Return Loss - E1/T1/J1 Notes 11, 12, 13 | 51 kHz - 102 kHz | - 18 | - 28 | - | dB |
| | 102 kHz - 2048 kHz | - 18 | - 30 | - | |
| | 2048 kHz - 3072 kHz | - 18 | - 27 | - | |

- Notes: 11. Parameters guaranteed by design and characterization.
 12. Using components on the CDB61884 evaluation board in Internal Match Impedance Mode.
 13. Return loss = $20\log_{10} \text{ABS}((Z1 + Z0) / (Z1 - Z0))$ where Z1 - impedance of the transmitter or receiver, and Z0 = cable impedance.
 14. Assuming that jitter free clock is input to TCLK.
 15. Jitter tolerance for 0 dB for T1/J1 input signal levels and 6 dB for E1 input signal levels. Jitter tolerance increases at lower frequencies. HDB3/B8ZS coders enabled.
 16. In Data Recovery Mode.
 17. Jitter Attenuator in the receive path.

19.6 Jitter Attenuator Characteristics

(TA = -40°C to 85°C; TV+, RV+ = 3.3 V ±5%; GND = 0 V)

| Parameter | | Min. | Typ | Max | Units |
|---|-------------------|--------|------|------|-------|
| Jitter Attenuator Corner Frequency Note 11, 19 (Depends on JACF Bit in host mode) | T1/J1 Modes | - | 3.78 | - | Hz |
| | T1/J1 Modes | - | 7.56 | - | |
| | E1 Modes | - | 1.25 | - | |
| | E1 Modes | - | 2.50 | - | |
| E1 Jitter Attenuation Note 11, 18 | 3 Hz to 40 Hz | + 0.5 | - | - | dB |
| | 400 Hz to 100 kHz | - 19.5 | - | - | |
| T1/J1 Jitter Attenuation Note 11, 18 | 1 Hz to 20 Hz | 0 | - | - | dB |
| | 1 kHz | - 33.3 | - | - | |
| | 1.4KHz to 100KHz | - 40 | - | - | |
| Attenuator Input Jitter Tolerance before FIFO over flow and under flow Note 11 | 32-bit FIFO | - | 24 | - | UI |
| | 64-bit FIFO | - | 56 | - | UI |
| Delay through Jitter Attenuator Only Note 11 | 32-bit FIFO | - | 16 | - | UI |
| | 64-bit FIFO | - | 32 | - | UI |
| Intrinsic Jitter in Remote Loopback | Notes 11, 17 | - | - | 0.11 | UI |

Notes: 18. Attenuation measured with sinusoidal input filter equal to 3/4 of measured jitter tolerance. Circuit attenuates jitter at 20 dB/decade above the corner frequency. Output jitter can increase significantly when more than 28 UI's are input to the attenuator.

19. Measurement is not effected by the position of the Jitter Attenuator.

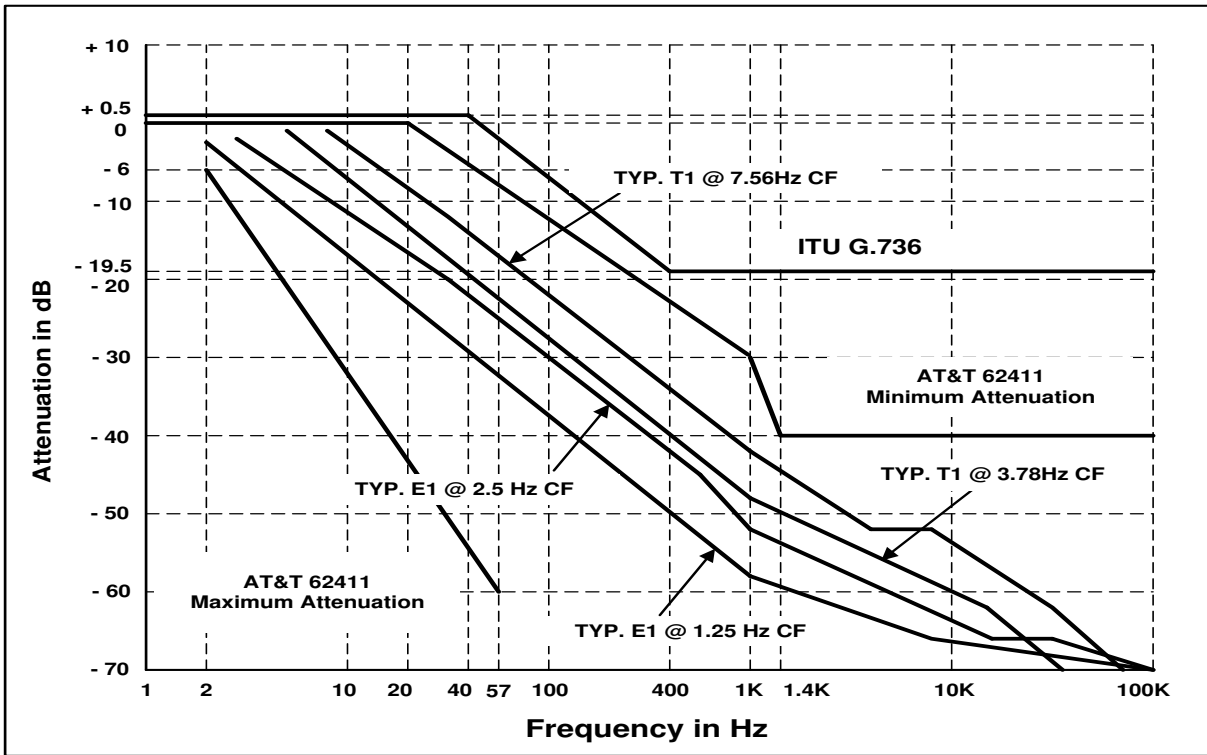


Figure 19. Jitter Transfer Characteristic vs. G.736, TBR 12/13 & AT&T 62411

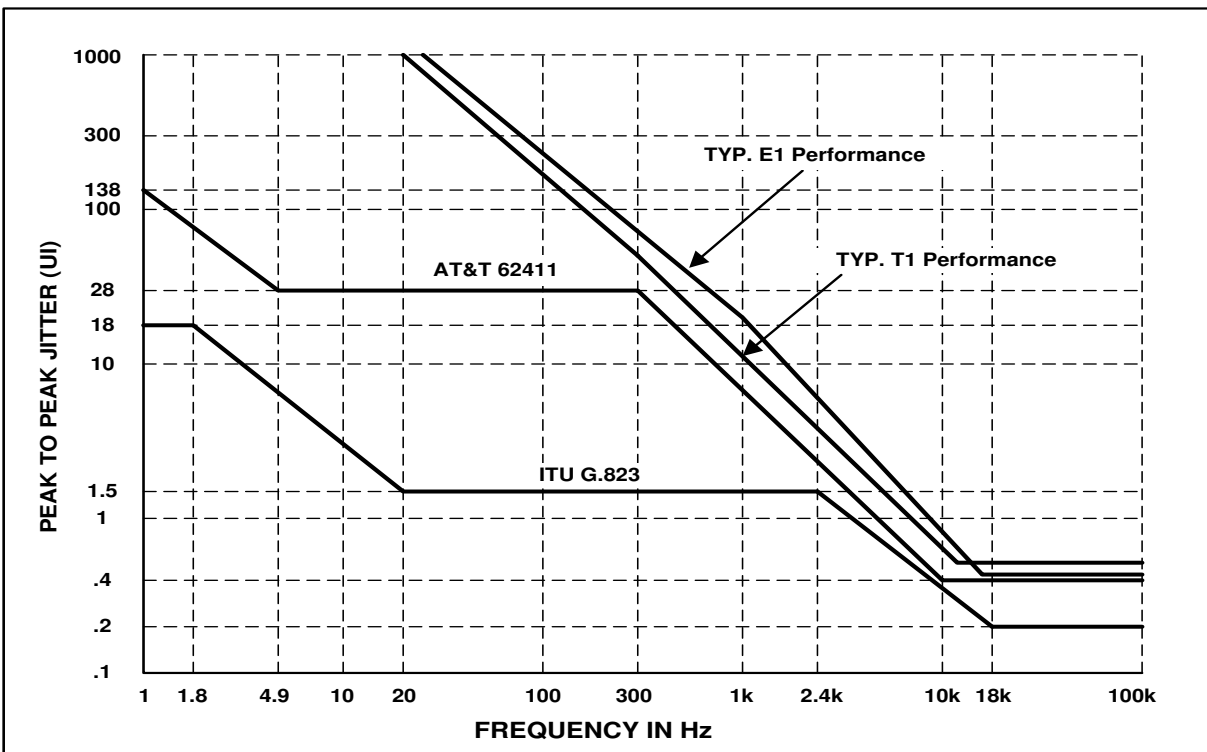


Figure 20. Jitter Tolerance Characteristic vs. G.823 & AT&T 62411

19.7 Master Clock Switching Characteristics

| Parameter | Symbol | Min. | Typ | Max | Units |
|------------------------------------|--------|------|-------|------|-------|
| MASTER CLOCK (MCLK) | | | | | |
| Master Clock Frequency E1 Modes | MCLK | | 2.048 | | MHz |
| Master Clock Frequency T1/J1 Modes | MCLK | | 1.544 | | MHz |
| Master Clock Tolerance | - | -100 | | +100 | ppm |
| Master Clock Duty Cycle | - | 40 | 50 | 60 | % |

19.8 Transmit Switching Characteristics

| Parameter | Symbol | Min. | Typ | Max | Units |
|---|--------------------|------|-------|-----|---------|
| E1 TCLK Frequency | $1/t_{pw2}$ | - | 2.048 | - | MHz |
| E1 TPOS/TNEG Pulse Width (RZ Mode) | | 236 | 244 | 252 | nS |
| T1/J1 TCLK Frequency | $1/t_{pw2}$ | - | 1.544 | - | MHz |
| TCLK Tolerance (NRZ Mode) | | -50 | - | 50 | PPM |
| TCLK Duty Cycle | t_{pwh2}/t_{pw2} | - | - | 90 | % |
| TCLK Pulse Width | | 20 | - | - | nS |
| TCLK Burst Rate Note 22 | | - | - | 20 | MHz |
| TPOS/TNEG to TCLK Falling Setup Time (NRZ Mode) | t_{su2} | 25 | - | - | nS |
| TCLK Falling to TPOS/TNEG Hold time (NRZ Mode) | t_{h2} | 25 | - | - | nS |
| TXOE Asserted Low to TX Driver HIGH-Z | | - | - | 1 | μ S |
| TCLK Held Low to Driver HIGH-Z Note 21 | | 8 | 12 | 20 | μ S |

19.9 Receive Switching Characteristics

* All parameters guaranteed by production, characterization or design.

| Parameter | Symbol | Min. | Typ | Max | Units |
|---|------------|------|-----|-----|-------|
| RCLK Duty Cycle | | 40 | 50 | 60 | % |
| E1 RCLK Pulse Width | | 196 | 244 | 328 | nS |
| E1 RPOS/RNEG Pulse Width (RZ Mode) | | 200 | 244 | 300 | nS |
| E1 RPOS/RNEG to RCLK rising setup time | t_{su} | 150 | 244 | - | nS |
| E1 RPOS/RNEG to RCLK hold time | t_h | 200 | 244 | - | nS |
| T1/J1 RCLK Pulse Width | | 259 | 324 | 388 | nS |
| T1/J1 RPOS/RNEG Pulse Width (RZ Mode) | | 250 | 324 | 400 | nS |
| T1/J1 POS/RNEG to RCLK rising setup time | t_{su} | 150 | 324 | - | nS |
| T1/J1 RPOS/RNEG to RCLK hold time | t_h | 200 | 324 | - | nS |
| RPOS/RNEG Output to RCLK Output (RZ Mode) | | - | - | 10 | nS |
| Rise/Fall Time, RPOS, RNEG, RCLK, LOS outputs | t_r, t_f | - | - | 85 | nS |

Notes: 20. Output load capacitance = 50pF.

21. MCLK is not active.

22. Parameters guaranteed by design and characterization.

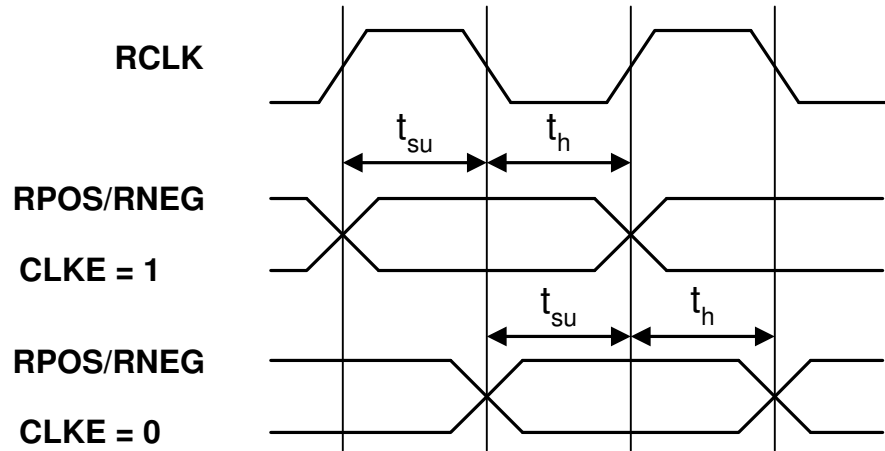


Figure 21. Recovered Clock and Data Switching Characteristics

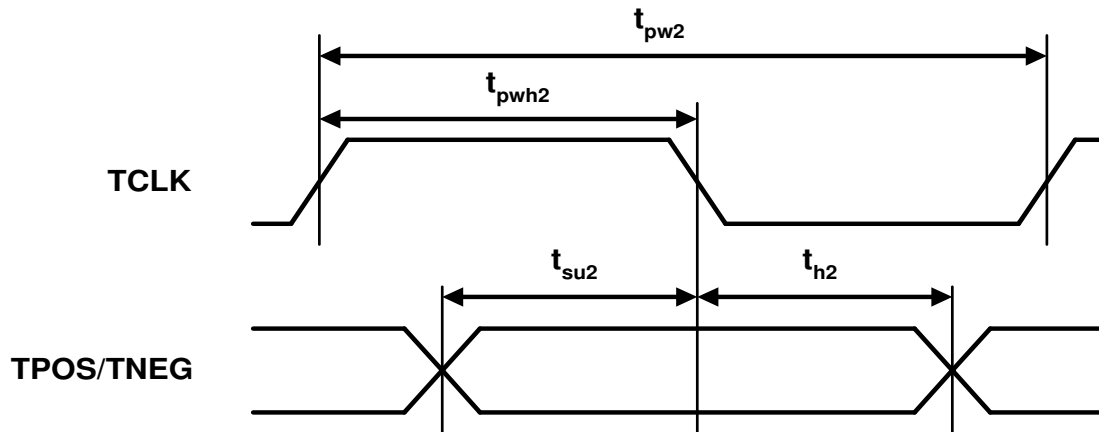


Figure 22. Transmit Clock and Data Switching Characteristics

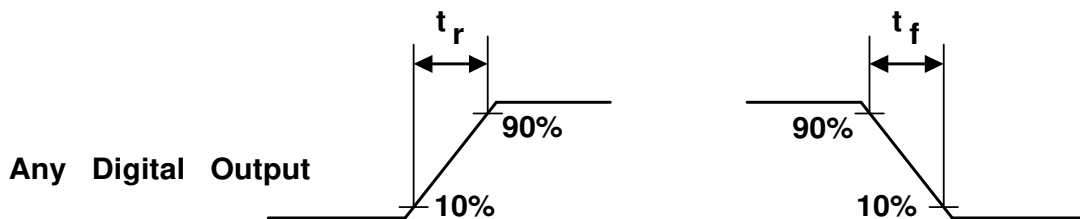


Figure 23. Signal Rise and Fall Characteristics

19.10 Switching Characteristics - Serial Port

| Parameter | Symbol | Min. | Typ. | Max | Unit |
|------------------------------------|----------------------|------|------|-----|------|
| SDI to SCLK Setup Time | t_{dc} | - | 20 | - | ns |
| SCLK to SDI Hold Time | t_{cdh} | - | 20 | - | ns |
| SCLK Low Time | t_{cl} | - | 50 | - | ns |
| SCLK High Time | t_{ch} | - | 50 | - | ns |
| SCLK Rise and Fall Time | t_r, t_f | - | 15 | - | ns |
| \overline{CS} to SCLK Setup Time | t_{cc} | - | 20 | - | ns |
| SCLK to \overline{CS} Hold Time | Note 23 t_{cch} | - | 20 | - | ns |
| \overline{CS} Inactive Time | t_{cwh} | - | 70 | - | ns |
| SDO Valid to SCLK | Note 23 t_{cdv} | - | 60 | - | ns |
| \overline{CS} to SDO High Z | t_{cdz} | - | 50 | - | ns |

Notes: 23. If SPOL = 0, then \overline{CS} should return high no sooner than 20 ns after the 16th rising edge of SCLK during a serial port read.

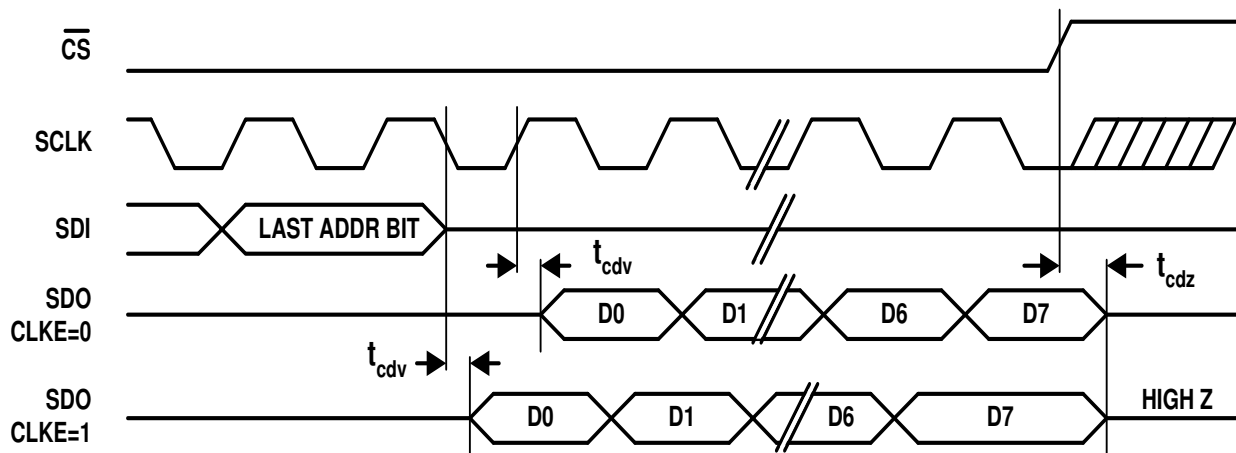


Figure 24. Serial Port Read Timing Diagram

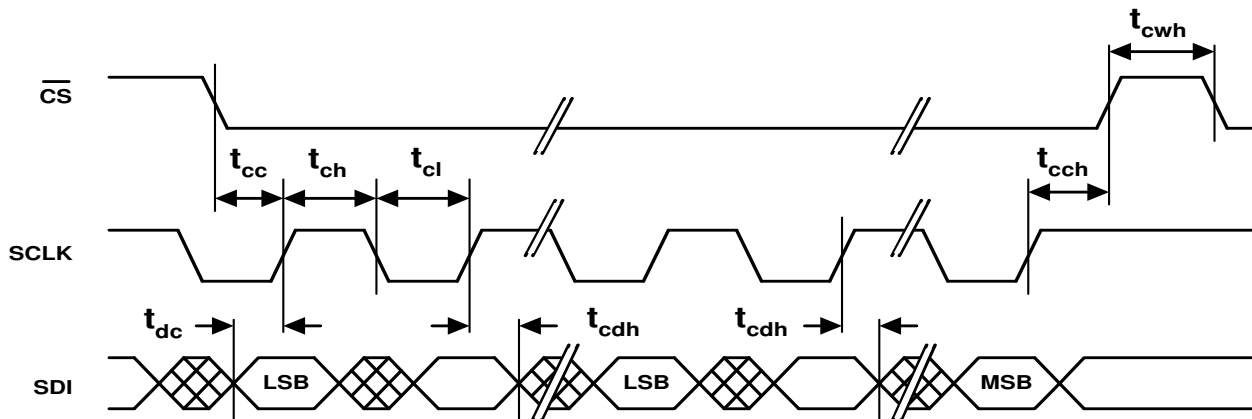


Figure 25. Serial Port Write Timing Diagram

19.11 Switching Characteristics - Parallel Port (Multiplexed Mode)

* All parameters guaranteed by production, characterization or design.

| Parameter | Ref. # | Min. | Typ. | Max | Unit |
|---|--------|------|------|-----|------|
| Pulse Width \overline{AS} or ALE High | 1 | 25 | - | - | ns |
| Muxed Address Setup Time to \overline{AS} or ALE Low | 2 | 10 | - | - | ns |
| Muxed Address Hold Time | 3 | 5 | - | - | ns |
| Delay Time \overline{AS} or ALE to \overline{WR} , \overline{RD} or \overline{DS} | 4 | 5 | - | - | ns |
| \overline{CS} & $\overline{R/W}$ Setup Time Before \overline{WR} , \overline{RD} or \overline{DS} Low | 5 | 0 | - | - | ns |
| \overline{CS} & $\overline{R/W}$ Hold Time | 6 | 0 | - | - | ns |
| Pulse Width, \overline{WR} , \overline{RD} , or \overline{DS} | 7 | 70 | - | - | ns |
| Write Data Setup Time | 8 | 30 | - | - | ns |
| Write Data Hold Time | 9 | 30 | - | - | ns |
| Output Data Delay Time from \overline{RD} or \overline{DS} Low | 10 | - | - | 100 | ns |
| Read Data Hold Time | 11 | 5 | - | - | ns |
| Delay Time \overline{WR} , \overline{RD} , or \overline{DS} to ALE or \overline{AS} Rise | 12 | 30 | - | - | ns |
| \overline{WR} or \overline{RD} Low to RDY Low | 13 | - | - | 55 | ns |
| \overline{WR} or \overline{RD} Low to RDY High | 14 | - | - | 100 | ns |
| \overline{WR} or \overline{RD} High to RDY HIGH-Z | 15 | - | - | 40 | ns |
| \overline{DS} Low to \overline{ACK} High | 16 | - | - | 65 | ns |
| \overline{DS} Low to \overline{ACK} Low | 17 | - | - | 100 | ns |
| \overline{DS} High to \overline{ACK} HIGH-Z | 18 | - | - | 40 | ns |

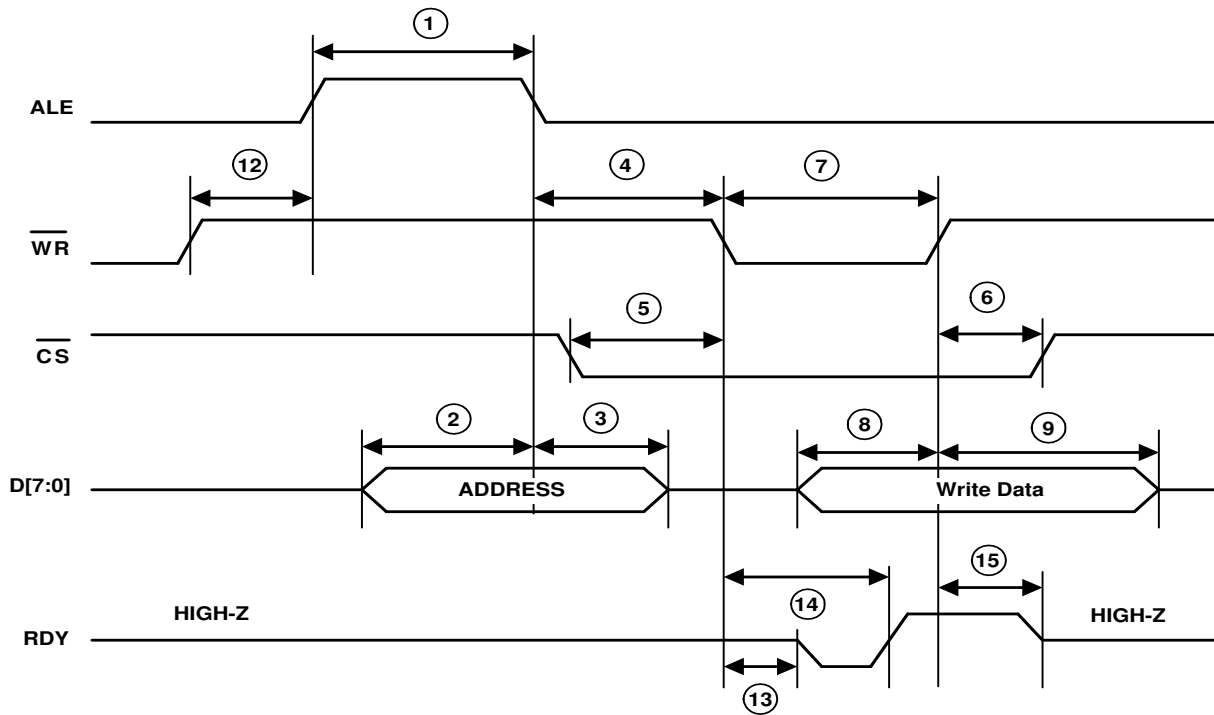


Figure 26. Parallel Port Timing - Write; Intel Multiplexed Address / Data Bus Mode

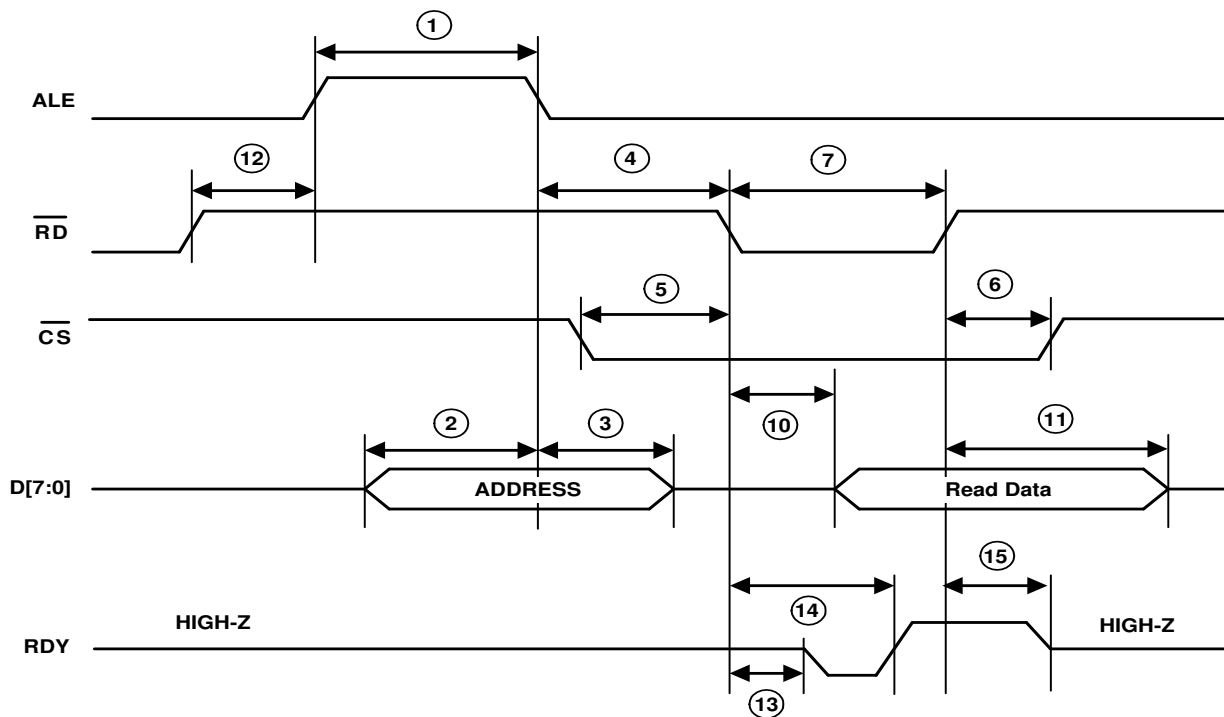


Figure 27. Parallel Mode Port Timing - Read; Intel Multiplexed Address / Data Bus Mode

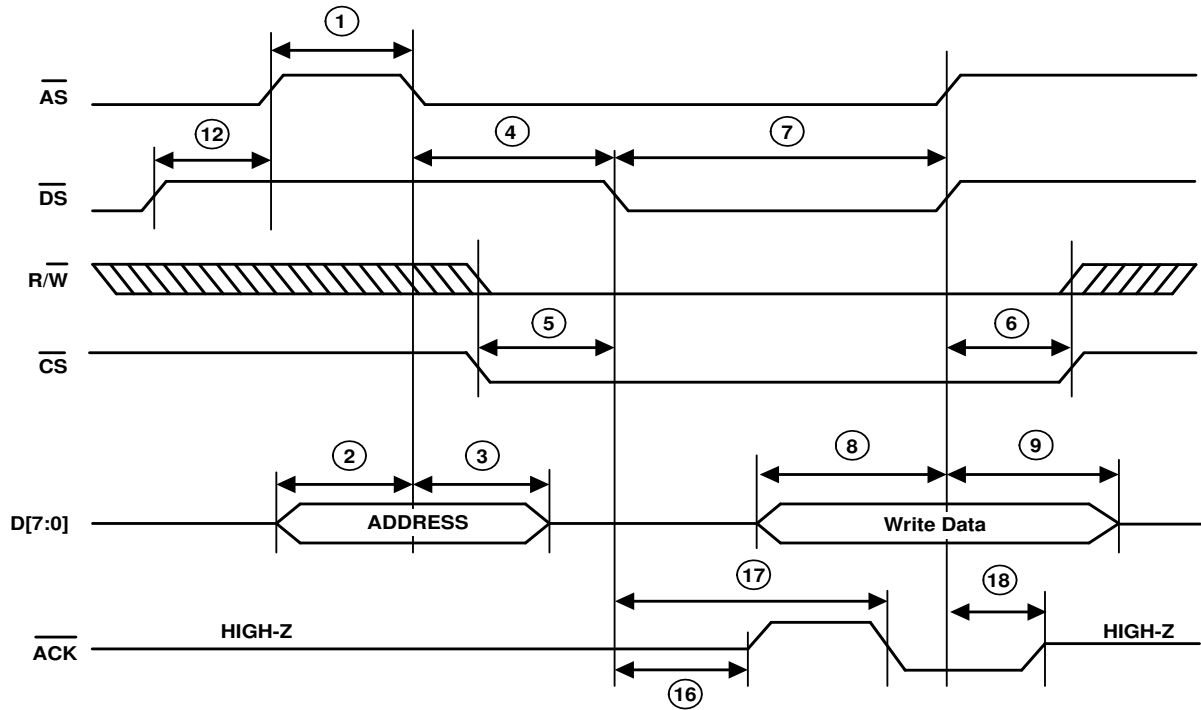


Figure 28. Parallel Port Timing - Write in Motorola Multiplexed Address / Data Bus

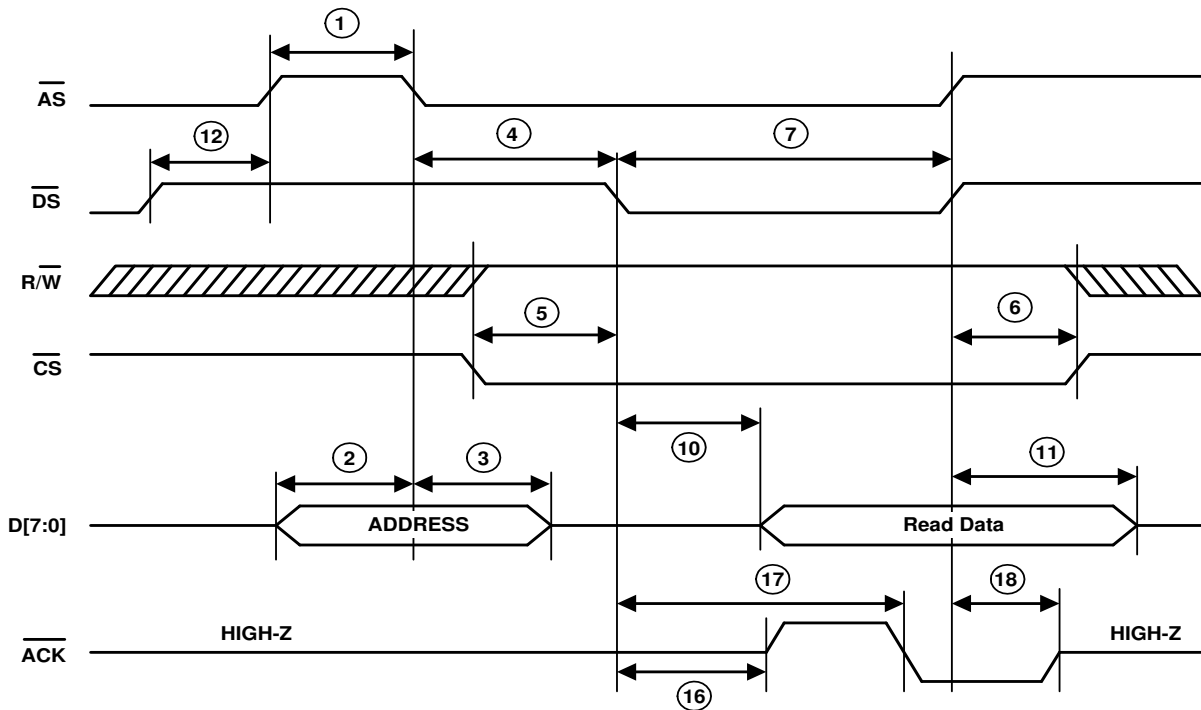


Figure 29. Parallel Port Timing - Read in Motorola Multiplexed Address / Data Bus

19.12 Switching Characteristics- Parallel Port (Non-multiplexed Mode)

* All paramters guaranteed by production, characterization or design.

| Parameter | Ref. # | Min. | Typ. | Max | Unit |
|---|--------|------|------|-----|------|
| Address Setup Time to \overline{WR} , \overline{RD} or \overline{DS} Low | 1 | 10 | - | - | ns |
| Address Hold Time | 2 | 5 | - | - | ns |
| \overline{CS} & $\overline{R/W}$ Setup Time Before \overline{WR} , \overline{RD} or \overline{DS} Low | 3 | 0 | - | - | ns |
| \overline{CS} & $\overline{R/W}$ Hold Time | 4 | 0 | - | - | ns |
| Pulse Width, \overline{WR} , \overline{RD} , or \overline{DS} | 5 | 70 | - | - | ns |
| Write Data Setup Time | 6 | 30 | - | - | ns |
| Write Data Hold Time | 7 | 30 | - | - | ns |
| Output Data Delay Time from \overline{RD} or \overline{DS} | 8 | - | - | 100 | ns |
| Read Data Hold Time | 9 | 5 | - | - | ns |
| \overline{WR} or \overline{RD} Low to RDY Low | 10 | - | - | 55 | ns |
| \overline{WR} , \overline{RD} or \overline{DS} Low to RDY High | 11 | - | - | 100 | ns |
| \overline{WR} , \overline{RD} or \overline{DS} High to RDY HIGH-Z | 12 | - | - | 40 | ns |
| \overline{DS} Low to \overline{ACK} High | 13 | - | - | 65 | ns |
| \overline{DS} Low to \overline{ACK} Low | 14 | - | - | 100 | ns |
| \overline{DS} High to \overline{ACK} HIGH-Z | 15 | - | - | 40 | ns |

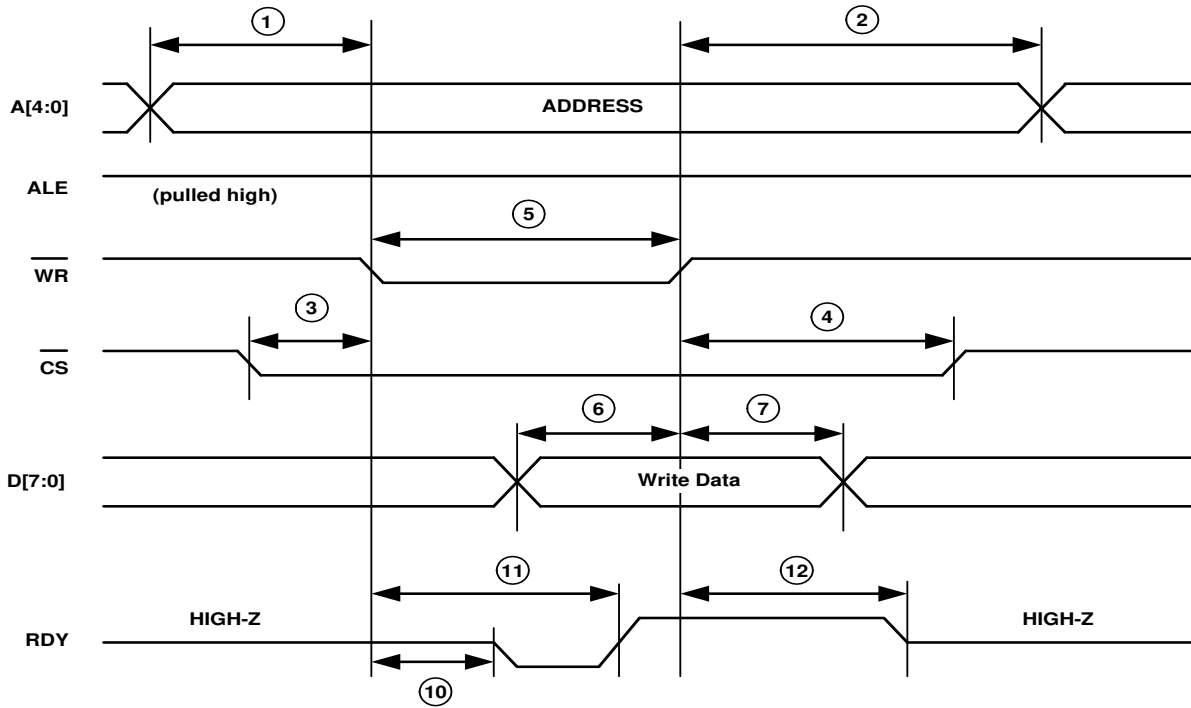


Figure 30. Parallel Port Timing - Write in Intel Non-Multiplexed Address / Data Bus Mode

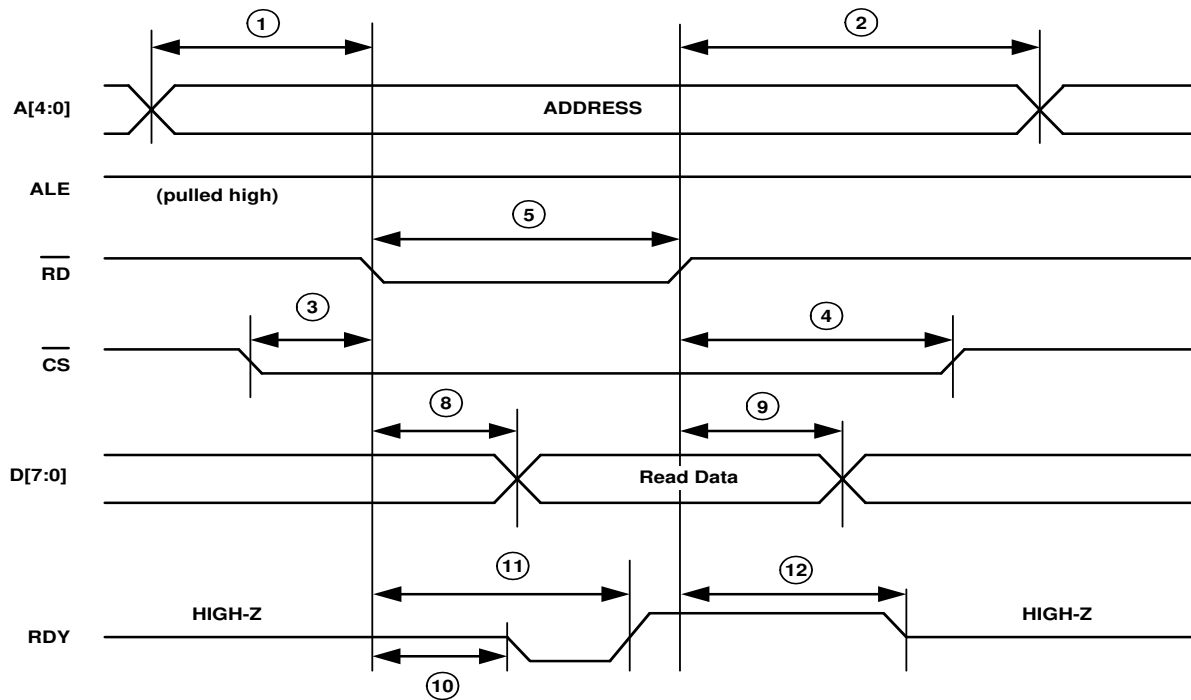


Figure 31. Parallel Port Timing - Read in Intel Non-Multiplexed Address / Data Bus Mode

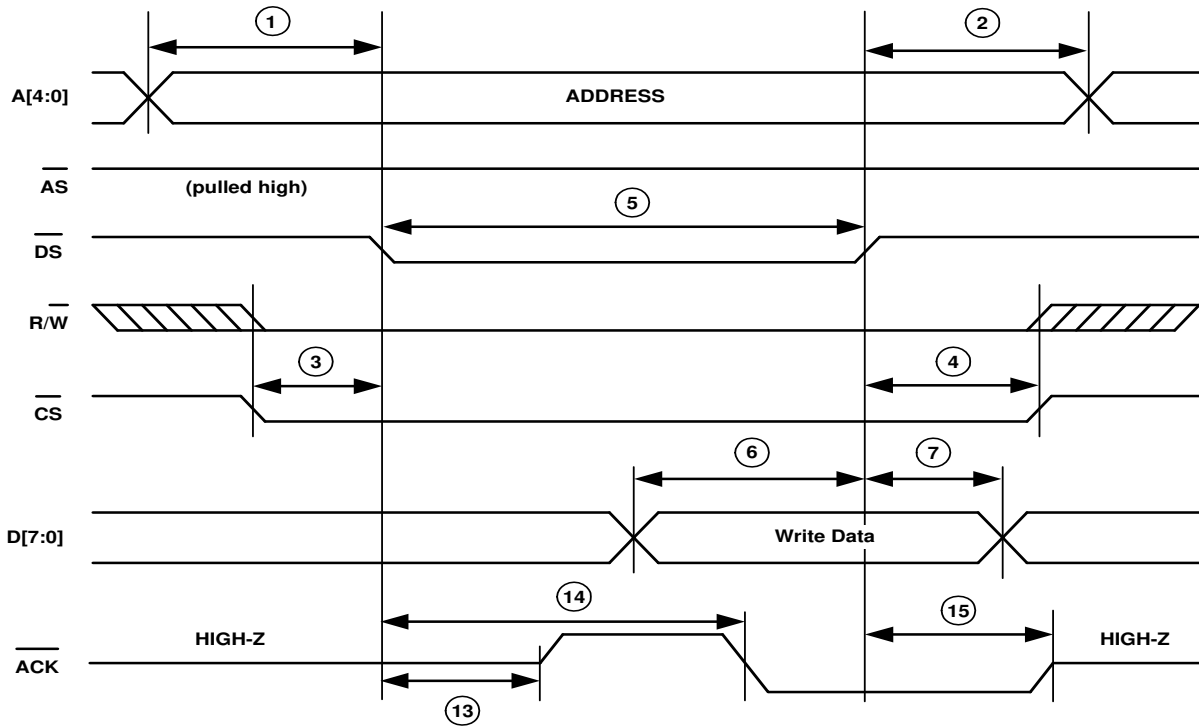


Figure 32. Parallel Port Timing - Write in Motorola Non-Multiplexed Address / Data Bus Mode

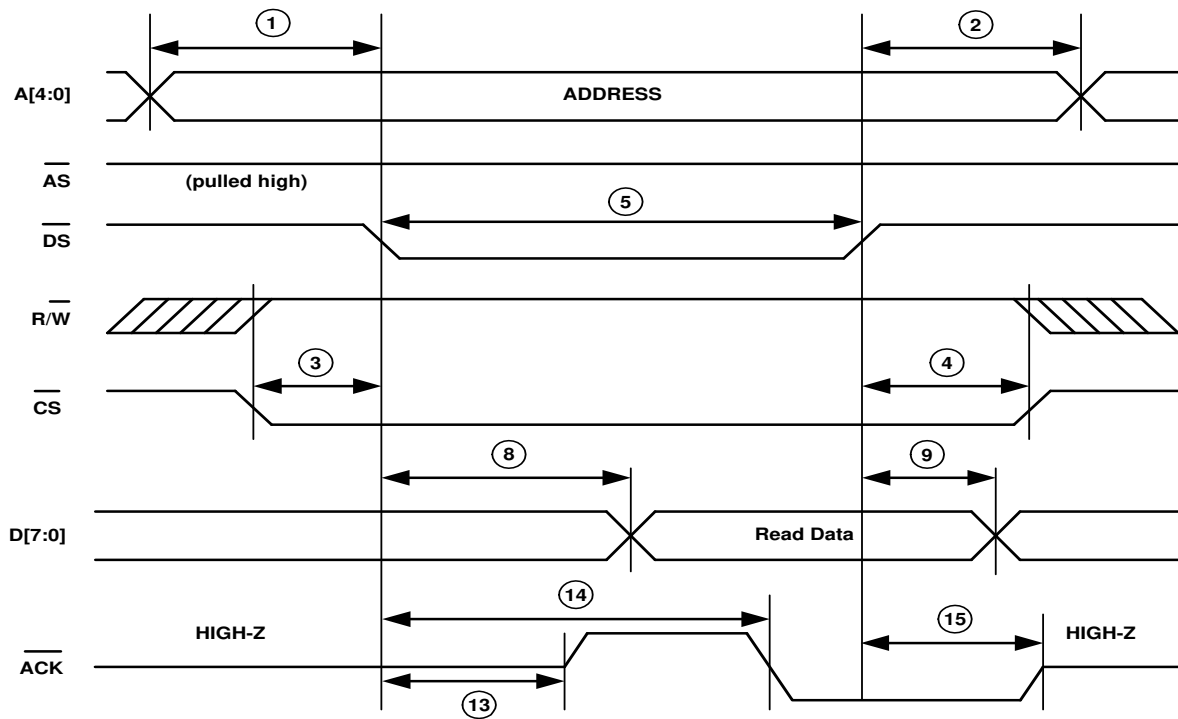
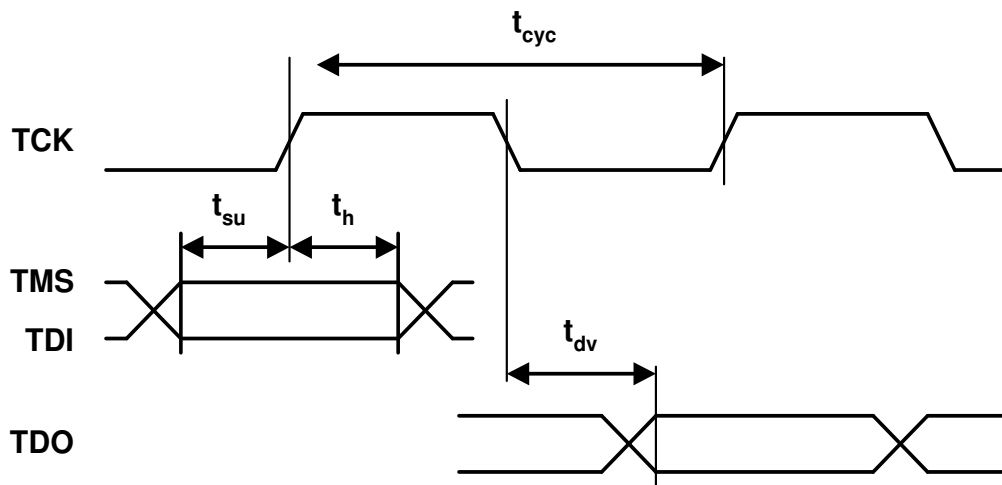


Figure 33. Parallel Port Timing - Read in Motorola Non-Multiplexed Address / Data Bus Mode

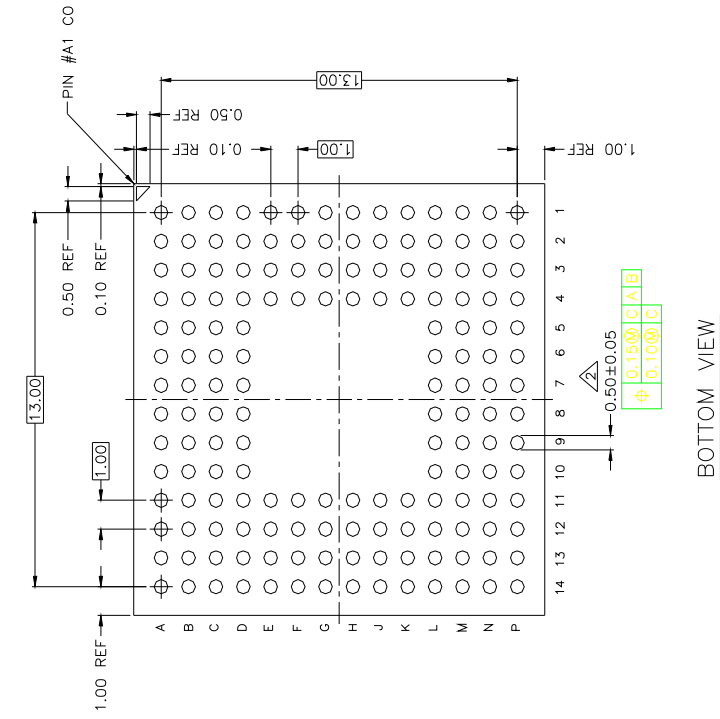
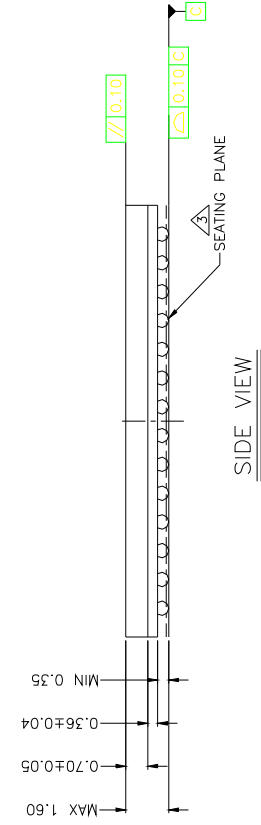
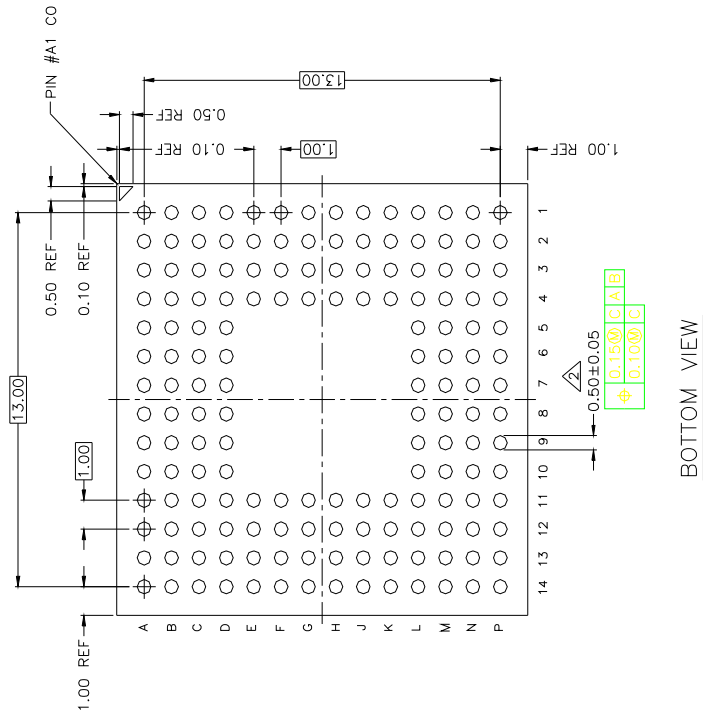
19.13 Switching Characteristics - JTAG

| Parameter | Symbol | Min. | Max | Units |
|----------------------------------|-----------|------|-----|-------|
| Cycle Time | t_{cyc} | 200 | - | nS |
| TMS/TDI to TCK Rising Setup Time | t_{su} | 50 | - | nS |
| TCK Rising to TMS/TDI Hold Time | t_h | 50 | - | nS |
| TCK Falling to TDO Valid | t_{dv} | - | 70 | nS |

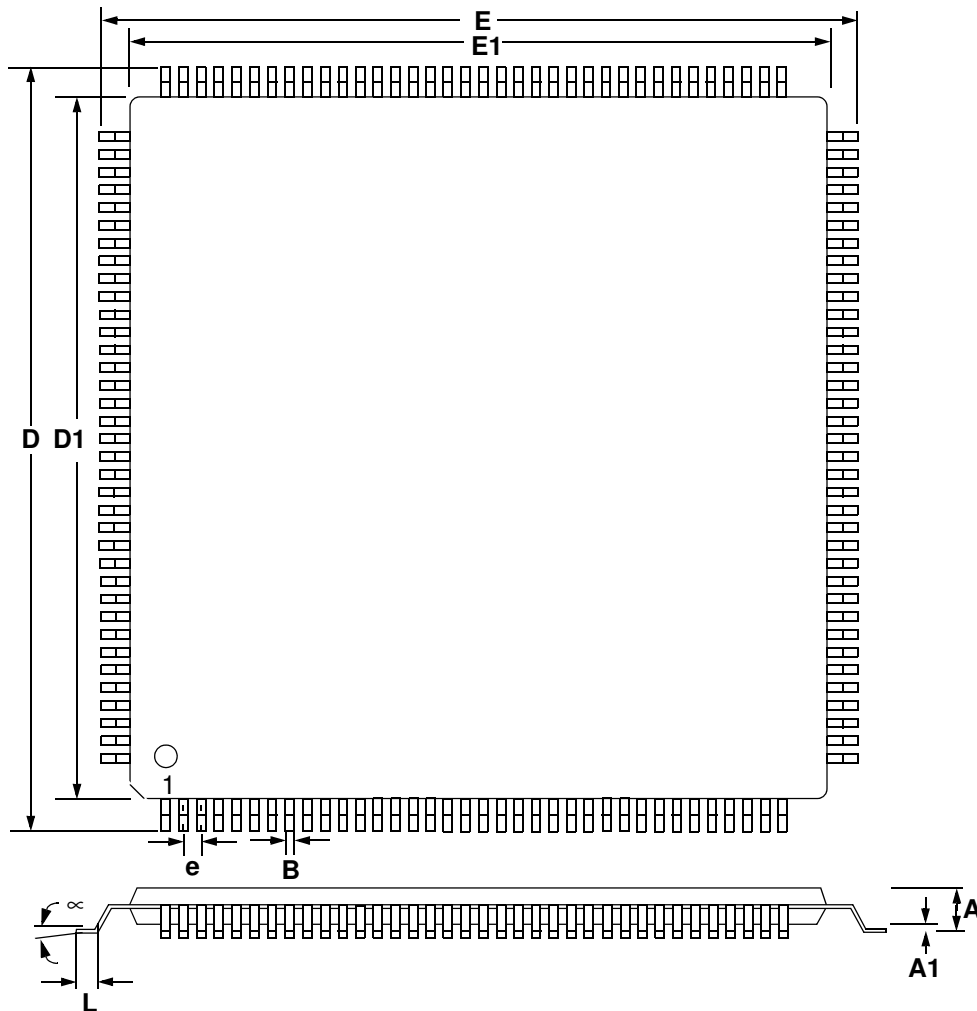

Figure 34. JTAG Switching Characteristics

20. COMPLIANT RECOMMENDATIONS AND SPECIFICATIONS

| | |
|-----------------------------|---------------|
| AT&T Pub 62411 | ITU-T I.431 |
| FCC Part 68 | ITU-T G.703 |
| ANSI T1.102 | ITU-T G.704 |
| ANSI T1.105 | ITU-T G.706 |
| ANSI T1.231 | ITU-T G.732 |
| ANSI T1.403 | ITU-T G.735 |
| ANSI T1.408 | ITU-T G.736 |
| Bell Core TR-TSY-000009 | ITU-T G.742 |
| Bell Core GR-253-Core Sonet | ITU-T G.772 |
| Bell Core GR-499-Core | ITU-T G.775 |
| ETSI ETS 300-011 | ITU-T G.783 |
| ETSI ETS 300-166 | ITU-T G.823 |
| ETSI ETS 300-233 | ITU-T O.151 |
| IEEE 1149.1 | OFTEL OTR-001 |
| ETSI TBR 12/13 | |

21. LFBGA PACKAGE DIMENSIONS

TOP VIEW

SIDE VIEW

BOTTOM VIEW

- NOTE
1. ALL DIMENSIONS AND TOLERANCE CONFORM TO ASME Y 14.5M—1994.
 2. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM [A].
 3. PRIMARY DATUM [C] AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
 4. THE SURFACE FINISH OF THE PACKAGE SHALL BE EDM CHARNILLE #24-#27.
 5. UNLESS OTHERWISE SPECIFIED TOLERANCE : DECIMAL ±0.05 ANGULAR ±2°

22. LQFP PACKAGE DIMENSIONS
144L LQFP PACKAGE DRAWING


| DIM | INCHES | | | MILLIMETERS | | |
|-----|--------|-----------|--------|-------------|----------|-------|
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | --- | 0.55 | 0.063 | --- | 1.40 | 1.60 |
| A1 | 0.002 | 0.004 | 0.006 | 0.05 | 0.10 | 0.15 |
| B | 0.007 | 0.008 | 0.011 | 0.17 | 0.20 | 0.27 |
| D | 0.854 | 0.866 BSC | 0.878 | 21.70 | 22.0 BSC | 22.30 |
| D1 | 0.783 | 0.787 BSC | 0.791 | 19.90 | 20.0 BSC | 20.10 |
| E | 0.854 | 0.866 BSC | 0.878 | 21.70 | 22.0 BSC | 22.30 |
| E1 | 0.783 | 0.787 BSC | 0.791 | 19.90 | 20.0 BSC | 20.10 |
| e* | 0.016 | 0.020 | 0.024 | 0.40 | 0.50 BSC | 0.60 |
| ∞ | 0.000° | 4° | 7.000° | 0.00° | 4° | 7.00° |
| L | 0.018 | 0.024 | 0.030 | 0.45 | 0.60 | 0.75 |

* Nominal pin pitch is 0.50 mm

Controlling dimension is mm.
JEDEC Designation: MS022

23. ORDERING INFORMATION

| Model | Temperature | Package |
|-------------|---------------|----------------------------|
| CS61884-IQZ | -40 to +85 °C | 160-pin LFBGA, 15mm X 15mm |
| CS61884-IRZ | | 144-pin LQFP, 15mm X 15mm |

24. ENVIRONMENTAL, MANUFACTURING, & HANDLING INFORMATION

| Model Number | Peak Reflow Temp | MSL Rating* | Max Floor Life |
|--------------|------------------|-------------|----------------|
| CS61884-IQZ | 260 °C | 3 | 7 Days |
| CS61884-IRZ | | | |

* MSL (Moisture Sensitivity Level) as specified by IPC/JEDEC J-STD-020.

All devices are now lead (Pb) free.

25. REVISION HISTORY

| Revision | Date | Changes |
|----------|----------|--|
| F3 | MAR 2011 | Removed all lead-containing device ordering information. Removed 160-pin FBGA package option. Corrected formerly named TFBGA to LFBGA. |