SDAS230A - DECEMBER 1983 - REVISED AUGUST 1995

- Functionally Equivalent to AMD's AM29821
- Provide Extra Data Width Necessary for Wider Address/Data Paths or Buses With Parity
- Outputs Have Undershoot-Protection Circuitry
- Power-Up High-Impedance State
- Buffered Control Inputs to Reduce dc Loading Effects
- Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (NT) and Ceramic (JT) 300-mil DIPs

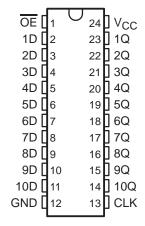
#### description

These 10-bit flip-flops feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers with parity, and working registers.

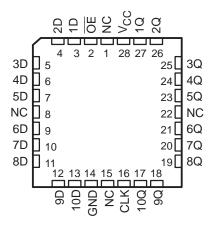
The ten flip-flops are edge-triggered D-type flip-flops. On the positive transition of the clock (CLK) input, the Q outputs are true to the data (D) input.

A buffered output-enable ( $\overline{OE}$ ) input can be used to place the ten outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

#### SN54AS821A . . . JT PACKAGE SN74AS821A . . . DW OR NT PACKAGE (TOP VIEW)



# SN54AS821A . . . FK PACKAGE (TOP VIEW)



NC - No internal connection

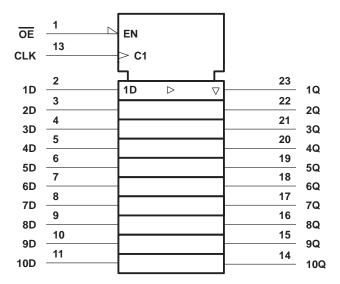
OE does not affect the internal operation of the flip-flops. Previously stored data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54AS821A is characterized for operation over the full military temperature range of  $-55^{\circ}$ C to  $125^{\circ}$ C. The SN74AS821A is characterized for operation from  $0^{\circ}$ C to  $70^{\circ}$ C.

# FUNCTION TABLE (each flip-flop)

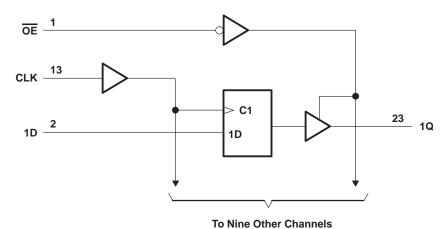
			1.7
	INPUTS		OUTPUT
OE	CLK	D	Q
L	1	Н	Н
L	$\uparrow$	L	L
L	L	Χ	Q <sub>0</sub>
Н	Χ	Χ	Z

#### logic symbol†



<sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the DW, JT, and NT packages.

#### logic diagram (positive logic)



Pin numbers shown are for the DW, JT, and NT packages.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V <sub>CC</sub>	7 V
Input voltage, V <sub>I</sub>	7 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range, T <sub>A</sub> : SN54AS821A	−55°C to 125°C
SN74AS821A	0°C to 70°C
Storage temperature range	-65°C to 150°C

<sup>‡</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.



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#### recommended operating conditions

		SN54AS821A		SN	UNIT			
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
V <sub>IL</sub>	Low-level input voltage			0.8			0.8	V
IOH	High-level output current			-24			-24	mA
lOL	Low-level output current			32			48	mA
t <sub>W</sub> *	Pulse duration, CLK high or low	9			8			ns
t <sub>su</sub> *	Setup time, data before CLK↑	7			6			ns
th*	Hold time, data after CLK↑	0			0			ns
TA	Operating free-air temperature	-55		125	0		70	°C

<sup>\*</sup> On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data but is not production tested.

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETER	TEST CONDITIONS			54AS82	1A	SN7	74AS82 <sup>-</sup>	1A	
PARAMETER	IESI C	TEST CONDITIONS			MAX	MIN	TYP†	MAX	UNIT
VIK	V <sub>CC</sub> = 4.5 V,	I <sub>I</sub> = -18 mA			-1.2			-1.2	V
	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	$I_{OH} = -2 \text{ mA}$	V <sub>CC</sub> -2	!		V <sub>CC</sub> -2	!		
VOH	V 45V	I <sub>OH</sub> = -15 mA	2.4	3.2		2.4	3.2		V
	V <sub>CC</sub> = 4.5 V	I <sub>OH</sub> = -24 mA	2			2			
.,	V45V	I <sub>OL</sub> = 32 mA		0.25	0.5				V
VOL	V <sub>CC</sub> = 4.5 V	I <sub>OL</sub> = 48 mA					0.35	0.5	V
<sup>I</sup> OZH	$V_{CC} = 5.5 V$ ,	$V_0 = 2.7 \text{ V}$			50			50	μΑ
lozL	$V_{CC} = 5.5 V$ ,	V <sub>I</sub> = 0.4 V			-50			-50	μΑ
lį	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 7 V			0.1			0.1	mA
lіН	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 2.7 V			20			20	μΑ
I <sub>IL</sub>	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 0.4 V			-0.5			-0.5	mA
IO <sup>‡</sup>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.25 V	-30		-112	-30		-112	mA
Icc		Outputs high		55	88		55	88	
	V <sub>CC</sub> = 5.5 V	Outputs low		68	109		68	109	mA
		Outputs disabled		70	113		70	113	

<sup>&</sup>lt;sup>†</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ .



<sup>&</sup>lt;sup>‡</sup> The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, los.

## SN54AS821A, SN74AS821A 10-BIT BUS-INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

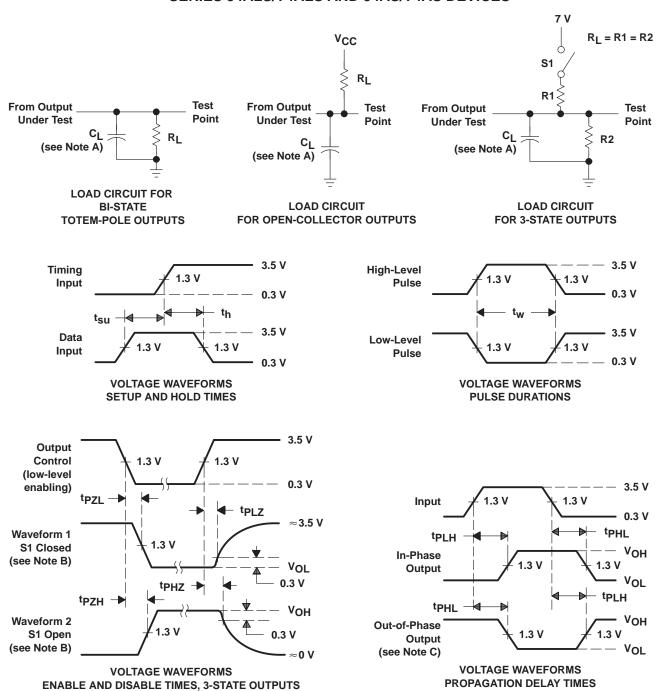
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## switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>C</sub> C <sub>L</sub> R1 R2 T <sub>A</sub>	UNIT			
			SN54A	S821A	SN74A		
			MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	CLK	Am. 0	3.5	9	3.5	7.5	ns
<sup>t</sup> PHL	OLIX	Any Q	3.5	14	3.5	13	113
<sup>t</sup> PZH	ŌĒ	A O	4	12	3	11	ns
t <sub>PZL</sub>	OE	Any Q	4	13	4	12	115
<sup>t</sup> PHZ	ŌĒ	Any Q	1	10	1	8	ns
<sup>t</sup> PLZ	OL .	Ally Q	1	10	1	8	113

<sup>†</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

#### PARAMETER MEASUREMENT INFORMATION SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
- D. All input pulses have the following characteristics:  $PRR \le 1$  MHz,  $t_f = t_f = 2$  ns, duty cycle = 50%.
- E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms







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#### **PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp (3)
5962-9078001M3A	ACTIVE	LCCC	FK	28	1	TBD	POST-PLATE	N / A for Pkg Type
5962-9078001MKA	ACTIVE	CFP	W	24	1	TBD	A42	N / A for Pkg Type
5962-9078001MLA	ACTIVE	CDIP	JT	24	1	TBD	A42 SNPB	N / A for Pkg Type
SN54AS821AJT	ACTIVE	CDIP	JT	24	1	TBD	A42 SNPB	N / A for Pkg Type
SN74AS821ADW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AS821ADWE4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AS821ADWG4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AS821ADWR	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AS821ADWRE4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AS821ADWRG4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AS821ANT	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74AS821ANTE4	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SNJ54AS821AFK	ACTIVE	LCCC	FK	28	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54AS821AJT	ACTIVE	CDIP	JT	24	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ54AS821AW	ACTIVE	CFP	W	24	1	TBD	A42	N / A for Pkg Type

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

**Pb-Free** (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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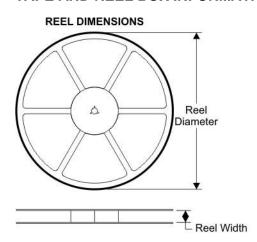
## **PACKAGE OPTION ADDENDUM**

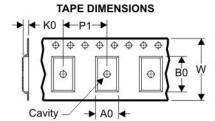
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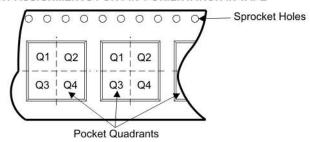
#### TAPE AND REEL BOX INFORMATION





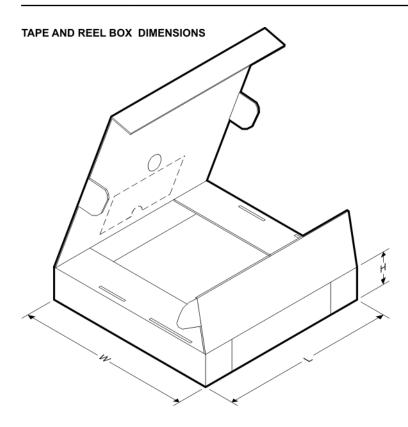
	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AS821ADWR	DW	24	SITE 60	330	24	10.75	15.7	2.7	12	24	Q1



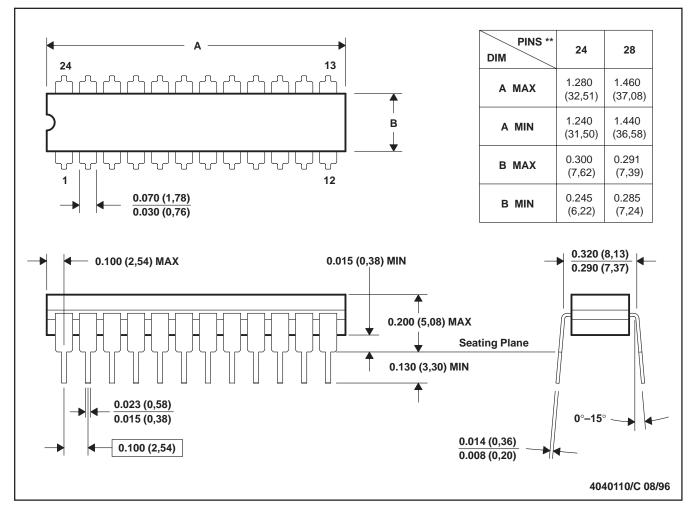


Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
SN74AS821ADWR	DW	24	SITE 60	346.0	346.0	0.0

#### JT (R-GDIP-T\*\*)

#### 24 LEADS SHOWN

#### **CERAMIC DUAL-IN-LINE**

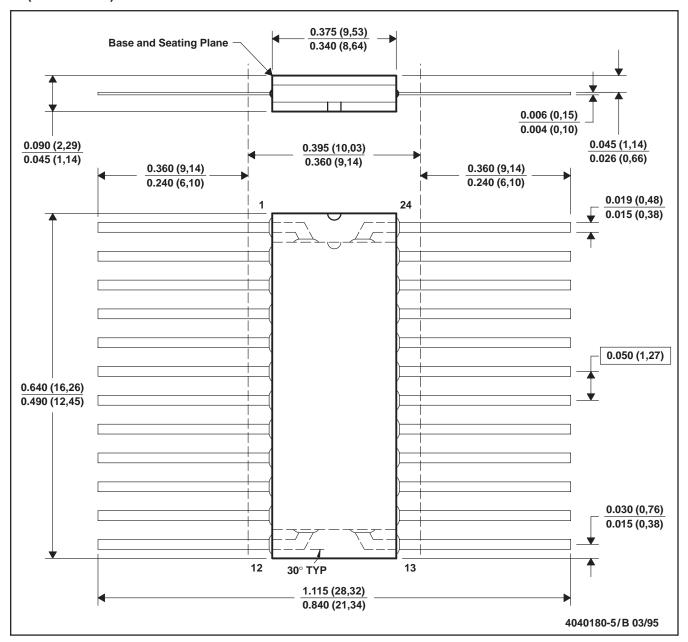


NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification.
- E. Falls within MIL STD 1835 GDIP3-T24, GDIP4-T28, and JEDEC MO-058 AA, MO-058 AB

#### W (R-GDFP-F24)

#### **CERAMIC DUAL FLATPACK**



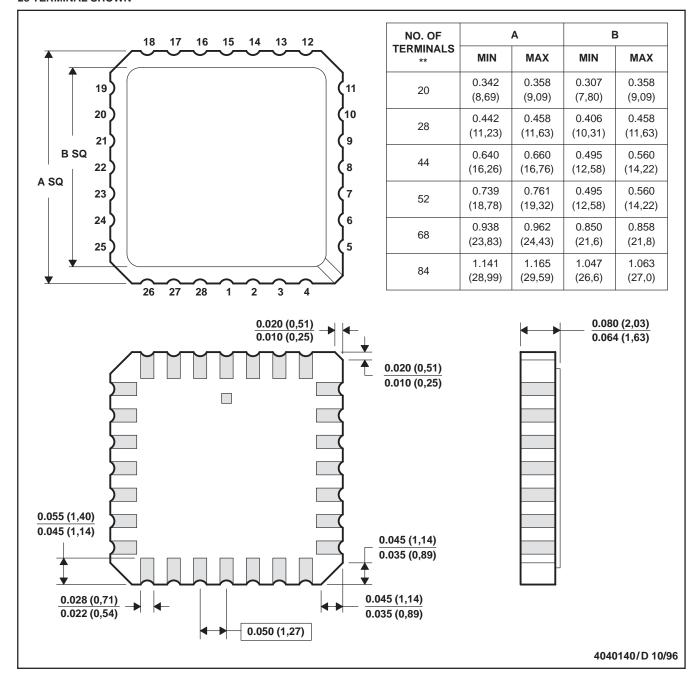
- NOTES: A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Falls within MIL-STD-1835 GDFP2-F24 and JEDEC MO-070AD
  - E. Index point is provided on cap for terminal identification only.



#### FK (S-CQCC-N\*\*)

#### **28 TERMINAL SHOWN**

#### **LEADLESS CERAMIC CHIP CARRIER**



NOTES: A. All linear dimensions are in inches (millimeters).

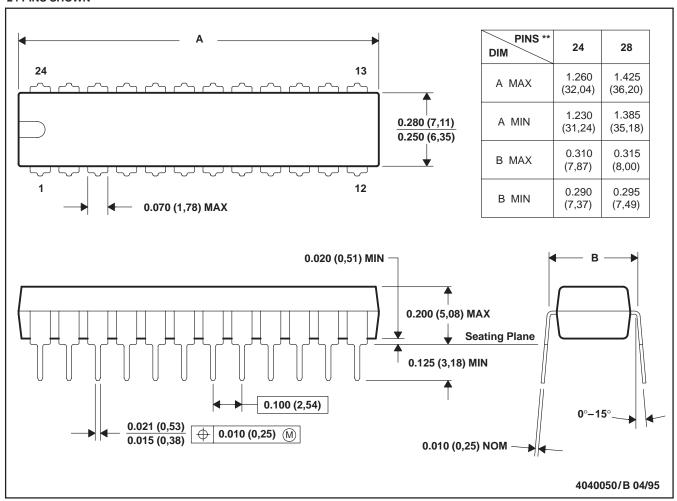
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. The terminals are gold plated.
- E. Falls within JEDEC MS-004



#### NT (R-PDIP-T\*\*)

#### PLASTIC DUAL-IN-LINE PACKAGE

#### **24 PINS SHOWN**

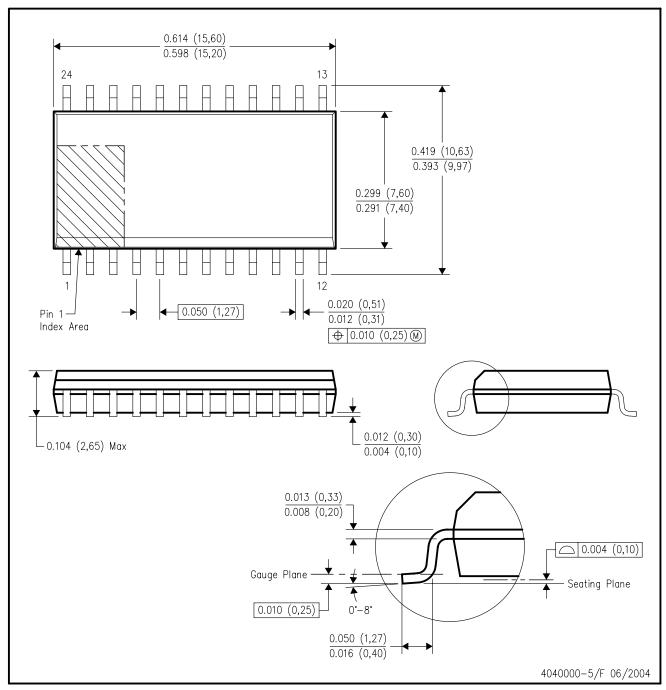


NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

## DW (R-PDSO-G24)

## PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AD.



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