LM2736 Thin SOT 750 mA Load Step-Down DC-DC Regulator

1 Features

- Thin SOT-6 Package
- 3.0 V to 18 V Input Voltage Range
- 1.25 V to 16 V Output Voltage Range
- 750 mA Output Current
- 550 kHz (LM2736Y) and 1.6 MHz (LM2736X) Switching Frequencies
- 350 mΩ NMOS Switch
- 30 nA Shutdown Current
- 1.25 V, 2% Internal Voltage Reference
- Internal Soft-Start
- Current-Mode, PWM Operation
- WEBENCH® Online Design Tool
- Thermal Shutdown

2 Applications

- Local Point of Load Regulation
- Core Power in HDDs
- Set-Top Boxes
- Battery Powered Devices
- USB Powered Devices
- DSL Modems
- Notebook Computers

3 Description

The LM2736 regulator is a monolithic, high frequency, PWM step-down DC/DC converter in a 6-pin Thin SOT package. It provides all the active functions to provide local DC/DC conversion with fast transient response and accurate regulation in the smallest possible PCB area.

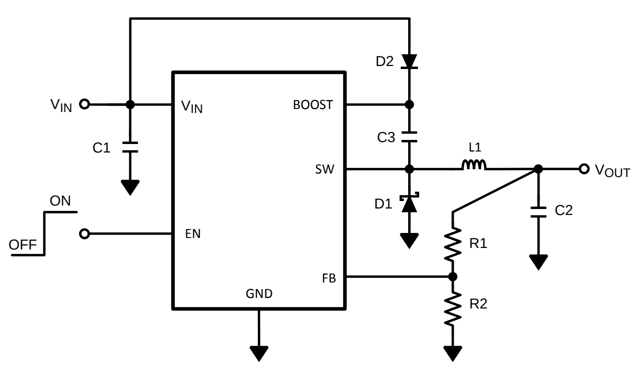
With a minimum of external components and online design support through WEBENCH®, the LM2736 is easy to use. The ability to drive 750 mA loads with an internal 350 mΩ NMOS switch using state-of-the-art 0.5 µm BiCMOS technology results in the best power density available. The world class control circuitry allows for on-times as low as 13 ns, thus supporting exceptionally high frequency conversion over the entire 3 V to 18 V input operating range down to the minimum output voltage of 1.25 V. Switching frequency is internally set to 550 kHz (LM2736Y) or 1.6 MHz (LM2736X), allowing the use of extremely small surface mount inductors and chip capacitors. Even though the operating frequencies are very high, efficiencies up to 90% are easy to achieve. External shutdown is included, featuring an ultra-low stand-by current of 30 nA. The LM2736 utilizes current-mode control and internal compensation to provide high-performance regulation over a wide range of operating conditions. Additional features include internal soft-start circuitry to reduce inrush current, pulse-by-pulse current limit, thermal shutdown, and output over-voltage protection.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM2736	SOT (6)	2.90 mm x 1.60 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Typical Application Circuit



Efficiency vs. Load Current "X"
V_{IN} = 5 V, V_{OUT} = 3.3 V

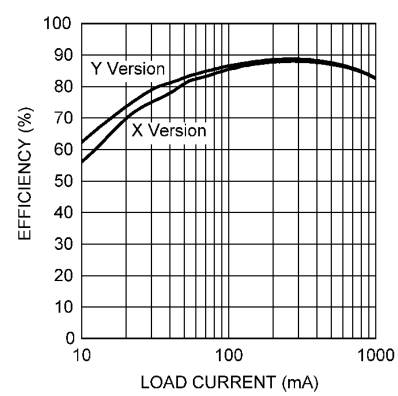


Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision G (October 2014) to Revision H — **Page**

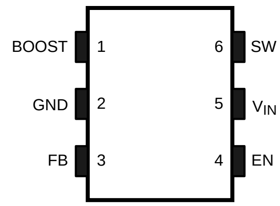
- Updated Design Requirements and moved *Bill of Materials* to *Detailed Design Procedures*. ... 13

Changes from Revision F (April 2013) to Revision G — **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 4

5 Pin Configuration and Functions

Package DDC (R-PDSO-G6)
6-Lead SOT
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
BOOST	1	I	Boost voltage that drives the internal NMOS control switch. A bootstrap capacitor is connected between the BOOST and SW pins.
GND	2	GND	Signal and Power ground pin. Place the bottom resistor of the feedback network as close as possible to this pin for accurate regulation.
FB	3	I	Feedback pin. Connect FB to the external resistor divider to set output voltage.
EN	4	I	Enable control input. Logic high enables operation. Do not allow this pin to float or be greater than V_{IN} + 0.3 V.
V_{IN}	5	I	Input supply voltage. Connect a bypass capacitor to this pin.
SW	6	O	Output switch. Connects to the inductor, catch diode, and bootstrap capacitor.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)]

		MIN	MAX	UNIT
V_{IN}		-0.5	22	V
SW Voltage		-0.5	22	V
Boost Voltage		-0.5	28	V
Boost to SW Voltage		-0.5	8	V
FB Voltage		-0.5	3	V
EN Voltage		-0.5	V_{IN} + 0.3	V
Junction Temperature			150	°C
Soldering Information	Infrared/Convection Reflow (15sec)		220	°C
	Wave Soldering Lead temperature (10sec)		260	°C
T_{stg}	Storage temperature	-65	150	°C

(1) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[(1)]	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
V_{IN}	3		18	V
SW Voltage	-0.5		18	V
Boost Voltage	-0.5		23	V
Boost to SW Voltage	1.6		5.5	V
Junction Temperature Range	−40		125	°C

6.4 Thermal Information

THERMAL METRIC[(1)]		LM2736 DDC 6 PINS	UNIT
$R_{\theta JA}$[(2)]	Junction-to-ambient thermal resistance	158.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	46.5	
$R_{\theta JB}$	Junction-to-board thermal resistance	29.5	
ψ_{JT}	Junction-to-top characterization parameter	0.8	
ψ_{JB}	Junction-to-board characterization parameter	29.2	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) Thermal shutdown will occur if the junction temperature exceeds 165°C. The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA} and T_A . The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly onto a 3” x 3” PC board with 2oz. copper on 4 layers in still air. For a 2 layer board using 1 oz. copper in still air, θ_{JA} = 204°C/W.

6.5 Electrical Characteristics

Specifications with standard typeface are for T_J = 25°C unless otherwise specified. Datasheet min/max specification limits are ensured by design, test, or statistical analysis.

PARAMETER		TEST CONDITIONS	T_J = 25°C			TJ = -40°C to 125°C			UNIT
			MIN(1)	TYP(2)	MAX(1)	MIN	TYP	MAX	
V_{FB}	Feedback Voltage			1.250		1.225		1.275	V
$\Delta V_{FB}/\Delta V_{IN}$	Feedback Voltage Line Regulation	V_{IN} = 3V to 18V		0.01					% / V
I_{FB}	Feedback Input Bias Current	Sink/Source		10				250	nA
UVLO	Undervoltage Lockout	V_{IN} Rising		2.74				2.90	V
	Undervoltage Lockout	V_{IN} Falling		2.3		2.0			
	UVLO Hysteresis			0.44		0.30		0.62	
F_{SW}	Switching Frequency	LM2736X		1.6		1.2		1.9	MHz
		LM2736Y		0.55		0.40		0.66	
D_{MAX}	Maximum Duty Cycle	LM2736X		92%		85%			
		LM2736Y		96%		90%			
D_{MIN}	Minimum Duty Cycle	LM2736X		2%					
		LM2736Y		1%					
$R_{DS(ON)}$	Switch ON Resistance	V_{BOOST} - V_{SW} = 3V		350				650	mΩ
I_{CL}	Switch Current Limit	V_{BOOST} - V_{SW} = 3V		1.5		1.0		2.3	A
I_Q	Quiescent Current	Switching		1.5				2.5	mA
	Quiescent Current (shutdown)	V_{EN} = 0V		30					nA
I_{BOOST}	Boost Pin Current	LM2736X (50% Duty Cycle)		2.2				3.3	mA
		LM2736Y (50% Duty Cycle)		0.9				1.6	
V_{EN_TH}	Shutdown Threshold Voltage	V_{EN} Falling						0.4	V
	Enable Threshold Voltage	V_{EN} Rising				1.8			
I_{EN}	Enable Pin Current	Sink/Source		10					nA
I_{SW}	Switch Leakage			40					nA

(1) Specified to Texas Instruments' Average Outgoing Quality Level (AOQL).
(2) Typicals represent the most likely parametric norm.

6.6 Typical Characteristics

All curves taken at V_{IN} = 5V, V_{BOOST} - V_{SW} = 5V, L1 = 4.7 µH ("X"), L1 = 10 µH ("Y"), and T_A = 25°C, unless specified otherwise.

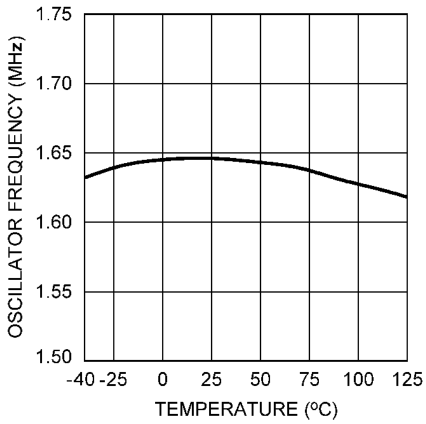


Figure 1. Oscillator Frequency vs Temperature - "X"

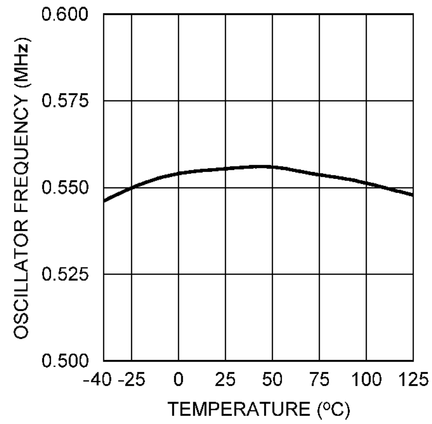


Figure 2. Oscillator Frequency vs Temperature - "Y"

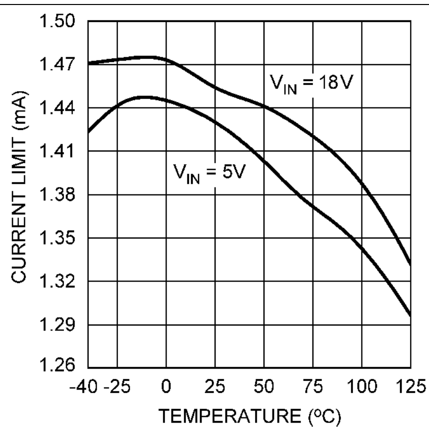


Figure 3. Current Limit vs Temperature

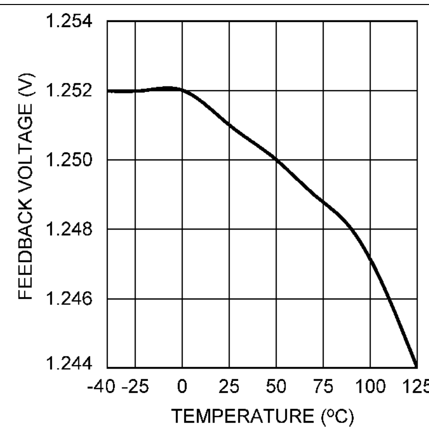


Figure 4. V_{FB} vs Temperature

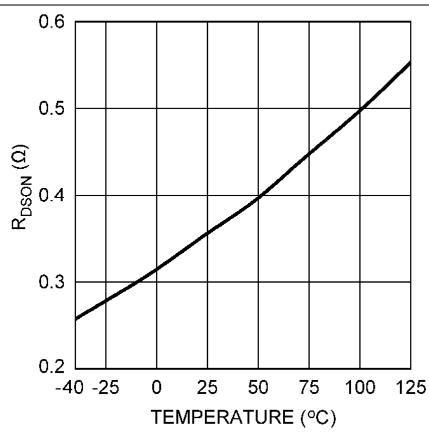


Figure 5. R_{DSON} vs Temperature

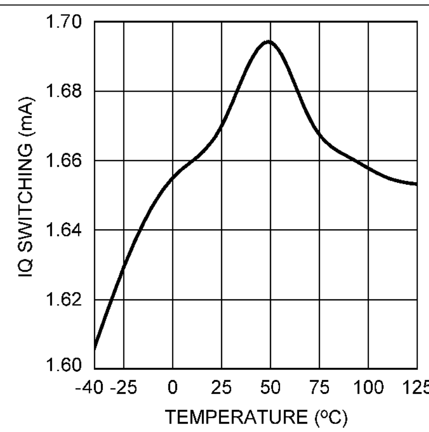


Figure 6. I_Q Switching vs Temperature

Typical Characteristics (continued)

All curves taken at V_{IN} = 5V, V_{BOOST} - V_{SW} = 5V, L1 = 4.7 µH ("X"), L1 = 10 µH ("Y"), and T_A = 25°C, unless specified otherwise.

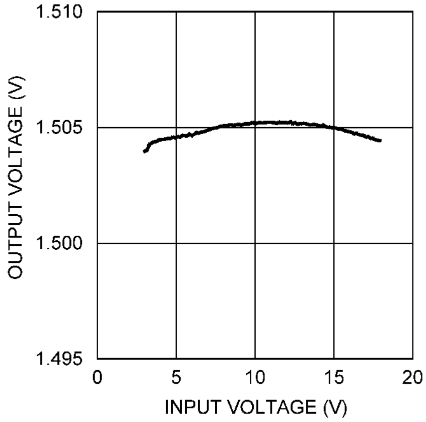


Figure 7. Line Regulation - "X"

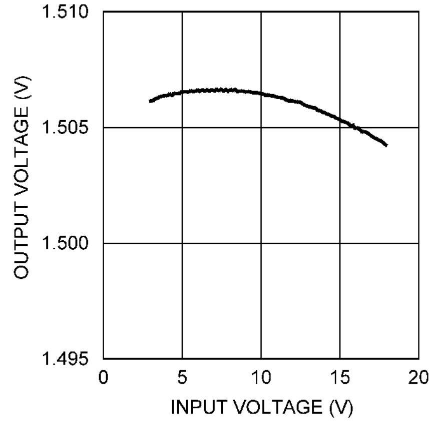
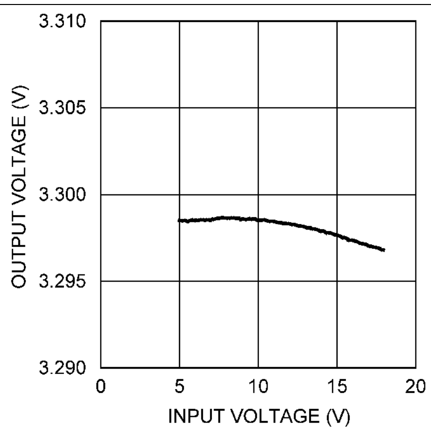
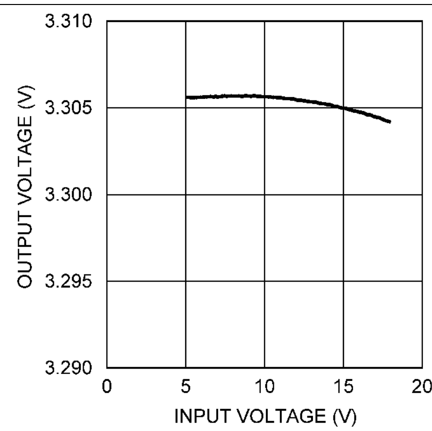


Figure 8. Line Regulation - "Y"



V_{OUT} = 3.3 V, I_{OUT} = 500 mA

Figure 9. Line Regulation - "X"



V_{OUT} = 3.3 V, I_{OUT} = 500 mA

Figure 10. Line Regulation - "Y"

7 Detailed Description

7.1 Overview

The LM2736 device is a constant frequency PWM buck regulator IC that delivers a 750 mA load current. The regulator has a preset switching frequency of either 550 kHz (LM2736Y) or 1.6 MHz (LM2736X). These high frequencies allow the LM2736 device to operate with small surface mount capacitors and inductors, resulting in DC/DC converters that require a minimum amount of board space. The LM2736 device is internally compensated, so it is simple to use, and requires few external components. The LM2736 device uses current-mode control to regulate the output voltage.

The following operating description of the LM2736 device will refer to the Simplified Block Diagram (*Functional Block Diagram*) and to the waveforms in Figure 11. The LM2736 device supplies a regulated output voltage by switching the internal NMOS control switch at constant frequency and variable duty cycle. A switching cycle begins at the falling edge of the reset pulse generated by the internal oscillator. When this pulse goes low, the output control logic turns on the internal NMOS control switch. During this on-time, the SW pin voltage (V_{SW}) swings up to approximately V_{IN}, and the inductor current (I_L) increases with a linear slope. I_L is measured by the current-sense amplifier, which generates an output proportional to the switch current. The sense signal is summed with the regulator's corrective ramp and compared to the error amplifier's output, which is proportional to the difference between the feedback voltage and V_{REF}. When the PWM comparator output goes high, the output switch turns off until the next switching cycle begins. During the switch off-time, inductor current discharges through Schottky diode D1, which forces the SW pin to swing below ground by the forward voltage (V_D) of the catch diode. The regulator loop adjusts the duty cycle (D) to maintain a constant output voltage.

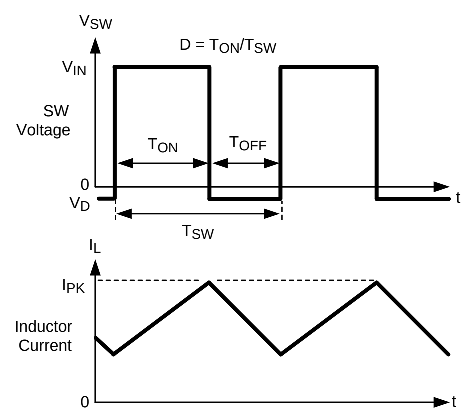
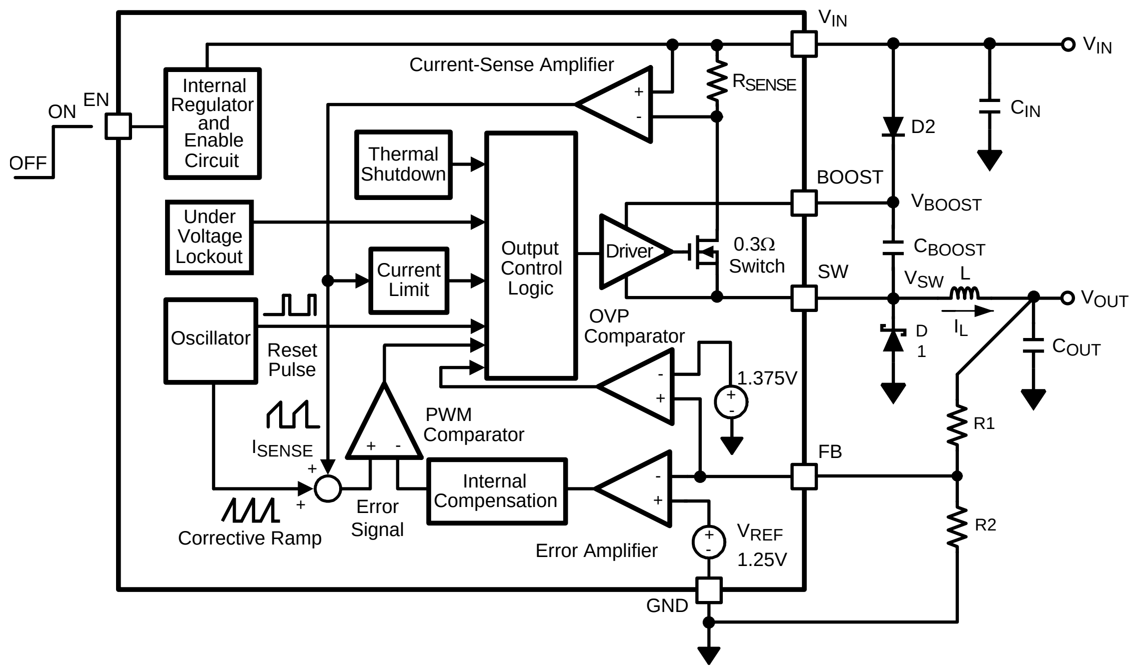


Figure 11. LM2736 Waveforms of SW Pin Voltage and Inductor Current

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Output Overvoltage Protection

The overvoltage comparator compares the FB pin voltage to a voltage that is 10% higher than the internal reference Vref. Once the FB pin voltage goes 10% above the internal reference, the internal NMOS control switch is turned off, which allows the output voltage to decrease toward regulation.

7.3.2 Undervoltage Lockout

Undervoltage lockout (UVLO) prevents the LM2736 device from operating until the input voltage exceeds 2.74 V (typ).

The UVLO threshold has approximately 440mV of hysteresis, so the part will operate until V_{IN} drops below 2.3 V (typ). Hysteresis prevents the part from turning off during power up if V_{IN} is non-monotonic.

7.3.3 Current Limit

The LM2736 device uses cycle-by-cycle current limiting to protect the output switch. During each switching cycle, a current limit comparator detects if the output switch current exceeds 1.5 A (typ), and turns off the switch until the next switching cycle begins.

7.3.4 Thermal Shutdown

Thermal shutdown limits total power dissipation by turning off the output switch when the IC junction temperature exceeds 165°C. After thermal shutdown occurs, the output switch doesn't turn on until the junction temperature drops to approximately 150°C.

7.4 Device Functional Modes

7.4.1 Enable Pin / Shutdown Mode

The LM2736 device has a shutdown mode that is controlled by the enable pin (EN). When a logic low voltage is applied to EN, the part is in shutdown mode and its quiescent current drops to typically 30 nA. Switch leakage adds another 40 nA from the input supply. The voltage at this pin should never exceed V_{IN} + 0.3 V.

7.4.2 Soft-Start

This function forces V_{OUT} to increase at a controlled rate during start up. During soft-start, the error amplifier's reference voltage ramps from 0 V to its nominal value of 1.25 V in approximately 200 µs. This forces the regulator output to ramp up in a more linear and controlled fashion, which helps reduce inrush current.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Boost Function

Capacitor C_{BOOST} and diode D2 in Figure 12 are used to generate a voltage V_{BOOST}. V_{BOOST} - V_{SW} is the gate drive voltage to the internal NMOS control switch. To properly drive the internal NMOS switch during its on-time, V_{BOOST} needs to be at least 1.6 V greater than V_{SW}. Although the LM2736 device will operate with this minimum voltage, it may not have sufficient gate drive to supply large values of output current. Therefore, it is recommended that V_{BOOST} be greater than 2.5 V above V_{SW} for best efficiency. V_{BOOST} – V_{SW} should not exceed the maximum operating limit of 5.5 V.

5.5 V > V_{BOOST} – V_{SW} > 2.5 V for best performance.

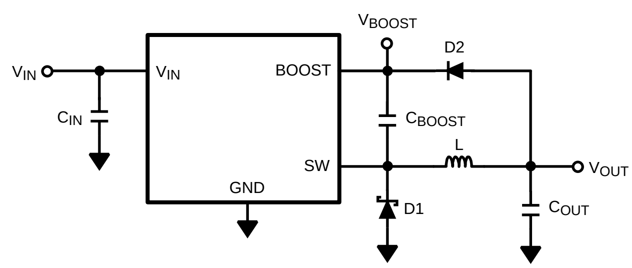


Figure 12. V_{OUT} Charges C_{BOOST}

When the LM2736 device starts up, internal circuitry from the BOOST pin supplies a maximum of 20 mA to C_{BOOST}. This current charges C_{BOOST} to a voltage sufficient to turn the switch on. The BOOST pin will continue to source current to C_{BOOST} until the voltage at the feedback pin is greater than 1.18 V.

There are various methods to derive V_{BOOST}:

1. From the input voltage (V_{IN})
2. From the output voltage (V_{OUT})
3. From an external distributed voltage rail (V_{EXT})
4. From a shunt or series zener diode

In the *Functional Block Diagram*, capacitor C_{BOOST} and diode D2 supply the gate-drive current for the NMOS switch. Capacitor C_{BOOST} is charged via diode D2 by V_{IN}. During a normal switching cycle, when the internal NMOS control switch is off (T_{OFF}) (refer to Figure 11), V_{BOOST} equals V_{IN} minus the forward voltage of D2 (V_{FD2}), during which the current in the inductor (L) forward biases the Schottky diode D1 (V_{FD1}). Therefore the voltage stored across C_{BOOST} is

$$V_{BOOST} - V_{SW} = V_{IN} - V_{FD2} + V_{FD1} \quad (1)$$

When the NMOS switch turns on (T_{ON}), the switch pin rises to

$$V_{SW} = V_{IN} – (R_{DSON} \times I_L), \quad (2)$$

forcing V_{BOOST} to rise thus reverse biasing D2. The voltage at V_{BOOST} is then

$$V_{BOOST} = 2V_{IN} – (R_{DSON} \times I_L) – V_{FD2} + V_{FD1} \quad (3)$$

which is approximately

$$2 V_{IN} - 0.4 \text{ V} \quad (4)$$

for many applications. Thus the gate-drive voltage of the NMOS switch is approximately

Application Information (continued)

$$V_{IN} - 0.2\ V \quad (5)$$

An alternate method for charging C_{BOOST} is to connect D2 to the output as shown in Figure 12. The output voltage should be between 2.5 V and 5.5 V, so that proper gate voltage will be applied to the internal switch. In this circuit, C_{BOOST} provides a gate drive voltage that is slightly less than V_{OUT}.

In applications where both V_{IN} and V_{OUT} are greater than 5.5 V, or less than 3 V, C_{BOOST} cannot be charged directly from these voltages. If V_{IN} and V_{OUT} are greater than 5.5 V, C_{BOOST} can be charged from V_{IN} or V_{OUT} minus a zener voltage by placing a zener diode D3 in series with D2, as shown in Figure 13. When using a series zener diode from the input, ensure that the regulation of the input supply doesn't create a voltage that falls outside the recommended V_{BOOST} voltage.

$$(V_{INMAX} – V_{D3}) < 5.5\ V \quad (6)$$

$$(V_{INMIN} – V_{D3}) > 1.6\ V \quad (7)$$

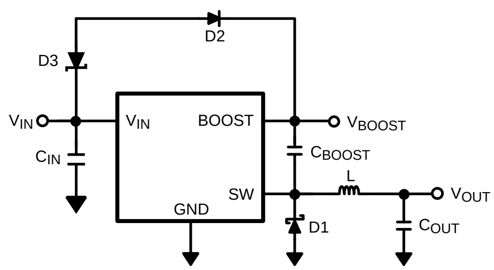


Figure 13. Zener Reduces Boost Voltage from V_{IN}

An alternative method is to place the zener diode D3 in a shunt configuration as shown in Figure 14. A small 350 mW to 500 mW 5.1 V zener in a SOT or SOD package can be used for this purpose. A small ceramic capacitor such as a 6.3 V, 0.1 µF capacitor (C4) should be placed in parallel with the zener diode. When the internal NMOS switch turns on, a pulse of current is drawn to charge the internal NMOS gate capacitance. The 0.1 µF parallel shunt capacitor ensures that the V_{BOOST} voltage is maintained during this time.

Resistor R3 should be chosen to provide enough RMS current to the zener diode (D3) and to the BOOST pin. A recommended choice for the zener current (I_{ZENER}) is 1 mA. The current I_{BOOST} into the BOOST pin supplies the gate current of the NMOS control switch and varies typically according to the following formula for the X - version:

$$I_{BOOST} = 0.49 \times (D + 0.54) \times (V_{ZENER} – V_{D2})\ mA \quad (8)$$

I_{BOOST} can be calculated for the Y version using the following:

$$I_{BOOST} = 0.20 \times (D + 0.54) \times (V_{ZENER} - V_{D2})\ \mu A \quad (9)$$

where D is the duty cycle, V_{ZENER} and V_{D2} are in volts, and I_{BOOST} is in milliamps. V_{ZENER} is the voltage applied to the anode of the boost diode (D2), and V_{D2} is the average forward voltage across D2. Note that this formula for I_{BOOST} gives typical current. For the worst case I_{BOOST}, increase the current by 40%. In that case, the worst case boost current will be

$$I_{BOOST\text{-}MAX} = 1.4 \times I_{BOOST} \quad (10)$$

R3 will then be given by

$$R3 = (V_{IN} - V_{ZENER}) / (1.4 \times I_{BOOST} + I_{ZENER}) \quad (11)$$

For example, using the X-version let V_{IN} = 10 V, V_{ZENER} = 5 V, V_{D2} = 0.7 V, I_{ZENER} = 1 mA, and duty cycle D = 50%. Then

$$I_{BOOST} = 0.49 \times (0.5 + 0.54) \times (5 - 0.7)\ mA = 2.19 mA \quad (12)$$

$$R3 = (10\ V - 5\ V) / (1.4 \times 2.19\ mA + 1\ mA) = 1.23\ k\Omega \quad (13)$$

Application Information (continued)

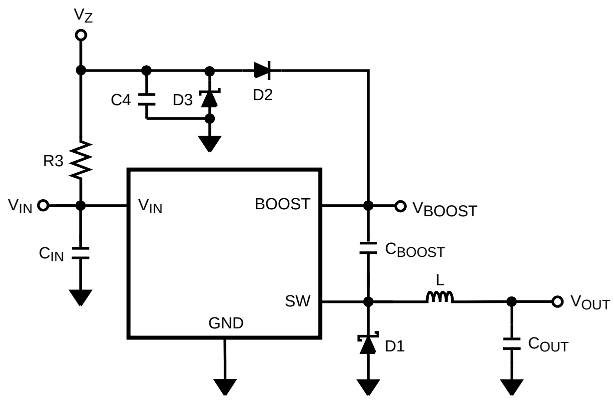


Figure 14. Boost Voltage Supplied from the Shunt Zener on V_{IN}

8.2 Typical Applications

8.2.1 LM2736X (1.6 MHz) V_{BOOST} Derived from V_{IN} 5 V to 1.5 V / 750 mA

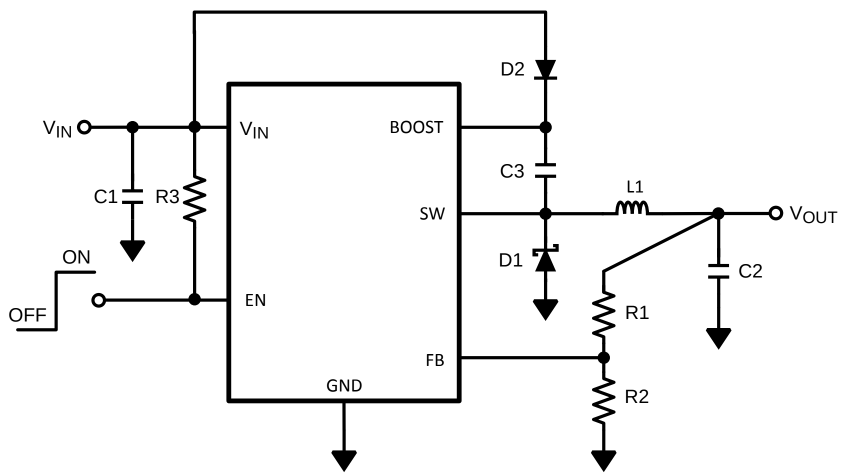


Figure 15. LM2736X (1.6 MHz) V_{BOOST} Derived from V_{IN} 5 V to 1.5 V / 750 mA

8.2.1.1 Design Requirements

Derive charge for V_{BOOST} from the input supply (V_{IN}). V_{BOOST} – V_{SW} should not exceed the maximum operating limit of 5.5 V.

8.2.1.2 Detailed Design Procedures

Table 1. Bill of Materials for Figure 15

PART ID	PART VALUE	PART NUMBER	MANUFACTURER
U1	750 mA Buck Regulator	LM2736X	TI
C1, Input Cap	10-µF, 6.3V, X5R	C3216X5ROJ106M	TDK
C2, Output Cap	10-µF, 6.3V, X5R	C3216X5ROJ106M	TDK
C3, Boost Cap	0.01-uF, 16V, X7R	C1005X7R1C103K	TDK
D1, Catch Diode	0.3 V_F Schottky 1 A, 10 VR	MBRM110L	ON Semi
D2, Boost Diode	1 V_F @ 50 mA Diode	1N4148W	Diodes, Inc.

Typical Applications (continued)

Table 1. Bill of Materials for Figure 15 (continued)

PART ID	PART VALUE	PART NUMBER	MANUFACTURER
L1	4.7-µH, 1.7 A,	VLCF4020T- 4R7N1R2	TDK
R1	2 kΩ, 1%	CRCW06032001F	Vishay
R2	10 kΩ, 1%	CRCW06031002F	Vishay
R3	100 kΩ, 1%	CRCW06031003F	Vishay

8.2.1.2.1 Inductor Selection

The Duty Cycle (D) can be approximated quickly using the ratio of output voltage (V_O) to input voltage (V_{IN}) as shown in Equation 14:

$$D = \frac{V_O}{V_{IN}} \tag{14}$$

The catch diode (D1) forward voltage drop and the voltage drop across the internal NMOS must be included to calculate a more accurate duty cycle. Use Equation 15 to Calculate D.

$$D = \frac{V_O + V_D}{V_{IN} + V_D - V_{SW}} \tag{15}$$

V_{SW} can be approximated by:

$$V_{SW} = I_O \times R_{DS(ON)} \tag{16}$$

The diode forward drop (V_D) can range from 0.3 V to 0.7 V depending on the quality of the diode. The lower V_D is, the higher the operating efficiency of the converter.

The inductor value determines the output ripple current. Lower inductor values decrease the size of the inductor, but increase the output ripple current. An increase in the inductor value will decrease the output ripple current. The ratio of ripple current (Δi_L) to output current (I_O) is optimized when it is set between 0.3 and 0.4 at 750 mA. The ratio r is defined in .

$$r = \frac{\Delta i_L}{I_O} \tag{17}$$

One must also ensure that the minimum current limit (1.0 A) is not exceeded, so the peak current in the inductor must be calculated. Use Equation 18 to calculate the peak current (I_{LPK}) in the inductor.

$$I_{LPK} = I_O + \Delta I_L/2 \tag{18}$$

If r = 0.7 at an output of 750 mA, the peak current in the inductor will be 1.0125 A. The minimum ensured current limit over all operating conditions is 1.0 A. One can either reduce r to 0.6 resulting in a 975 mA peak current, or make the engineering judgement that 12.5 mA over will be safe enough with a 1.5 A typical current limit and 6 sigma limits. When the designed maximum output current is reduced, the ratio r can be increased. At a current of 0.1 A, r can be made as high as 0.9. The ripple ratio can be increased at lighter loads because the net ripple is actually quite low, and if r remains constant the inductor value can be made quite large. Equation 19 is empirically developed for the maximum ripple ratio at any current below 2 A.

$$r = 0.387 \times I_{OUT}^{-0.3667} \tag{19}$$

Note that this is just a guideline.

The LM2736 device operates at frequencies allowing the use of ceramic output capacitors without compromising transient response. Ceramic capacitors allow higher inductor ripple without significantly increasing output ripple. See the *Output Capacitor* section for more details on calculating output voltage ripple.

Now that the ripple current or ripple ratio is determined, the inductance is calculated using Equation 20

$$L = \frac{V_O + V_D}{I_O \times r \times f_S} \times (1\text{-}D) \tag{20}$$

where f_s is the switching frequency and I_O is the output current. When selecting an inductor, make sure that it is capable of supporting the peak output current without saturating. Inductor saturation will result in a sudden reduction in inductance and prevent the regulator from operating correctly. Because of the speed of the internal current limit, the peak current of the inductor need only be specified for the required maximum output current. For example, if the designed maximum output current is 0.5 A and the peak current is 0.7 A, then the inductor should be specified with a saturation current limit of >0.7 A. There is no need to specify the saturation or peak current of the inductor at the 1.5 A typical switch current limit. The difference in inductor size is a factor of 5. Because of the operating frequency of the LM2736, ferrite based inductors are preferred to minimize core losses. This presents little restriction since the variety of ferrite based inductors is huge. Lastly, inductors with lower series resistance (DCR) will provide better operating efficiency. For recommended inductors see Example Circuits.

8.2.1.2.2 Input Capacitor

An input capacitor is necessary to ensure that V_{IN} does not drop excessively during switching transients. The primary specifications of the input capacitor are capacitance, voltage, RMS current rating, and ESL (Equivalent Series Inductance). The recommended input capacitance is 10-µF, although 4.7-µF works well for input voltages below 6 V. The input voltage rating is specifically stated by the capacitor manufacturer. Make sure to check any recommended deratings and also verify if there is any significant change in capacitance at the operating input voltage and the operating temperature. The input capacitor maximum RMS input current rating ($I_{RMS\text{-}IN}$) must be greater than:

$$I_{RMS\text{-}IN} = I_O \times \sqrt{D \times \left(1 - D + \frac{r^2}{12}\right)} \tag{21}$$

It can be shown from the above equation that maximum RMS capacitor current occurs when D = 0.5. Always calculate the RMS at the point where the duty cycle, D, is closest to 0.5. The ESL of an input capacitor is usually determined by the effective cross sectional area of the current path. A large leaded capacitor will have high ESL and a 0805 ceramic chip capacitor will have very low ESL. At the operating frequencies of the LM2736, certain capacitors may have an ESL so large that the resulting impedance (2πfL) will be higher than that required to provide stable operation. As a result, surface mount capacitors are strongly recommended. Sanyo POSCAP, Tantalum or Niobium, Panasonic SP or Cornell Dubilier ESR, and multilayer ceramic capacitors (MLCC) are all good choices for both input and output capacitors and have very low ESL. For MLCCs it is recommended to use X7R or X5R dielectrics. Consult capacitor manufacturer datasheet to see how rated capacitance varies over operating conditions.

8.2.1.2.3 Output Capacitor

The output capacitor is selected based upon the desired output ripple and transient response. The initial current of a load transient is provided mainly by the output capacitor. The output ripple of the converter is:

$$\Delta V_O = \Delta i_L \times \left(R_{ESR} + \frac{1}{8 \times f_S \times C_O}\right) \tag{22}$$

When using MLCCs, the ESR is typically so low that the capacitive ripple may dominate. When this occurs, the output ripple will be approximately sinusoidal and 90° phase shifted from the switching action. Given the availability and quality of MLCCs and the expected output voltage of designs using the LM2736, there is really no need to review any other capacitor technologies. Another benefit of ceramic capacitors is their ability to bypass high frequency noise. A certain amount of switching edge noise will couple through parasitic capacitances in the inductor to the output. A ceramic capacitor will bypass this noise while a tantalum will not. Since the output capacitor is one of the two external components that control the stability of the regulator control loop, most applications will require a minimum at 10-µF of output capacitance. Capacitance can be increased significantly with little detriment to the regulator stability. Like the input capacitor, recommended multilayer ceramic capacitors are X7R or X5R. Again, verify actual capacitance at the desired operating voltage and temperature.

Check the RMS current rating of the capacitor. The RMS current rating of the capacitor chosen must also meet the following condition:

$$I_{RMS\text{-}OUT} = I_O \times \frac{r}{\sqrt{12}} \tag{23}$$

8.2.1.2.4 Catch Diode

The catch diode (D1) conducts during the switch off-time. A Schottky diode is recommended for its fast switching times and low forward voltage drop. The catch diode should be chosen so that its current rating is greater than:

$$I_{D1} = I_O \times (1\text{-}D) \quad (24)$$

The reverse breakdown rating of the diode must be at least the maximum input voltage plus appropriate margin. To improve efficiency choose a Schottky diode with a low forward voltage drop.

8.2.1.2.5 Boost Diode

A standard diode such as the 1N4148 type is recommended. For V_{BOOST} circuits derived from voltages less than 3.3 V, a small-signal Schottky diode is recommended for greater efficiency. A good choice is the BAT54 small signal diode.

8.2.1.2.6 Boost Capacitor

A ceramic 0.01-µF capacitor with a voltage rating of at least 16 V is sufficient. The X7R and X5R MLCCs provide the best performance.

8.2.1.2.7 Output Voltage

The output voltage is set using the following equation where R2 is connected between the FB pin and GND, and R1 is connected between V_O and the FB pin. A good value for R2 is 10 kΩ.

$$R1 = \left(\frac{V_O}{V_{REF}} - 1\right) \times R2 \quad (25)$$

8.2.1.3 Application Curves

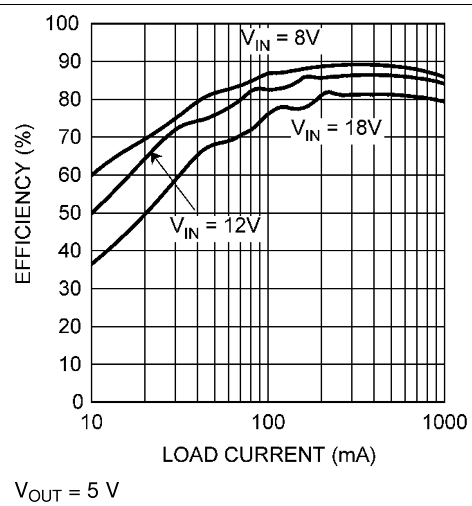


Figure 16. Efficiency vs Load Current - "X"

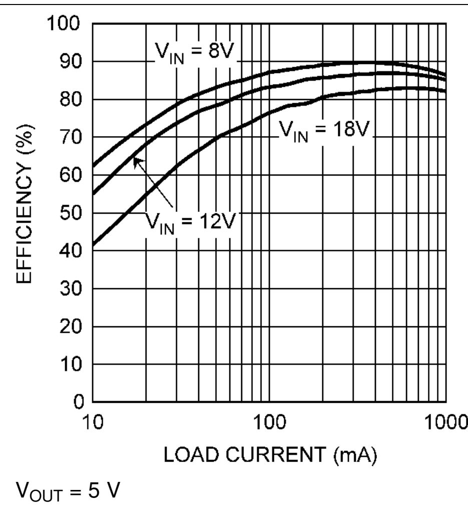
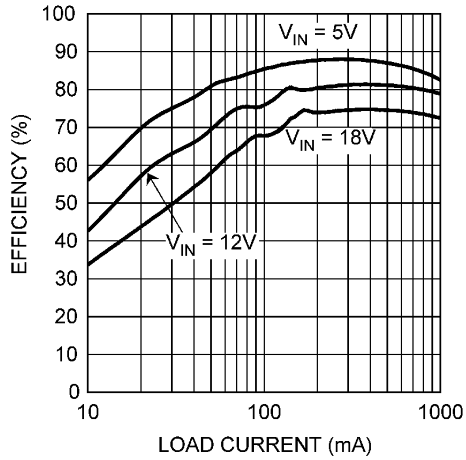
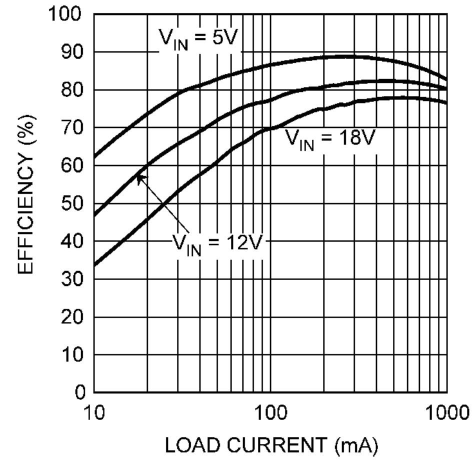


Figure 17. Efficiency vs Load Current - "Y"



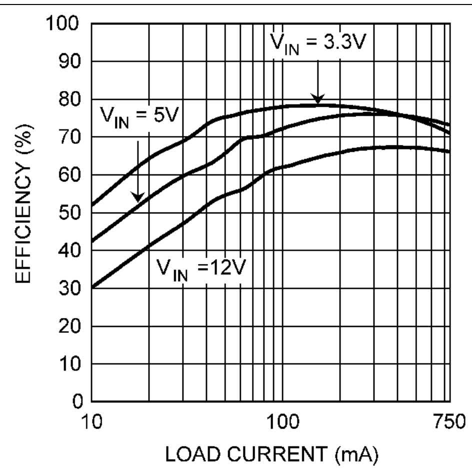
V_{OUT} = 3.3 V

Figure 18. Efficiency vs Load Current - "X"



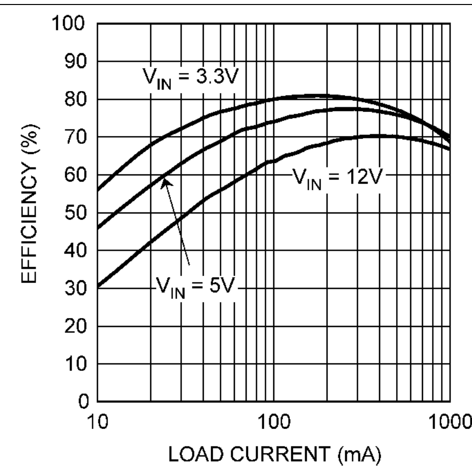
V_{OUT} = 3.3 V

Figure 19. Efficiency vs Load Current - "Y"



V_{OUT} = 1.5 V

Figure 20. Efficiency vs Load Current - "X"



V_{OUT} = 1.5 V

Figure 21. Efficiency vs Load Current - "Y"

8.2.2 LM2736X (1.6 MHz) V_{BOOST} Derived from V_{OUT} 12 V to 3.3 V / 750 mA

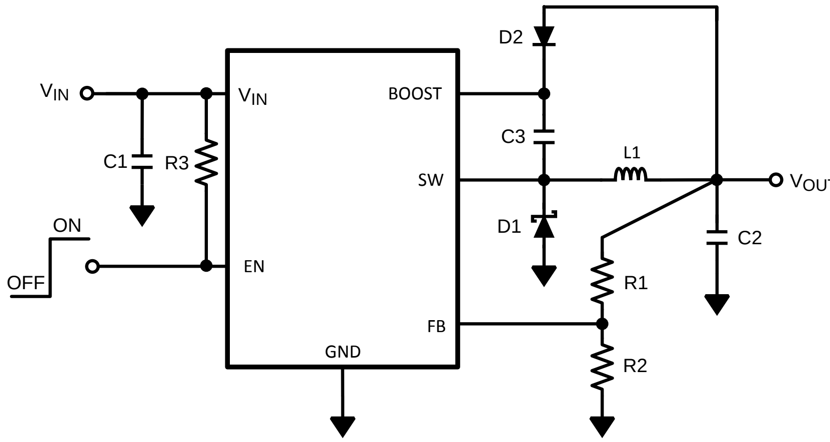


Figure 22. LM2736X (1.6 MHz) V_{BOOST} Derived from V_{OUT} 12 V to 3.3 V / 750 mA

8.2.2.1 Design Requirements

Derive charge for V_{BOOST} from the output voltage, (V_{OUT}). The output voltage should be between 2.5V and 5.5V.

8.2.2.2 Detailed Design Procedures

Table 2. Bill of Materials for Figure 22

PART ID	PART VALUE	PART NUMBER	MANUFACTURER
U1	750mA Buck Regulator	LM2736X	TI
C1, Input Cap	10µF, 25V, X7R	C3225X7R1E106M	TDK
C2, Output Cap	22µF, 6.3V, X5R	C3216X5ROJ226M	TDK
C3, Boost Cap	0.01µF, 16V, X7R	C1005X7R1C103K	TDK
D1, Catch Diode	0.34V_F Schottky 1A, 30VR	SS1P3L	Vishay
D2, Boost Diode	30V, 200 mA Schottky	BAT54	Diodes Inc.
L1	4.7µH, 1.7A,	VLCF4020T- 4R7N1R2	TDK
R1	16.5kΩ, 1%	CRCW06031652F	Vishay
R2	10.0 kΩ, 1%	CRCW06031002F	Vishay
R3	100kΩ, 1%	CRCW06031003F	Vishay

Please refer to *Detailed Design Procedures*.

8.2.2.3 Application Curves

Please refer to *Application Curves*

8.2.3 LM2736X (1.6 MHz) V_{BOOST} Derived from V_{SHUNT} 18 V to 1.5 V / 750 mA

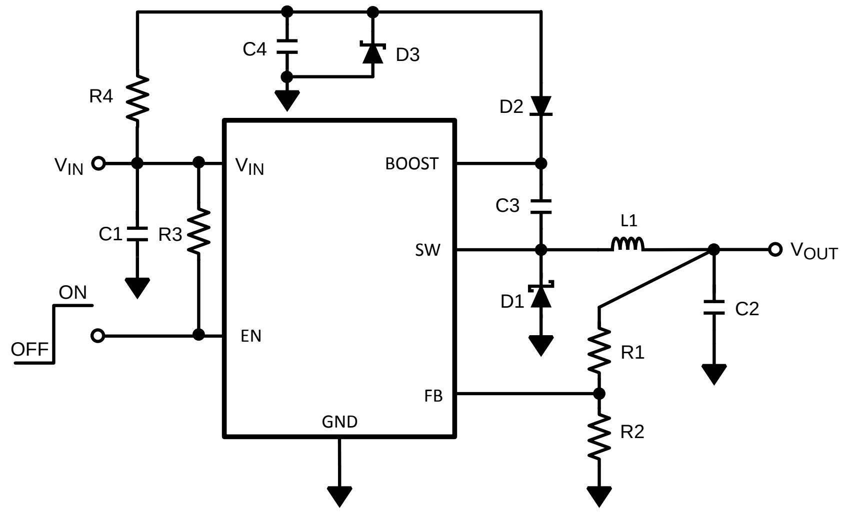


Figure 23. LM2736X (1.6 MHz) V_{BOOST} Derived from V_{SHUNT} 18 V to 1.5 V / 750 mA

8.2.3.1 Design Requirements

An alternative method when V_{IN} is greater than 5.5V is to place the zener diode D3 in a shunt configuration. A small 350 mW to 500 mW 5.1 V zener in a SOT or SOD package can be used for this purpose. A small ceramic capacitor such as a 6.3 V, 0.1 µF capacitor (C4) should be placed in parallel with the zener diode. When the internal NMOS switch turns on, a pulse of current is drawn to charge the internal NMOS gate capacitance. The 0.1 µF parallel shunt capacitor ensures that the V_{BOOST} voltage is maintained during this time

8.2.3.2 Detailed Design Procedure

Table 3. Bill of Materials for Figure 23

PART ID	PART VALUE	PART NUMBER	MANUFACTURER
U1	750mA Buck Regulator	LM2736X	TI
C1, Input Cap	10µF, 25V, X7R	C3225X7R1E106M	TDK
C2, Output Cap	22µF, 6.3V, X5R	C3216X5ROJ226M	TDK
C3, Boost Cap	0.01µF, 16V, X7R	C1005X7R1C103K	TDK
C4, Shunt Cap	0.1µF, 6.3V, X5R	C1005X5R0J104K	TDK
D1, Catch Diode	0.4V_F Schottky 1A, 30VR	SS1P3L	Vishay
D2, Boost Diode	1V_F @ 50mA Diode	1N4148W	Diodes, Inc.
D3, Zener Diode	5.1V 250Mw SOT	BZX84C5V1	Vishay
L1	6.8µH, 1.6A,	SLF7032T-6R8M1R6	TDK
R1	2kΩ, 1%	CRCW06032001F	Vishay
R2	10kΩ, 1%	CRCW06031002F	Vishay
R3	100kΩ, 1%	CRCW06031003F	Vishay
R4	4.12kΩ, 1%	CRCW06034121F	Vishay

Please refer to *Detailed Design Procedures*.

8.2.3.3 Application Curves

Please refer to *Application Curves*.

8.2.4 LM2736X (1.6 MHz) V_{BOOST} Derived from Series Zener Diode (V_{IN}) 15 V to 1.5 V / 750 mA

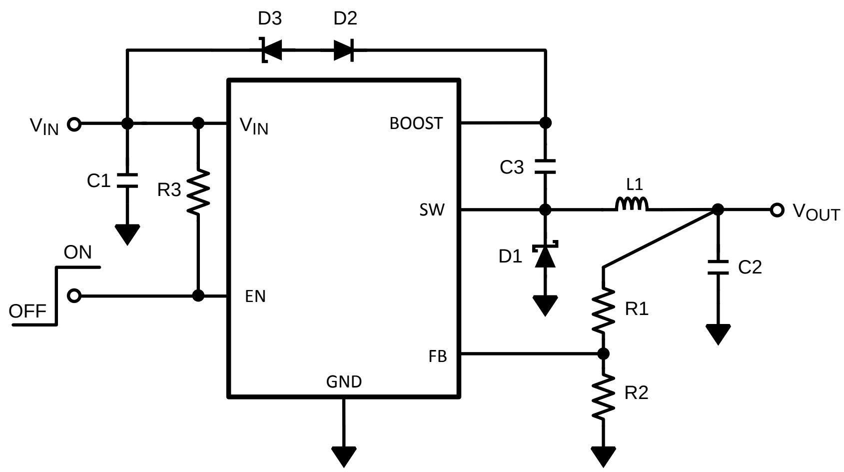


Figure 24. LM2736X (1.6 MHz) V_{BOOST} Derived from Series Zener Diode (V_{IN}) 15 V to 1.5 V / 750 mA

8.2.4.1 Design Requirements

In applications where both V_{IN} and V_{OUT} are greater than 5.5 V, or less than 3 V, C_{BOOST} cannot be charged directly from these voltages. If V_{IN} is greater than 5.5 V, C_{BOOST} can be charged from V_{IN} minus a zener voltage by placing a zener diode D3 in series with D2. When using a series zener diode from the input, ensure that the regulation of the input supply doesn't create a voltage that falls outside the recommended V_{BOOST} voltage.

$$(V_{INMAX} - V_{D3}) < 5.5\ V \quad (26)$$

$$(V_{INMIN} - V_{D3}) > 1.6\ V \quad (27)$$

8.2.4.2 Detailed Design Procedure

Table 4. Bill of Materials for Figure 24

PART ID	PART VALUE	PART NUMBER	MANUFACTURER
U1	750 mA Buck Regulator	LM2736X	TI
C1, Input Cap	10-µF, 25 V, X7R	C3225X7R1E106M	TDK
C2, Output Cap	22-µF, 6.3 V, X5R	C3216X5ROJ226M	TDK
C3, Boost Cap	0.01-µF, 16 V, X7R	C1005X7R1C103K	TDK
D1, Catch Diode	0.4 V_F Schottky 1 A, 30VR	SS1P3L	Vishay
D2, Boost Diode	1V_F @ 50 mA Diode	1N4148W	Diodes, Inc.
D3, Zener Diode	11 V 350 Mw SOT	BZX84C11T	Diodes, Inc.
L1	6.8µH, 1.6 A,	SLF7032T-6R8M1R6	TDK
R1	2 kΩ, 1%	CRCW06032001F	Vishay
R2	10 kΩ, 1%	CRCW06031002F	Vishay
R3	100 kΩ, 1%	CRCW06031003F	Vishay

Please refer to *Detailed Design Procedures*.

8.2.4.3 Application Curves

Please refer to *Application Curves*

8.2.5 LM2736X (1.6 MHz) V_{BOOST} Derived from Series Zener Diode (V_{OUT}) 15 V to 9 V / 750 mA

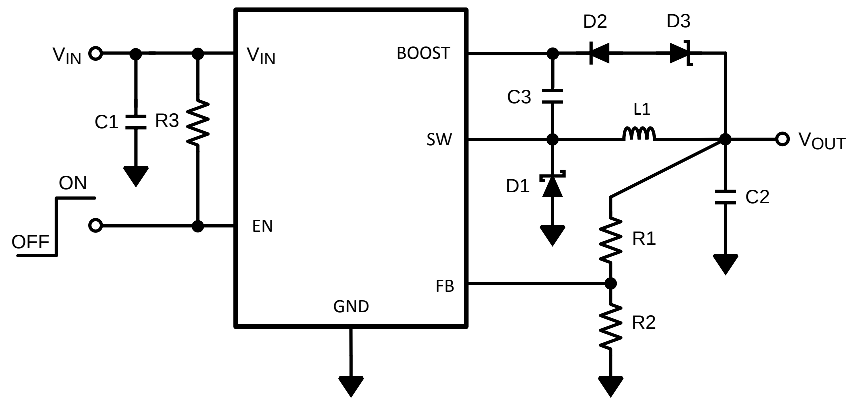


Figure 25.

8.2.5.1 Design Requirements

In applications where both V_{IN} and V_{OUT} are greater than 5.5 V, or less than 3 V, C_{BOOST} cannot be charged directly from these voltages. If V_{IN} and V_{OUT} are greater than 5.5 V, C_{BOOST} can be charged from V_{OUT} minus a zener voltage by placing a zener diode D3 in series with D2.

8.2.5.2 Detailed Design Procedure

Table 5. Bill of Materials for Figure 25

PART ID	PART VALUE	PART NUMBER	MANUFACTURER
U1	750mA Buck Regulator	LM2736X	TI
C1, Input Cap	10µF, 25V, X7R	C3225X7R1E106M	TDK
C2, Output Cap	22µF, 16V, X5R	C3216X5R1C226M	TDK
C3, Boost Cap	0.01µF, 16V, X7R	C1005X7R1C103K	TDK
D1, Catch Diode	0.4V_F Schottky 1A, 30VR	SS1P3L	Vishay
D2, Boost Diode	1V_F @ 50mA Diode	1N4148W	Diodes, Inc.
D3, Zener Diode	4.3V 350mw SOT	BZX84C4V3	Diodes, Inc.
L1	6.8µH, 1.6A,	SLF7032T-6R8M1R6	TDK
R1	61.9kΩ, 1%	CRCW06036192F	Vishay
R2	10kΩ, 1%	CRCW06031002F	Vishay
R3	100kΩ, 1%	CRCW06031003F	Vishay

Please refer to *Detailed Design Procedures*.

8.2.5.3 Application Curves

Please refer to *Application Curves*

8.2.6 LM2736Y (550 kHz) V_{BOOST} Derived from V_{IN} 5 V to 1.5 V / 750 mA

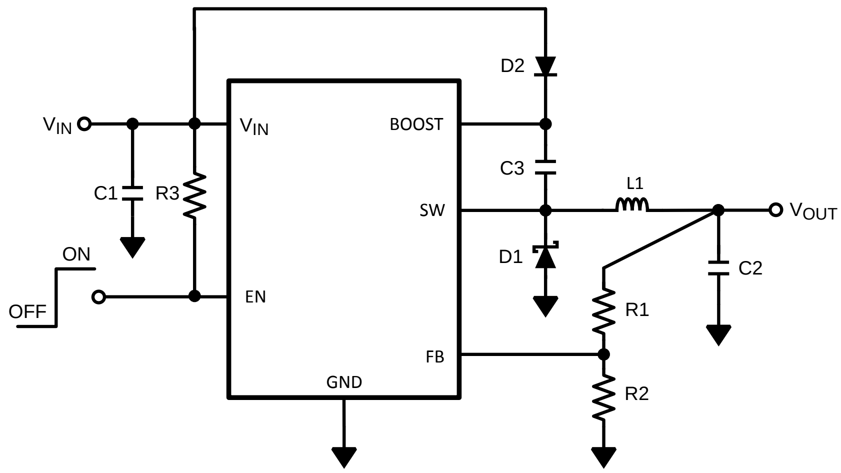


Figure 26. LM2736Y (550 kHz) V_{BOOST} Derived from V_{IN} 5 V to 1.5 V / 750 mA

8.2.6.1 Design Requirements

Derive charge for V_{BOOST} from the input voltage, (V_{IN}). V_{BOOST} should be greater than 2.5 V above V_{SW} for best efficiency. V_{BOOST} – V_{SW} should not exceed the maximum operating limit of 5.5 V.

8.2.6.2 Detailed Design Procedure

Table 6. Bill of Materials for Figure 26

PART ID	PART VALUE	PART NUMBER	MANUFACTURER
U1	750mA Buck Regulator	LM2736Y	TI
C1, Input Cap	10µF, 6.3V, X5R	C3216X5ROJ106M	TDK
C2, Output Cap	22µF, 6.3V, X5R	C3216X5ROJ226M	TDK
C3, Boost Cap	0.01µF, 16V, X7R	C1005X7R1C103K	TDK
D1, Catch Diode	0.3V_F Schottky 1A, 10VR	MBRM110L	ON Semi
D2, Boost Diode	1V_F @ 50mA Diode	1N4148W	Diodes, Inc.
L1	10µH, 1.6A,	SLF7032T-100M1R4	TDK
R1	2kΩ, 1%	CRCW06032001F	Vishay
R2	10kΩ, 1%	CRCW06031002F	Vishay
R3	100kΩ, 1%	CRCW06031003F	Vishay

Please refer to *Detailed Design Procedures*.

8.2.6.3 Application Curves

Please refer to *Application Curves*.

8.2.7 LM2736Y (550 kHz) V_{BOOST} Derived from V_{OUT} 12 V to 3.3 V / 750 mA

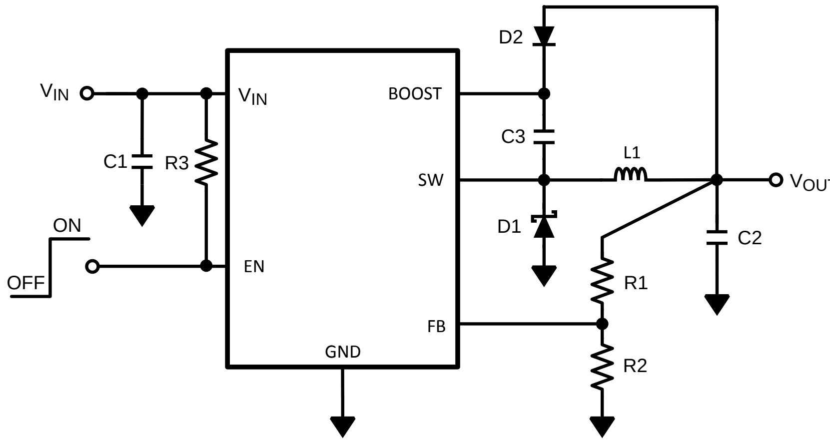


Figure 27. LM2736Y (550 kHz) V_{BOOST} Derived from V_{OUT} 12 V to 3.3 V / 750 mA

8.2.7.1 Design Requirements

Derive charge for V_{BOOST} from the output voltage, (V_{OUT}). The output voltage should be between 2.5V and 5.5V.

8.2.7.2 Detailed Design Procedure

Table 7. Bill of Materials for Figure 27

PART ID	PART VALUE	PART NUMBER	MANUFACTURER
U1	750mA Buck Regulator	LM2736Y	TI
C1, Input Cap	10µF, 25V, X7R	C3225X7R1E106M	TDK
C2, Output Cap	22µF, 6.3V, X5R	C3216X5ROJ226M	TDK
C3, Boost Cap	0.01µF, 16V, X7R	C1005X7R1C103K	TDK
D1, Catch Diode	0.34V_F Schottky 1A, 30VR	SS1P3L	Vishay
D2, Boost Diode	30V, 200 mA Schottky	BAT54	Diodes Inc.
L1	10µH, 1.6A,	SLF7032T-100M1R4	TDK
R1	16.5kΩ, 1%	CRCW06031652F	Vishay
R2	10.0 kΩ, 1%	CRCW06031002F	Vishay
R3	100kΩ, 1%	CRCW06031003F	Vishay

Please refer to *Detailed Design Procedures*.

8.2.7.3 Application Curves

Please refer to *Application Curves*.

8.2.8 LM2736Y (550 kHz) V_{BOOST} Derived from V_{SHUNT} 18 V to 1.5 V / 750 mA

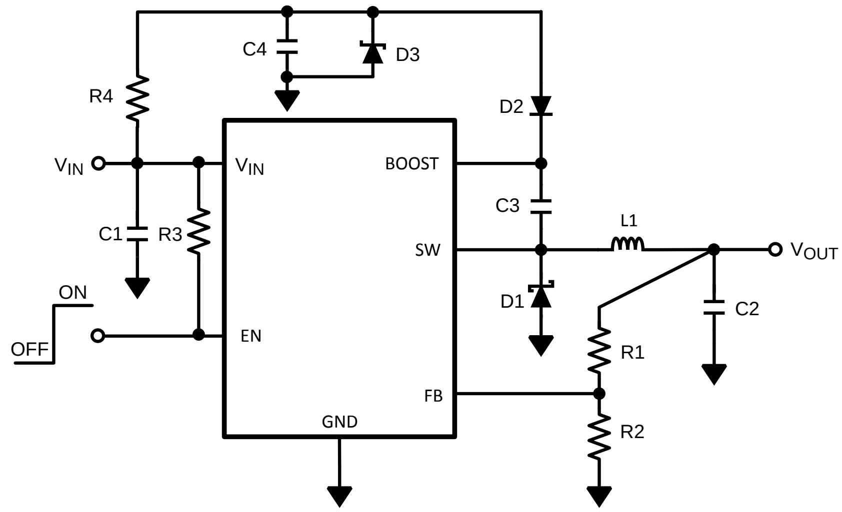


Figure 28. LM2736Y (550 kHz) V_{BOOST} Derived from V_{SHUNT} 18 V to 1.5 V / 750 mA

8.2.8.1 Design Requirements

An alternative method when V_{IN} is greater than 5.5V is to place the zener diode D3 in a shunt configuration. A small 350 mW to 500 mW 5.1 V zener in a SOT or SOD package can be used for this purpose. A small ceramic capacitor such as a 6.3 V, 0.1 µF capacitor (C4) should be placed in parallel with the zener diode. When the internal NMOS switch turns on, a pulse of current is drawn to charge the internal NMOS gate capacitance. The 0.1 µF parallel shunt capacitor ensures that the V_{BOOST} voltage is maintained during this time.

8.2.8.2 Detailed Design Procedure

Table 8. Bill of Materials for Figure 28

PART ID	PART VALUE	PART NUMBER	MANUFACTURER
U1	750mA Buck Regulator	LM2736Y	TI
C1, Input Cap	10µF, 25V, X7R	C3225X7R1E106M	TDK
C2, Output Cap	22µF, 6.3V, X5R	C3216X5ROJ226M	TDK
C3, Boost Cap	0.01µF, 16V, X7R	C1005X7R1C103K	TDK
C4, Shunt Cap	0.1µF, 6.3V, X5R	C1005X5R0J104K	TDK
D1, Catch Diode	0.4V_F Schottky 1A, 30VR	SS1P3L	Vishay
D2, Boost Diode	1V_F @ 50mA Diode	1N4148W	Diodes, Inc.
D3, Zener Diode	5.1V 250Mw SOT	BZX84C5V1	Vishay
L1	15µH, 1.5A	SLF7045T-150M1R5	TDK
R1	2kΩ, 1%	CRCW06032001F	Vishay
R2	10kΩ, 1%	CRCW06031002F	Vishay
R3	100kΩ, 1%	CRCW06031003F	Vishay
R4	4.12kΩ, 1%	CRCW06034121F	Vishay

Please refer to *Detailed Design Procedures*.

8.2.8.3 Application Curves

Please refer to *Application Curves*.

8.2.9 LM2736Y (550 kHz) V_{BOOST} Derived from Series Zener Diode (V_{IN}) 15 V to 1.5 V / 750 mA

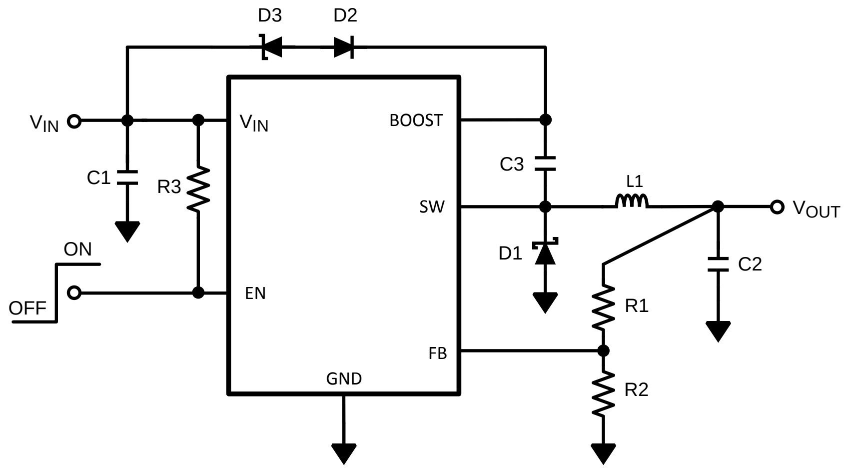


Figure 29. M2736Y (550 kHz) V_{BOOST} Derived from Series Zener Diode (V_{IN}) 15 V to 1.5 V / 750 mA

8.2.9.1 Design Requirements

In applications where both V_{IN} and V_{OUT} are greater than 5.5 V, or less than 3 V, C_{BOOST} cannot be charged directly from these voltages. If V_{IN} is greater than 5.5 V, C_{BOOST} can be charged from V_{IN} minus a zener voltage by placing a zener diode D3 in series with D2. When using a series zener diode from the input, ensure that the regulation of the input supply doesn't create a voltage that falls outside the recommended V_{BOOST} voltage.

$$(V_{INMAX} - V_{D3}) < 5.5\text{ V} \quad (28)$$

$$(V_{INMIN} - V_{D3}) > 1.6\text{ V} \quad (29)$$

8.2.9.2 Detailed Design Procedure

Table 9. Bill of Materials for Figure 29

PART ID	PART VALUE	PART NUMBER	MANUFACTURER
U1	750mA Buck Regulator	LM2736Y	TI
C1, Input Cap	10µF, 25V, X7R	C3225X7R1E106M	TDK
C2, Output Cap	22µF, 6.3V, X5R	C3216X5ROJ226M	TDK
C3, Boost Cap	0.01µF, 16V, X7R	C1005X7R1C103K	TDK
D1, Catch Diode	0.4V_F Schottky 1A, 30VR	SS1P3L	Vishay
D2, Boost Diode	1V_F @ 50mA Diode	1N4148W	Diodes, Inc.
D3, Zener Diode	11V 350Mw SOT	BZX84C11T	Diodes, Inc.
L1	15µH, 1.5A,	SLF7045T-150M1R5	TDK
R1	2kΩ, 1%	CRCW06032001F	Vishay
R2	10kΩ, 1%	CRCW06031002F	Vishay
R3	100kΩ, 1%	CRCW06031003F	Vishay

Please refer to *Detailed Design Procedures*.

8.2.9.3 Application Curves

Please refer to *Application Curves*.

8.2.10 LM2736Y (550 kHz) V_{BOOST} Derived from Series Zener Diode (V_{OUT}) 15 V to 9 V / 750 mA

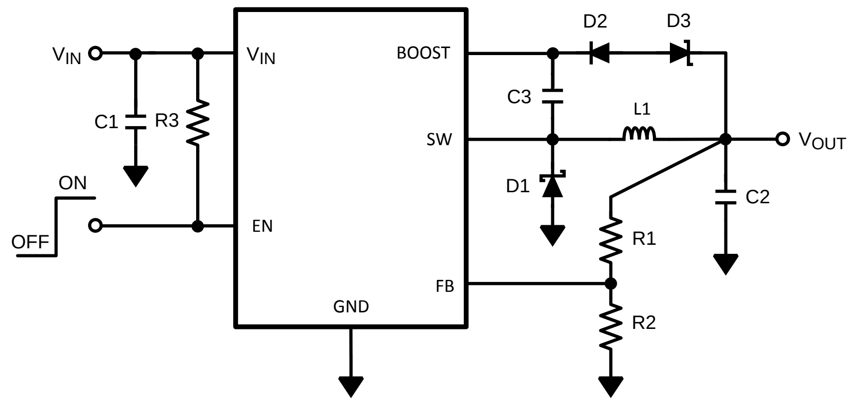


Figure 30. LM2736Y (550 kHz) V_{BOOST} Derived from Series Zener Diode (V_{OUT}) 15 V to 9 V / 750 mA

8.2.10.1 Design Requirements

In applications where both V_{IN} and V_{OUT} are greater than 5.5 V, or less than 3 V, C_{BOOST} cannot be charged directly from these voltages. If V_{IN} and V_{OUT} are greater than 5.5 V, C_{BOOST} can be charged from V_{OUT} minus a zener voltage by placing a zener diode D3 in series with D2.

8.2.10.2 Detailed Design Procedure

Table 10. Bill of Materials for Figure 30

PART ID	PART VALUE	PART NUMBER	MANUFACTURER
U1	750 mA Buck Regulator	LM2736Y	TI
C1, Input Cap	10-µF, 25 V, X7R	C3225X7R1E106M	TDK
C2, Output Cap	22-µF, 16 V, X5R	C3216X5R1C226M	TDK
C3, Boost Cap	0.01-µF, 16 V, X7R	C1005X7R1C103K	TDK
D1, Catch Diode	0.4 V_F Schottky 1 A, 30 VR	SS1P3L	Vishay
D2, Boost Diode	1 V_F @ 50 mA Diode	1N4148W	Diodes, Inc.
D3, Zener Diode	4.3 V 350 mw SOT	BZX84C4V3	Diodes, Inc.
L1	22 µH, 1.4 A,	SLF7045T-220M1R3-1PF	TDK
R1	61.9 kΩ, 1%	CRCW06036192F	Vishay
R2	10 kΩ, 1%	CRCW06031002F	Vishay
R3	100 kΩ, 1%	CRCW06031003F	Vishay

Please refer to *Detailed Design Procedures*.

8.2.10.3 Application Curves

Please refer to *Application Curves*.

9 Power Supply Recommendations

Input voltage is rated as 3 V to 18 V however care should be taken in certain circuit configurations eg. V_{BOOST} derived from V_{IN} where the requirement that V_{BOOST} - V_{SW} < 5.5 V should be observed. Also for best efficiency V_{BOOST} should be at least 2.5 V above V_{SW}.

The voltage on the Enable pin should not exceed V_{IN} by more than 0.3 V.

10 Layout

10.1 Layout Guidelines

When planning layout there are a few things to consider when trying to achieve a clean, regulated output. The most important consideration when completing the layout is the close coupling of the GND connections of the C_{IN} capacitor and the catch diode D1. These ground ends should be close to one another and be connected to the GND plane with at least two through-holes. Place these components as close to the IC as possible. Next in importance is the location of the GND connection of the C_{OUT} capacitor, which should be near the GND connections of C_{IN} and D1.

There should be a continuous ground plane on the bottom layer of a two-layer board except under the switching node island.

The FB pin is a high impedance node and care should be taken to make the FB trace short to avoid noise pickup and inaccurate regulation. The feedback resistors should be placed as close as possible to the IC, with the GND of R2 placed as close as possible to the GND of the IC. The V_{OUT} trace to R1 should be routed away from the inductor and any other traces that are switching.

High AC currents flow through the V_{IN}, SW and V_{OUT} traces, so they should be as short and wide as possible. However, making the traces wide increases radiated noise, so the designer must make this trade-off. Radiated noise can be decreased by choosing a shielded inductor.

The remaining components should also be placed as close as possible to the IC. Please see Application Note AN-1229 SNVA054 for further considerations and the LM2736 device demo board as an example of a four-layer layout.

10.2 Layout Example

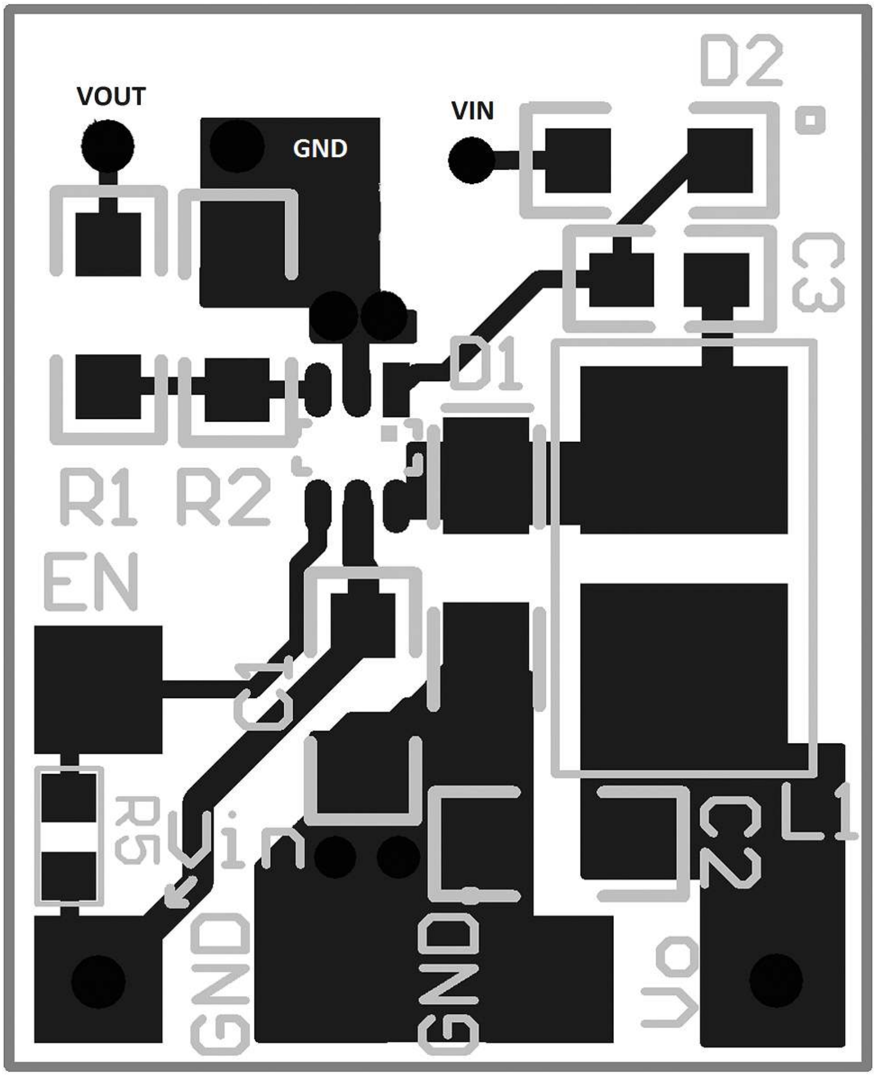


Figure 31. Top Layer

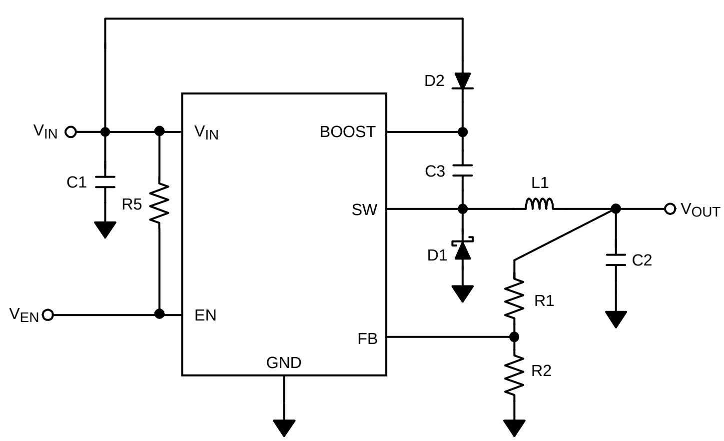


Figure 32. Layout Schematic

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

- *AN-1229 SIMPLE SWITCHER® PCB Layout Guidelines* SNVA054

11.3 Trademarks

WEBENCH, SIMPLE SWITCHER are registered trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM2736XMK	NRND	SOT-23-THIN	DDC	6	1000	TBD	Call TI	Call TI	-40 to 125	SHAB	
LM2736XMK/NOPB	ACTIVE	SOT-23-THIN	DDC	6	1000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	SHAB	Samples
LM2736XMKX/NOPB	ACTIVE	SOT-23-THIN	DDC	6	3000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	SHAB	Samples
LM2736YMK	NRND	SOT-23-THIN	DDC	6	1000	TBD	Call TI	Call TI	-40 to 125	SHBB	
LM2736YMK/NOPB	ACTIVE	SOT-23-THIN	DDC	6	1000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	SHBB	Samples
LM2736YMKX/NOPB	ACTIVE	SOT-23-THIN	DDC	6	3000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	SHBB	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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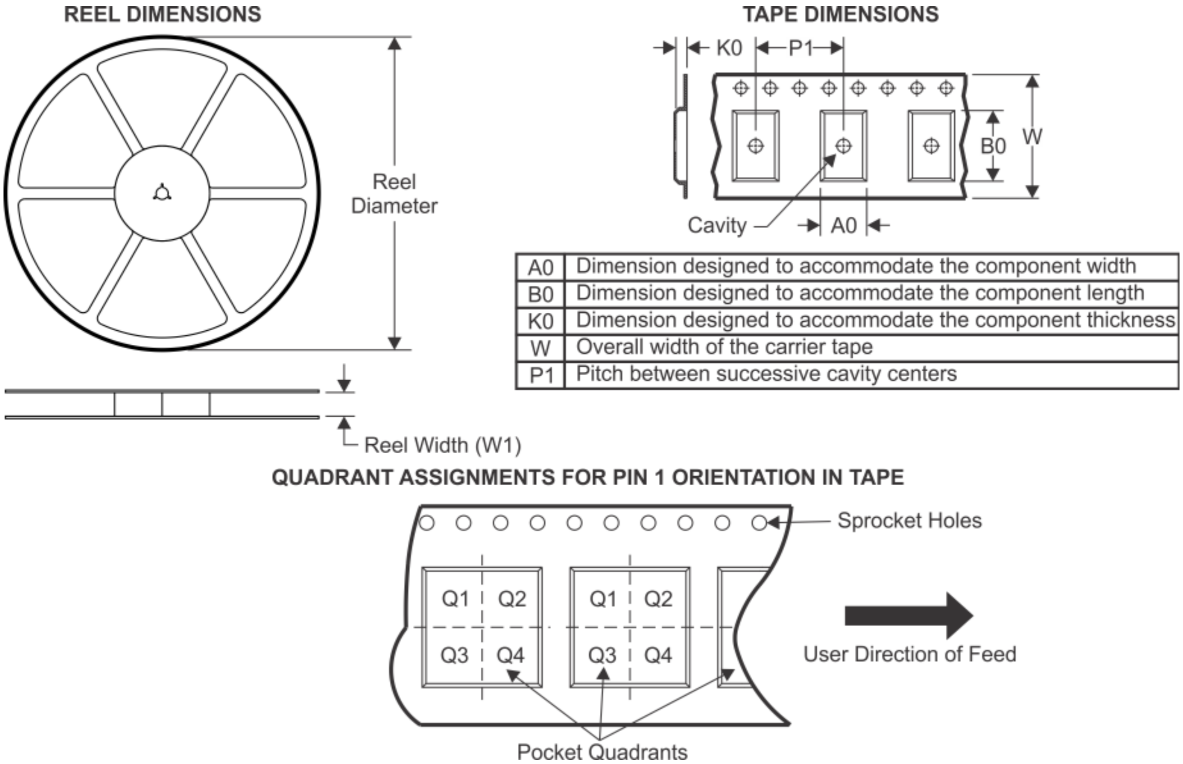
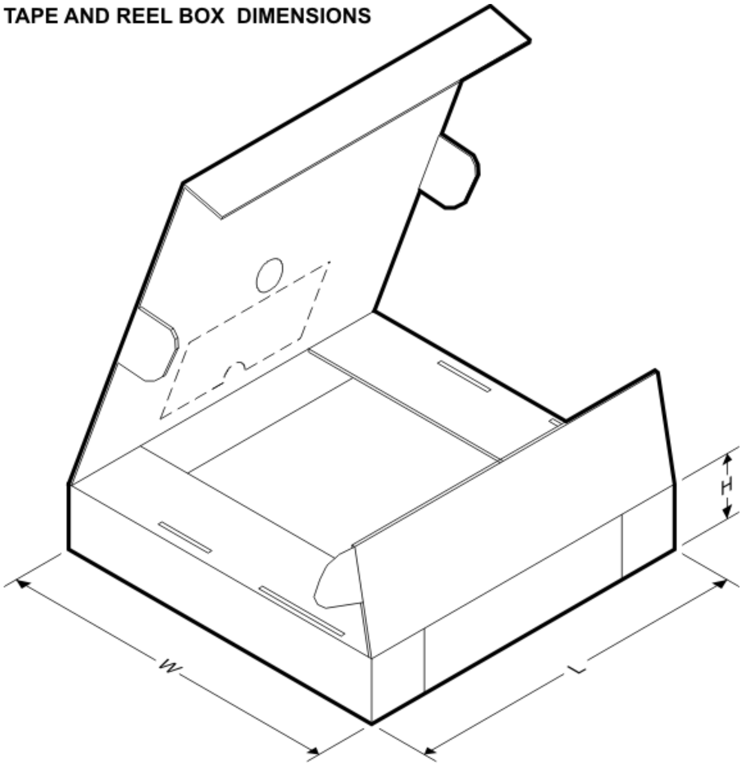
TAPE AND REEL INFORMATION



*All dimensions are nominal

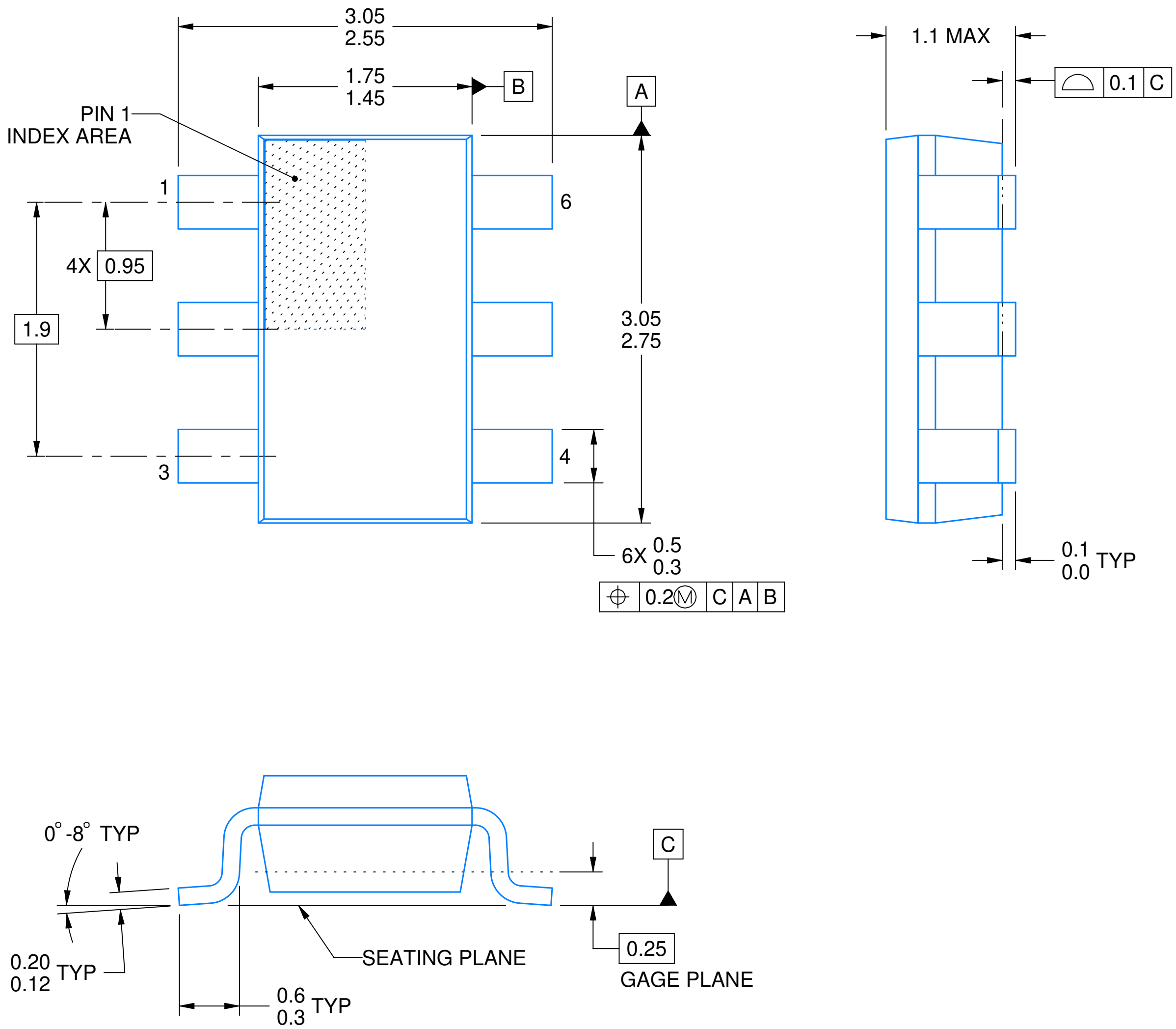
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM2736XMK	SOT-23-THIN	DDC	6	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM2736XMK/NOPB	SOT-23-THIN	DDC	6	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM2736XMKX/NOPB	SOT-23-THIN	DDC	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM2736YMK	SOT-23-THIN	DDC	6	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM2736YMK/NOPB	SOT-23-THIN	DDC	6	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM2736YMKX/NOPB	SOT-23-THIN	DDC	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM2736XMK	SOT-23-THIN	DDC	6	1000	210.0	185.0	35.0
LM2736XMK/NOPB	SOT-23-THIN	DDC	6	1000	210.0	185.0	35.0
LM2736XMKX/NOPB	SOT-23-THIN	DDC	6	3000	210.0	185.0	35.0
LM2736YMK	SOT-23-THIN	DDC	6	1000	210.0	185.0	35.0
LM2736YMK/NOPB	SOT-23-THIN	DDC	6	1000	210.0	185.0	35.0
LM2736YMKX/NOPB	SOT-23-THIN	DDC	6	3000	210.0	185.0	35.0



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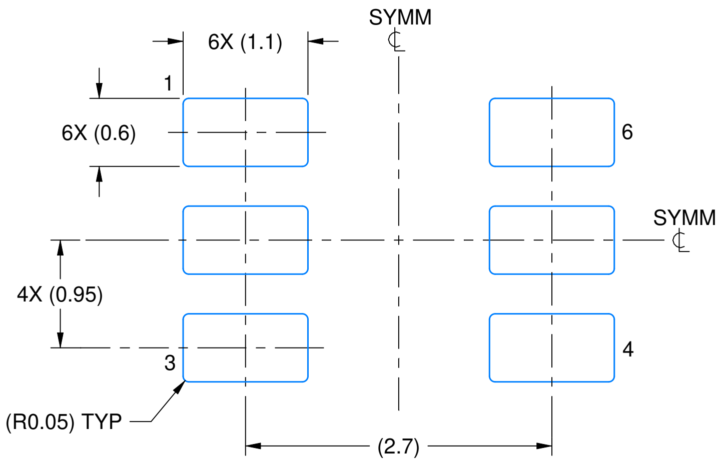
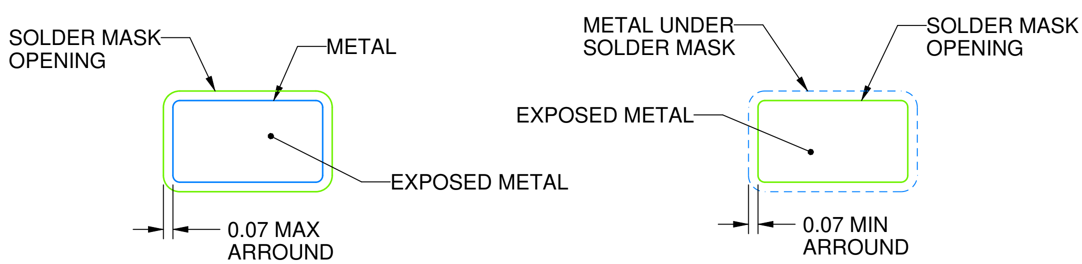
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-193.



LAND PATTERN EXAMPLE
EXPLOSED METAL SHOWN
SCALE:15X



NON SOLDER MASK DEFINED

SOLDER MASK DEFINED

SOLDERMASK DETAILS

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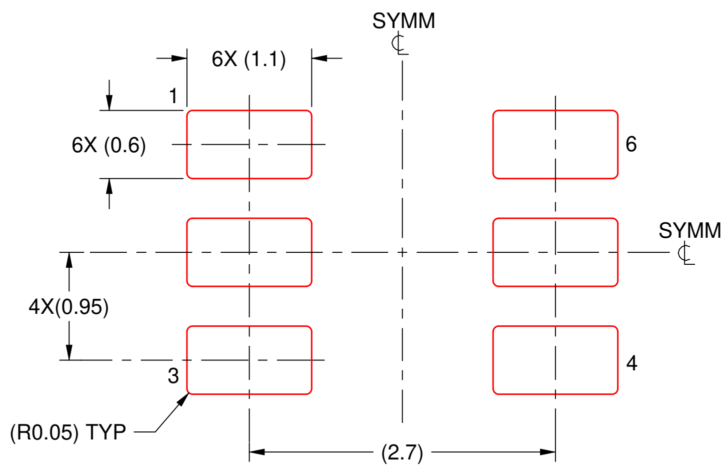
NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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