

**1.1 Scope.**

This specification covers the requirements for a monolithic high speed video signal multiplexer whose four channels of video input signals can be randomly switched at megahertz rates to the single output. Multiple devices can be configured in either parallel or cascade arrangements to form switch matrices. Refer to the commercial data sheet for the AD9300 for typical specifications, theory, and applications information.

**1.2 Part Number.**

The complete part number is as follows:

Device	Part Number
-1	AD9300T(X)/883B

**1.2.3 Case Outline.**

See Appendix 1 of General Specification ADI-M-1000:

(X)	Package	Description
Q	Q-16	16-Pin Ceramic DIP
E	E-20	20-Pin Leadless Chip Carrier

**1.3 Absolute Maximum Ratings.** ( $T_A = +25^\circ\text{C}$  unless otherwise noted)

Power Supply Voltages ( $\pm V_S$ )	$\pm 16$ V
Analog Input Voltage Each Input ( $IN_1$ thru $IN_4$ )	$\pm 3.5$ V
Differential Voltage Between Any Two Inputs ( $IN_1$ thru $IN_4$ )	5 V
Digital Input Voltages ( $A_0$ , $A_1$ , ENABLE)	-0.5 V to +5.5 V
Output Current	
Sinking	6.0 mA
Sourcing	6.0 mA
Junction Temperature	+175°C
Operating Temperature Range (Case)	-55°C to +125°C
Storage Temperature Range (Case)	-65°C to +150°C
Lead Temperature (Soldering 10 sec)	+300°C

**1.5 Thermal Characteristics.**

Maximum junction temperature should not be allowed to exceed +175°C. Maximum power dissipation is related to typical thermal impedances:

16-pin ceramic: $\theta_{JA} = 87^\circ\text{C}/\text{W}$ , $\theta_{JC} = 25^\circ\text{C}/\text{W}$
20-pin LCC: $\theta_{JA} = 74^\circ\text{C}/\text{W}$ , $\theta_{JC} = 10^\circ\text{C}/\text{W}$

# AD9300—SPECIFICATIONS

Table 1.

Test	Symbol	Design Limit <sup>1</sup>	Sub Group 1	Sub Group 2, 3	Sub Group 4	Sub Group 9	Test Condition <sup>2</sup>	Units
Input Offset Voltage	$V_{OS}$		10	18				mV max
Input Bias Current	$I_{IB}$		37	55				$\mu$ A max
Voltage Gain <sup>3</sup>	$A_V$		0.990	0.985				V/V min
Gain Tolerance DC to 5 MHz 5 MHz to 8 MHz	$A_E$				0.1 0.3		$V_{IN} = \pm 1$ V	dB max dB max
Full Power Bandwidth <sup>4</sup>	FPBW				27		$V_{IN} = 2$ V p-p	MHz min
Output Swing	$V_{OUT}$		$\pm 2$	$\pm 2$				V min
Slew Rate <sup>5</sup>	$t_{SR}$				170			V/ $\mu$ s
$A_X$ Input to Channel HIGH Time	$t_{HIGH}$					50		ns max
$A_X$ Input to Channel LOW Time	$t_{LOW}$					45		ns max
Enable to Channel ON Time	$t_{ON}$					45		ns max
Enable to Channel OFF Time	$t_{OFF}$					45		ns max
Digital Inputs								
Logic "1" Voltage	$V_{OH}$		2	2				V min
Logic "0" Voltage	$V_{OL}$		0.8	0.8				V max
Logic "1" Current	$I_{OH}$		5	5				$\mu$ A max
Logic "0" Current	$I_{OL}$		1	1				$\mu$ A max
Positive Supply Current (+12.0 V)	$+I_S$		16	16				mA max
Negative Supply Current (-12.0 V)	$-I_S$		5	16				mA max
Power Supply Rejection Ratio	PSRR		67	67				dB min

NOTES

<sup>1</sup>Indicates specification which is guaranteed but not tested. Value shown is over full temperature range.

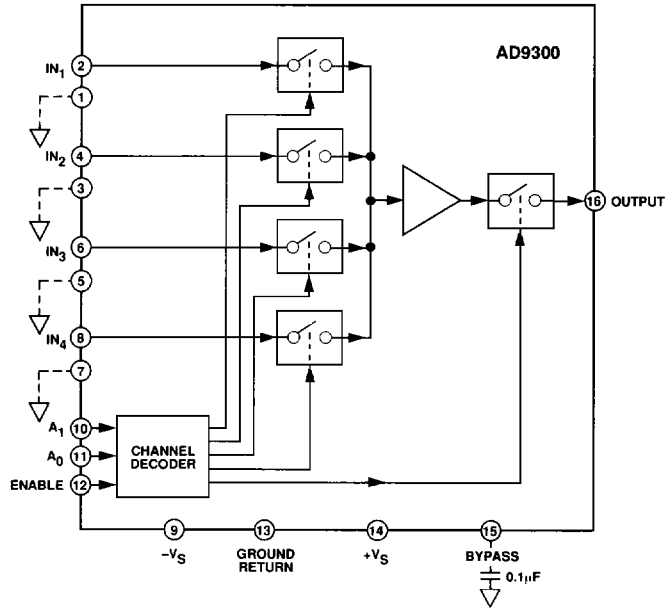
<sup>2</sup> $\pm V_S = \pm 12$  V  $\pm 5\%$ ;  $C_L = 10$  pF;  $R_L = 2$  k $\Omega$ , unless otherwise noted.

<sup>3</sup>Measured as slope of  $V_{OUT}$  versus  $V_{IN}$  with  $V_{IN} = \pm 1$  V.

<sup>4</sup>Full Power Bandwidth (FPBW) based on Slew Rate (SR).  $FPBW = SR/2 \pi V_{Peak}$ .

<sup>5</sup>Measured between 20% and 80% transition points of  $\pm 1$  V output.

### 3.2.1 Functional Block Diagram and Terminal Assignments.



### 3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group D58.

### 4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).

