TPS54317EVM-159 3-A, SWIFT™ Regulator Evaluation Module

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1 Introduction

This user's guide contains background information for the TPS54317 as well as support documentation for the TPS54317EVM-159 evaluation module (HPA159). The TPS54317EVM-159 performance specifications are given, as well as the schematic and bill of materials for the TPS54317EVM-159.

1.1 Background

The TPS54317 dc/dc converter is designed to provide up to 3 A output from an input voltage source of 3 V to 6 V. This device features extended operating frequency range. Rated input voltage and output current range is given in Table 1. This evaluation module is designed to demonstrate the small PCB areas that may be achieved when designing with the TPS54317 regulator, and does not reflect the high efficiencies that may be achieved when designing with this part. The switching frequency is set at a nominal 1100 kHz, allowing the use of a small-footprint 1.5-µH output inductor. The high and low-side MOSFETs are incorporated inside the TPS54317 package along with the gate drive circuitry. The low drain-to-source on

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resistance of the MOSFETs allows the TPS54317 to achieve high efficiencies and helps to keep the junction temperature low at high output currents. The compensation components are provided external to the IC, and allow for an adjustable output voltage and a customizable loop response. Additionally, the TPS54317 provides a full feature set including programmable undervoltage lockout, synchronization, adjustable switching frequency, enable, and power-good functions.

Table 1. Input Voltage and Output Current Summary

EVM	INPUT VOLTAGE RANGE	OUTPUT CURRENT RANGE
TPS54317EVM-159	VIN = 3.1 V to 3.5 V	0 A to 3 A

1.2 Performance Specification Summary

A summary of the TPS54317EVM-159 performance specifications is provided in Table 2. Specifications are given for an input voltage of VIN = 3.3 V and an output voltage of 1.8 V unless otherwise specified. The TPS54317EVM-159 is designed and tested for VIN = 3.1 V to 3.5 V. The ambient temperature is 25°C for all measurements, unless otherwise noted. The maximum input voltage for the TPS54317 is 6.0 V.

Table 2. TPS54317EVM-159 Performance Specification Summary

SPECIFICATION		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VIN voltage range			3.1	3.3	3.5	V
Output voltage set point				1.8		V
Output current range		V_{IN} = 3.3 V	0		3	A
Line regulation		I_O = 0 A – 3 A, VIN = 3 V - 6 V		±0.1%		
Load regulation		VIN = 3.3 V, I_O = 0 A to 3 A		±0.2%		
Load transient response	Voltage change	I_O = 0.75A to 2.25 A		-40		mV
	Recovery time			200		ms
	Voltage change	I_O = 10.5 A to 3.5 A		+40		mV
	Recovery time			200		ms
Loop bandwidth		VIN = 3.3 V		46		kHz
		VIN = V				
Phase margin		VIN = 3.3 V		59		°
		VIN = V				
Input ripple voltage				80		mVpp
Output ripple voltage				4		mVpp
Output rise time				3.7		ms
Operating frequency				1100		kHz
Max efficiency		VIN = 3.3 V, V_O = 1.8 V, I_O = 0.6 A		90.5%		

1.3 Modifications

While the TPS54317EVM-159 is designed to demonstrate the small size that can be attained when designing with the TPS54317, many features allowing extensive modifications have been included in this EVM.

1.3.1 Output Voltage Setpoint

To change the output voltage of the EVM, it is necessary to change the value of resistor R2. Changing the value of R2 can change the output voltage in the range of 0.9 V to 2.5 V. The value of R2 for a specific output voltage can be calculated using Equation 1.

$$R2 = 10\ k\Omega \times \frac{0.891\ V}{V_O - 0.891\ V} \quad (1)$$

Table 3 list the R2 values for some common output voltages. Note that PVIN must be greater than 3 V to generate a 2.5 V output.

Table 3. Output Voltages Available

Output Voltage (V)	R_2 Value (Ω)
1.0	82.3 k
1.2	28.7 k
1.5	14.7 k
1.8	9.76 k
2.5	5.49 k

1.3.2 Switching Frequency

The switching frequency of the EVM is set to 1100 kHz by setting R4 to 41.2 kΩ. The switching frequency may be trimmed to any value between 280 kHz and 1600 kHz by changing the value of R4 using Equation 2. The EVM may also be set to one of the two internally-programmed frequencies. Remove R4 and use a jumper on the three-pin header J4 to select 350-kHz or 550-kHz operation. The jumper settings are conveniently silk-screened on the EVM printed circuit board. Note that decreasing the switching frequency will result in increased output ripple unless the value of L1 is increased.

$$f_S = \frac{51\ k\Omega}{R4} + 4.7\ k\Omega \quad (2)$$

Where f_{SW} is in MHz and R4 is in kΩ.

1.3.3 Input Filter

An onboard electrolytic input capacitor is included at C1. Depending on the application, this capacitor may be removed.

1.3.4 Synchronization

The TPS54317EVM-159 may be synchronized to an external clock frequency. The synchronization-frequency range is 330 kHz to 700 kHz. Drive a synchronization signal into the SYNC pin by connecting to Pin 2 of J4, and use R4 to set the free-running frequency to 80% of the synchronization-signal frequency.

1.3.5 Extending Slow Start Time

The slow-start time may be extended by adding a capacitor at C5. The value for C5 for a desired slow-start time is given by Equation 3.

$$C5(\mu F) = T_{SS}(ms) \times \frac{5\ \mu A}{1.2\ V} \quad (3)$$

1.3.6 Input Voltage Range

The EVM is designed to operate from a nominal 3.3 V ±0.2 V input voltage. The TPS54317 is specified to operate over an input voltage range of 3 to 6 V. The EVM may be operated over this range without damage, however the inductor ripple current will increase at higher voltages, resulting in increased output ripple voltage. Also, at higher input voltages, the closed loop crossover frequency will increase and the phase margin will decrease.

2 Test Setup and Results

This chapter describes how to properly connect, setup, and use the TPS54317EVM-159 evaluation module. The chapter also includes test results typical for the TPS54317EVM-159 and covers efficiency, output voltage regulation, load transients, loop response, output ripple, input ripple, and startup.

2.1 Input / Output Connections

The TPS54317EVM-159 is provided with input/output connectors and testpoints as shown in Table 4. A power supply capable of supplying 3 A should be connected to J1 through a pair of 20 AWG wires. The load should be connected to J3 through a pair of 20 AWG wires. The maximum load current capability should be 14 A. Wire lengths should be minimized to reduce losses in the wires. Testpoint TP1 provides a place to monitor the VIN input voltages with TP2 providing a convenient ground reference. TP4 is used to monitor the output voltage with TP5 as the ground reference.

Table 4. EVM Connectors and Testpoints

Reference Designator	Function
J1	VIN, 3.3 V nominal, 3.1 to 3.5 V
J2	VOUT, 1.8 V at 3 A maximum
JP1	3 pin header to select pre-set operating frequency. Jumper SYNC to VIN for 550 kHz operation, jumper SYNC to GND for 350 kHz operation. Must remove R4 to use this function.
JP2	2 pin header with SS/ENA and GND. Connect SS/ENA to ground to disable, open to enable.
JP3	2 pin header with VIN and PWRGD Pull Up. Connect Pull up to Vin if desired.
TP1	VIN test point at VIN connector
TP2	GND testpoint at VIN
TP3	Test point between compensation network and R7. Used for loop response measurements.
TP4	Output voltage testpoint at VOUT connector
TP5	GND testpoint at VOUT connector
TP6	PWRGD test point

2.2 Efficiency

The TPS54317EVM-159 efficiency peaks at load current of about 0.6 A, and then decreases as the load current increases towards full load. Figure 1 shows the efficiency for theTPS54317EVM-159 at an ambient temperature of 25°C. The efficiency is lower at higher ambient temperatures, due to temperature variation in the drain-to-source resistance of the MOSFETs. The efficiency is slightly lower at 1100 kHz than at lower switching frequencies due to the gate and switching losses in the MOSFETs.

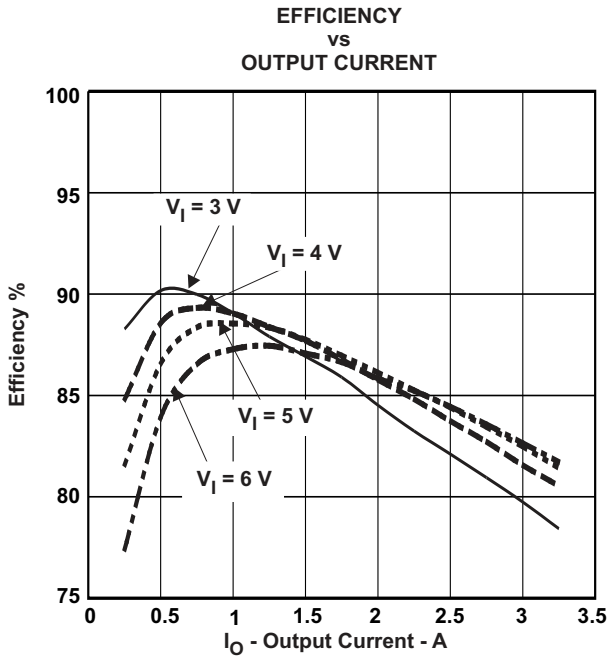

Figure 1. Measured Efficiency

2.3 Output Voltage Regulation

The output voltage load regulation of the TPS54317EVM-159 is shown in Figure 2, while the output voltage line regulation is shown in Figure 3. Measurements are given for an ambient temperature of 25°C.

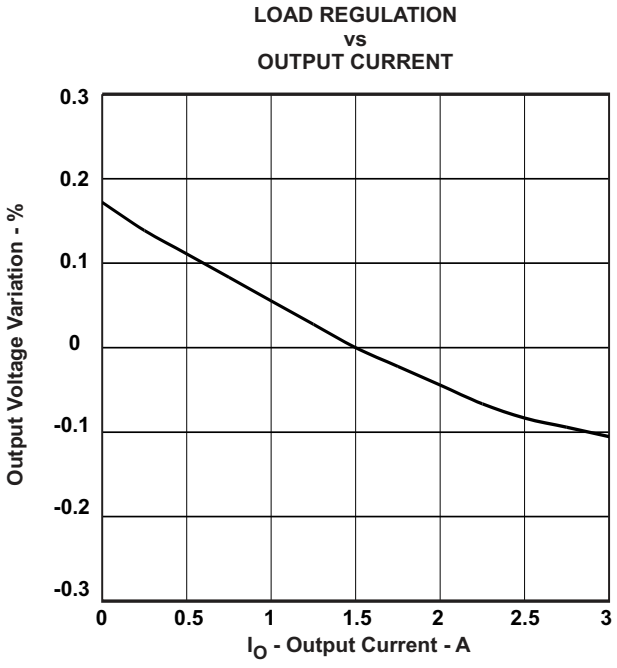

Figure 2. Load Regulation

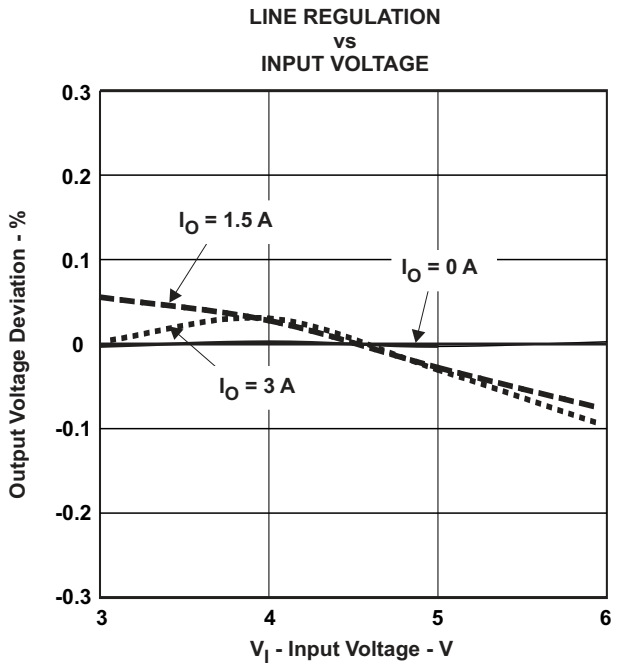

Figure 3. Line Regulation

2.4 Load Transients

The TPS54317EVM-159 response to load transients is shown in Figure 4. The current step is from 25 to 75 percent of maximum rated load. Total peak-to-peak voltage variation is as shown, including ripple and noise on the output.

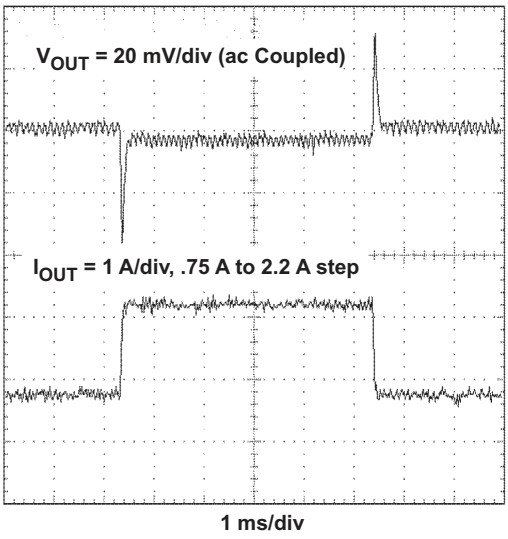

Figure 4. Load Transient Response

2.5 Loop Characteristics

The TPS54317EVM-159 loop-response characteristics are shown in Figure 5. Gain and phase plots are shown for VIN voltage of 3.3 V.

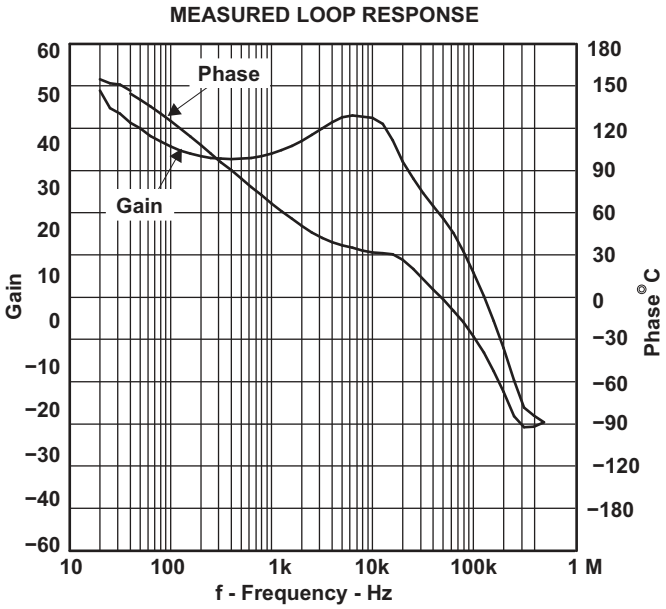

Figure 5. Measured Loop Response

2.6 Output Voltage Ripple

The TPS54317EVM-159 output voltage ripple is shown in Figure 6. The input voltage is VIN = 3.3 V for the TPS54317. Output current is the rated full load of 3 A. Voltage is measured directly across output capacitors.

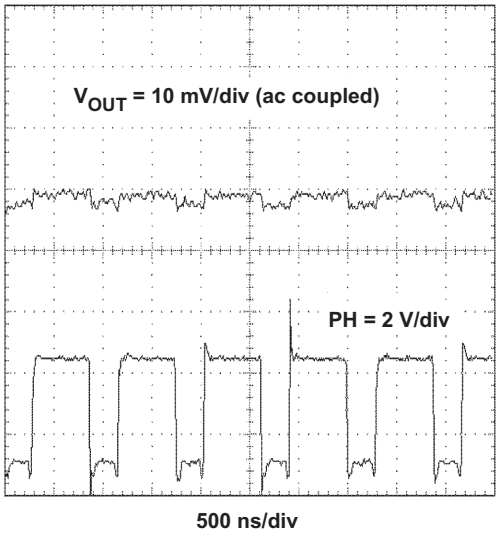

Figure 6. Measured Output Voltage Ripple

2.7 Input Voltage Ripple

The TPS54317EVM-159 output voltage ripple is shown in Figure 7. The input voltage is VIN = 3.3 V for the TPS54317. Output current for each device is at full rated load of 3 A.

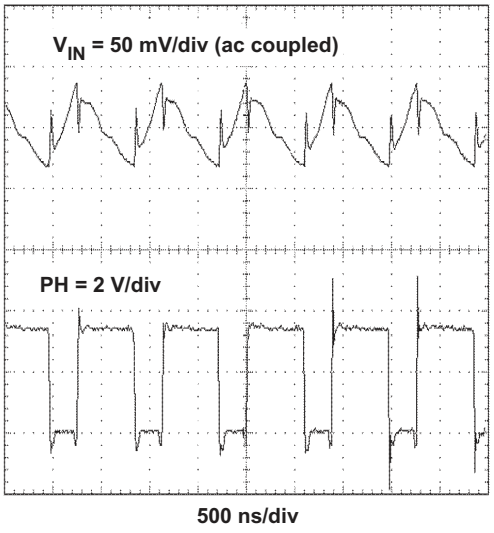

Figure 7. Input Voltage Ripple

2.8 Powering Up

The TPS54317EVM-159 start up waveforms are shown in Figure 8 The top trace shows VIN while the bottom trace shows Vout. Vin charges up from 0 V towards 3.3 V. When the input voltage reaches the internally set UVLO threshold voltage, the slow-start sequence begins. After a delay, the internal reference

begins to ramp up linearly at the internally set slow start rate towards 0.891 V and the output ramps up towards the set voltage of 1.8 V. The output may be inhibited by using a jumper at JP2 to tie SS/ENA to GND. When the jumper is removed, SS/ENA is released and the slow-start voltage begins to ramp up at the internally set rate. When the SS/ENA voltage reaches the enable-threshold voltage of 1.2 V, the start-up sequence begins as described above.

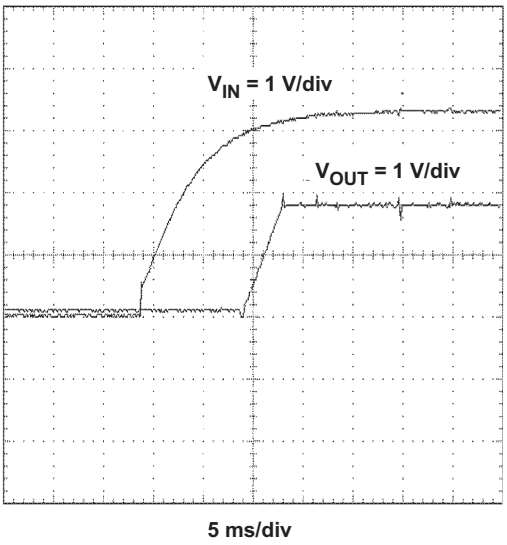

Figure 8. Power Up, VOUT relative to VIN

3 Board Layout

This chapter provides a description of the TPS54317EVM-159 board layout and layer illustrations.

3.1 Layout

The board layout for the TPS54317EVM-159 is shown in Figure 9 through Figure 11. The topside layer of the TPS54317EVM-159 is laid out in a manner typical of a user application. The top, and bottom layers are 2.0 oz. copper.

The top layer contains the main power traces for VIN, VOUT, and VPHASE. Also on the top layer are connections for the remaining pins of the TPS54317 and a large area filled with ground. The bottom layer contains ground and some signal routing. The top and bottom and internal ground traces are connected with multiple vias placed around the board including 6 directly under the TPS54317 device to provide a thermal path from the PowerPAD™ land to ground.

The input decoupling capacitors (C1 and C9), bias decoupling capacitor (C4), and bootstrap capacitor (C3) are all located as close to the IC as possible. In addition, the compensation components are also kept close to the IC. The compensation circuit ties to the output voltage at the point of regulation, adjacent to the high frequency bypass output capacitor.

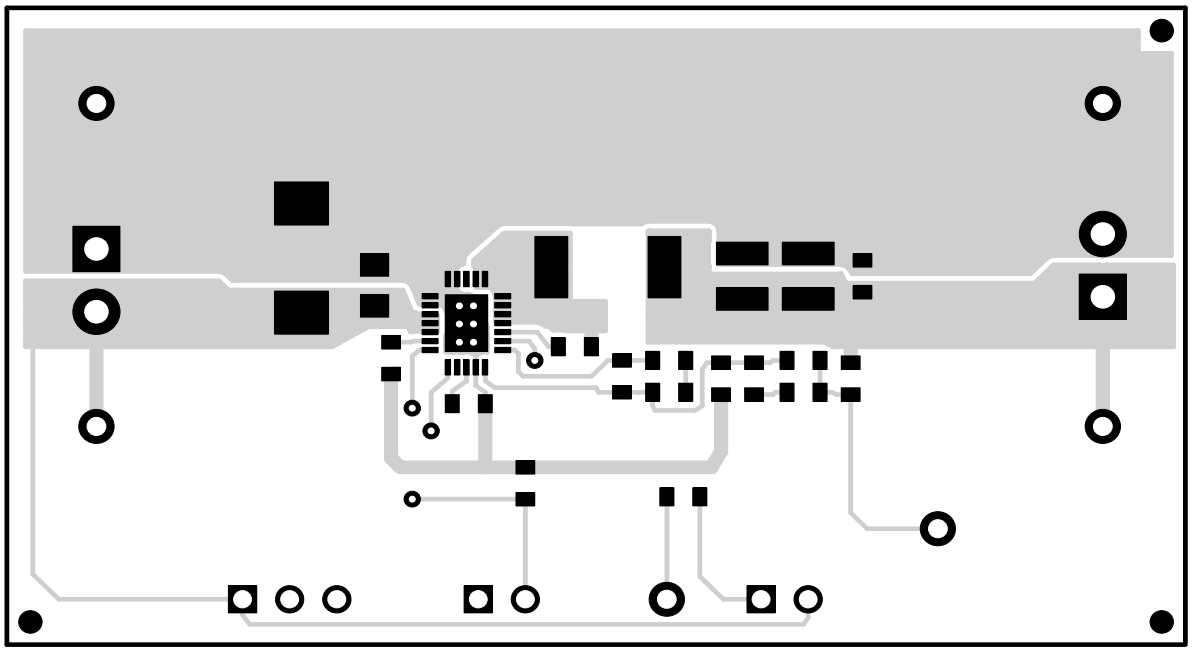

Figure 9. Top-side Layout

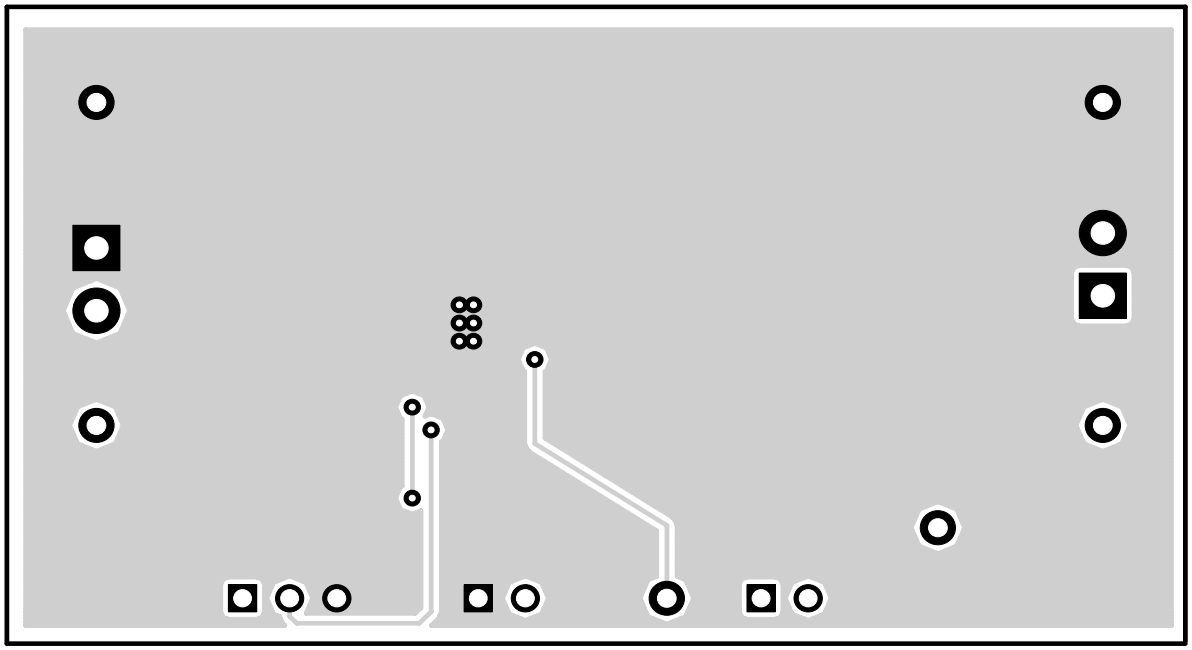

Figure 10. Bottom Side Layout (looking from top side)

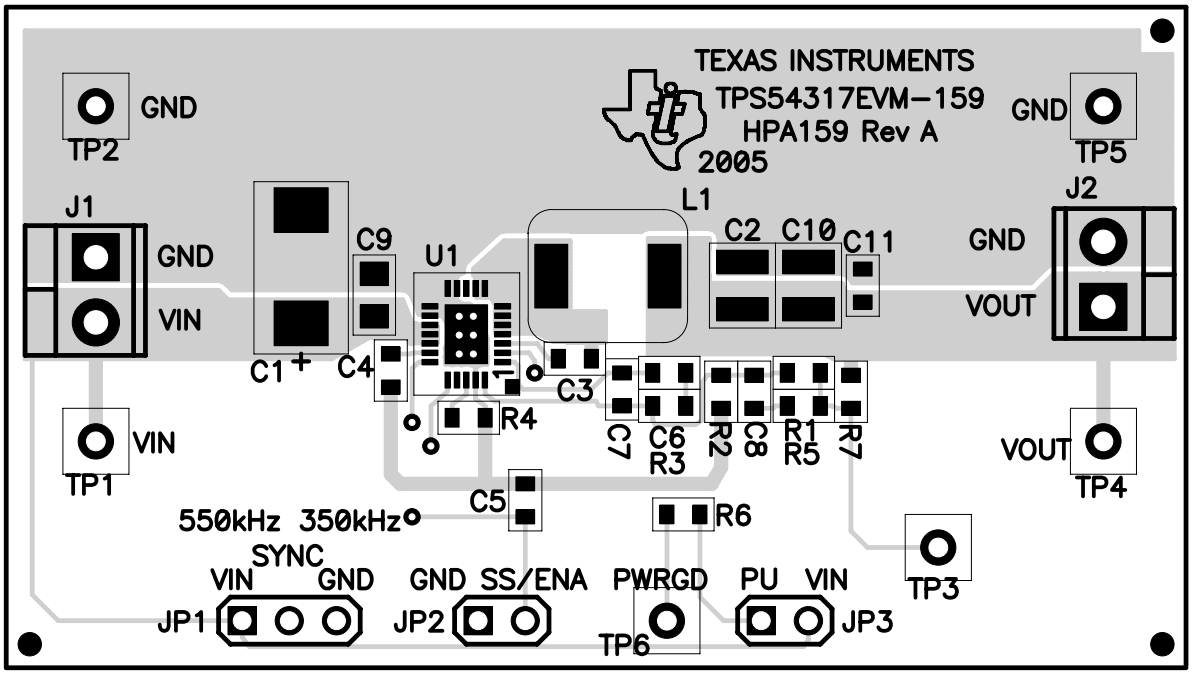

Figure 11. Top Side Assembly

4 Schematic and Bill of Materials

The TPS54317EVM-159 schematic and bill of materials are presented in this chapter.

4.1 Schematic

The schematic for the TPS54317EVM-159 is shown in Figure 12.

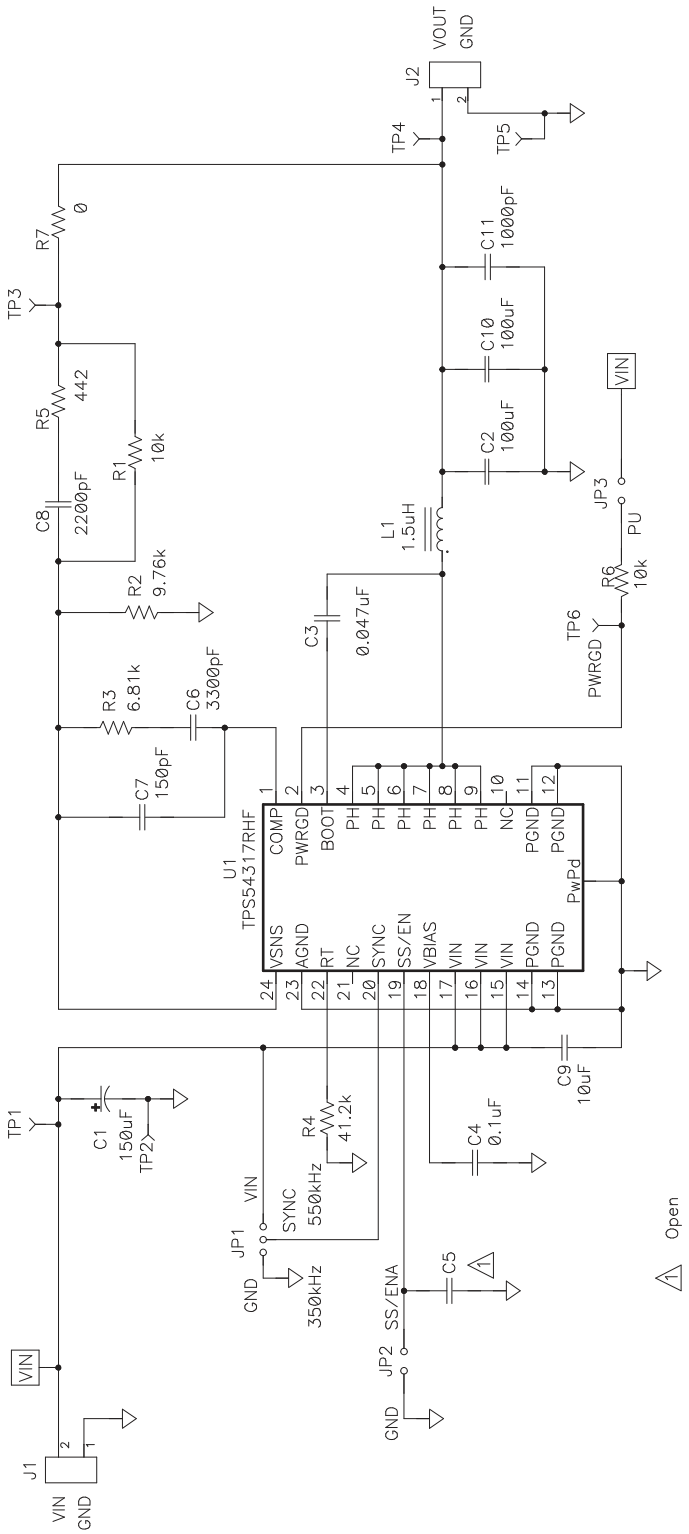

Figure 12. TPS54317EVM-159 Schematic

4.2 Bill of Materials

The bill of materials for the TPS54317EVM-159 is given by Table 5.

Table 5. TPS54317EVM-159 Bill of Materials

COUNT	REF DES	VALUE	DESCRIPTION	SIZE	PART NUMBER	MFR
1	C1	150uF	Capacitor, POSCAP, 6.3V, 55milliohm, 20%	7343(D)	6TPB150ML	Sanyo
2	C10, C2	100uF	Capacitor, Ceramic, 6.3V, X5R, 20 %	1210	C3225X5R0J107M	TDK
1	C11	1000pF	Capacitor, Ceramic, 50V, C0G, 5%	0603	C1608C0G1H102JB	TDK
1	C3	0.047uF	Capacitor, Ceramic, 50V, X5R, 10%	0603	C1608X5R1H473KB	TDK
1	C4	0.1uF	Capacitor, Ceramic, 25V, X7R, 10%	0603	C1608X7R1E104K	TDK
0	C5	Open	Capacitor, Ceramic	0603		
1	C6	3300pF	Capacitor, Ceramic, 50V, C0G, 5%	0603	C1608C0G1H332JB	TDK
1	C7	150pF	Capacitor, Ceramic, 50V, C0G, 5%	0603	C1608C0G1H151JB	TDK
1	C8	2200pF	Capacitor, Ceramic, 50V, C0G, 5%	0603	C1608C0G1H222JB	TDK
1	C9	10uF	Capacitor, Ceramic, 10V, X5R, 10%	0805	C2012X5R1A106K	TDK
2	J1, J2		Terminal Block, 2 pin, 6A, 3.5mm	0.27 x 0.25	ED1514	OST
1	JP1		Header, 3-pin, 100mil spacing, (36-pin strip)	0.100 x 3	PTC36SAAN	Sullins
2	JP2, JP3		Header, 2 pin, 100mil spacing, (36-pin strip)	0.100 x 2	PTC36SAAN	Sullins
1	L1	1.5uH	Inductor, SMT, 9A, 15milliohm	0.255 x 0.270	IHLP2525CZ-01	Vishay
2	R1. R6	10k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R2	9.76k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R3	6.81k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R4	41.2k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R5	442	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R7	0	Resistor, Chip, 1/16W, 1%	0603	Std	Std
4	TP1, TP3, TP4, TP6		Test Point, Red, Thru Hole Color Keyed	0.100 x 0.100	5000	Keystone
2	TP2, TP5		Test Point, Black, Thru Hole Color Keyed	0.100 x 0.100	5001	Keystone
1	U1		IC, IFET Power Controller, Adj V, 3A	QFN-24	TPS54317RHF	TI
1	–		PCB, 2.5 In x 1.4 In x 0.062 In		HPA159	Any
3	–		Shunt, 100-mil, Black	0.1	929950-00	3M

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