

# BGS14PN10

SP4T high linearity, high power RF Switch

## Data Sheet

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## BGS14PN10 SP4T high linearity, high power RF Switch

### 1 Features

- High max RF power: 40 dBm CW @ 900 MHz, room temperature
- Two ultra-low loss ports (RF1 and RF3):
  - 0.19 dB @ f=0.9 GHz,  $P_{IN}$ =38 dBm
  - 0.29 dB @ f=1.9 GHz,  $P_{IN}$ =38 dBm
  - 0.51 dB @ f=2.7 GHz,  $P_{IN}$ =33 dBm
  - 1.20 dB @ f=3.8 GHz,  $P_{IN}$ =33 dBm
  - 1.90 dB @ f=5.8 GHz,  $P_{IN}$ =33 dBm
- Two low loss ports (RF2 and RF4):
  - 0.32 dB @ f=0.9 GHz,  $P_{IN}$ =38 dBm
  - 0.40 dB @ f=1.9 GHz,  $P_{IN}$ =38 dBm
  - 0.64 dB @ f=2.7 GHz,  $P_{IN}$ =33 dBm
  - 1.19 dB @ f=3.8 GHz,  $P_{IN}$ =33 dBm
  - 1.78 dB @ f=5.8 GHz,  $P_{IN}$ =33 dBm
- No DC decoupling components required, if no external DC is applied on RF ports
- High ESD robustness
- Low harmonic generation
- High linearity
  - RF1/RF3 72 dBm IIP3
  - RF2/RF4 74 dBm IIP3
- No power supply blocking required
- Supply voltage range: 1.8 to 3.6 V
- No insertion loss change within supply voltage range
- No linearity change within supply voltage range
- Suitable for EDGE / C2K / LTE / WCDMA / SV-LTE Applications
- Mobile cellular Rx/Tx applications, suitable for LTE/3G
- Applicable for main path and entire RF-Front-end without any power restrictions in mobile communication
  - DL/UL CA and MIMO
  - Micro/Pico Cells / Cellular base stations
  - Test equipment
  - Suitable for SV-LTE
- 0.5 to 6.0 GHz coverage
- Small form factor 1.1 mm x 1.5 mm
- 400  $\mu$ m pad pitch
- RoHS and WEEE compliant package

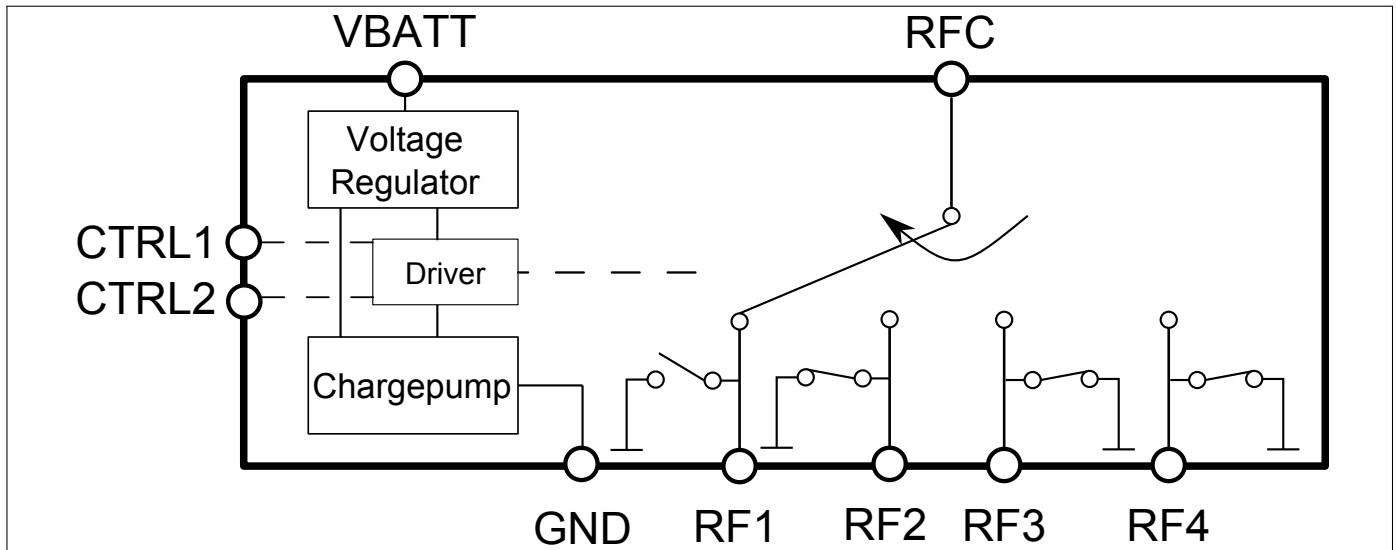


## 2 Product Description

The BGS14PN10 is a Single Pole Quad Throw (SP4T) RF antenna aperture switch optimized for mobile phone applications up to 6.0 GHz. This single supply chip integrates on-chip CMOS logic driven by a two simple, CMOS or TTL compatible control input signals. Unlike GaAs technology, the 0.1 dB compression point exceeds the switch maximum input power level, resulting in linear performance at all signal levels and external DC blocking capacitors at the RF ports are only required if DC voltage is applied externally.

**Table 1: Ordering Information**

Type	Package	Marking	Chip
BGS14PN10	TSNP10-1	4P	M4821C


**Figure 1:** BGS14PN10 block diagram

### 3 Maximum Ratings

**Table 2: Maximum Ratings, Table I** at  $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Frequency Range	$f$	0.5	–	–	GHz	<sup>1)</sup>
Supply voltage	$V_{DD}$	-0.5	–	3.6	V	–
Storage temperature range	$T_{STG}$	-55	–	150	$^\circ\text{C}$	–
RF input power	$P_{RF\_TRX}$	–	–	40	dBm	25% duty cycle
ESD capability Human Body Model	$V_{ESD_{HBM}}$	-1	–	+1	kV	
ESD capability ANT port (according IEC 61000-4-2 contact)	$V_{ESD_{ANT}}$	-8	–	+8	kV	On application board with 27nH shunt inductor
Junction temperature	$T_j$	–	–	125	$^\circ\text{C}$	–

<sup>1)</sup> Switch has no highpass response. There is also a high ohmic DC to the RF path. The DC voltage at RF ports  $V_{RFDC}$  has to be 0V.

**Table 3: Maximum Ratings, Table II at  $T_A = 25\text{ °C}$ , unless otherwise specified**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Maximum DC-voltage on RF-Ports and RF-Ground	$V_{RFDC}$	0	–	0	V	No DC voltages allowed on RF-Ports
Control Voltage Levels	$V_{CTRL}$	-0.7	–	3.3	V	–

## 4 Operation Ranges

**Table 4: Operation Ranges**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply voltage	$V_{DD}$	1.8	2.85	3.6	V	–
Supply current <sup>1)</sup>	$I_{DD}$	–	75	120	$\mu A$	–
Control voltage low	$V_{Ctrl,low}$	0		0.45	V	–
Control voltage high	$V_{Ctrl,high}$	1.2	1.8	2.85	V	$V_{Ctrl,high} \ll V_{DD}$
Control current low	$I_{Ctrl,low}$	-1	0	1	$\mu A$	–
Control current high	$I_{Ctrl,high}$	-1	0	1	$\mu A$	$V_{Ctrl,high} \ll V_{DD}$
Ambient temperature	$T_A$	-40	25	85	$^{\circ}C$	–
RF switching time <sup>2)</sup>	$t_{sw}$	1	2	5	$\mu s$	–
Startup time <sup>2)</sup>	$t_{sw}$		10	30	$\mu s$	–

<sup>1)</sup>  $T_A = -30\text{ °C} - +85\text{ °C}$ ,  $V_{BATT} = 1.8 - 3.6\text{ V}$

<sup>2)</sup>, Represents actual alpha status. To be updated.

## 5 Logic Table

**Table 5: Logic Table**

CTRL 1	CTRL 2	Mode
0	0	RF1 connected to ANT
0	1	RF2 connected to ANT
1	0	RF3 connected to ANT
1	1	RF4 connected to ANT



## 6 RF Characteristics for RF1 and RF3

Table 6: RF Specifications

Parameter	Symbol	Values			Unit	Note / Test Condition	
		Min.	Typ.	Max.			
<b>Insertion Loss</b>							
698 - 960 MHz	<i>IL</i>	–	0.18	0.26	dB	$V_{DD} = 1.8 - 3.6 V$ , $T_A = -30 \dots +85 \text{ }^\circ\text{C}$ , $Z_0 = 50 \text{ } \Omega$ , $P_{IN}$ up to 38 dBm	
1710 - 1980 MHz		–	0.29	0.36	dB		
1981 - 2170 MHz		–	0.30	0.41	dB		
2171 - 2690 MHz		–	0.51	0.68	dB		
3400 - 3800 MHz		–	1.20	1.40	dB		
5150 - 5850 MHz		–	1.90	2.35	dB		
<b>Return Loss</b>							
All Ports @ 698 - 915 MHz	<i>RL</i>	23	30	–	dB		
All Ports @ 1710 - 1980 MHz		16	19	–	dB		
All Ports @ 1981 - 2170 MHz		14	17	–	dB		
All Ports @ 2171 - 2690 MHz		11	12	–	dB		
All Ports @ 3400 - 3800 MHz		7	8	–	dB		
All Ports @ 5150 - 5850 MHz		6	7	–	dB		
<b>Isolation RFC</b>							
698 - 915 MHz	<i>ISO</i>	34	41	–	dB		
1710 - 1980 MHz		27	32	–	dB		
1981 - 2170 MHz		26	30	–	dB		
2171 - 2690 MHz		24	28	–	dB		
3400 - 3800 MHz		20	24	–	dB		
5150 - 5850 MHz		15	18	–	dB		
<b>Isolation RF1,2,3,4 - RF4,3,2,1</b>							
698 - 915 MHz	<i>ISO</i>	43	50	–	dB		
1710 - 1980 MHz		34	38	–	dB		
1981 - 2170 MHz		33	36	–	dB		
2170 - 2690 MHz		30	33	–	dB		
3400 - 3800 MHz		24	28	–	dB		
5150 - 5850 MHz		18	21	–	dB		

## 7 RF Characteristics for RF2 and RF4

Table 7: RF Specifications

Parameter	Symbol	Values			Unit	Note / Test Condition	
		Min.	Typ.	Max.			
<b>Insertion Loss</b>							
698 - 960 MHz	<i>IL</i>	–	0.30	0.40	dB	$V_{DD} = 1.8 - 3.6 V$ , $T_A = -30 \dots +85 \text{ }^\circ\text{C}$ , $Z_0 = 50 \text{ } \Omega$ , $P_{IN}$ up to 38 dBm	
1710 - 1980 MHz		–	0.40	0.50	dB		
1981 - 2170 MHz		–	0.41	0.54	dB		
2171 - 2690 MHz		–	0.64	0.80	dB		
3400 - 3800 MHz		–	1.19	1.45	dB		
5150 - 5850 MHz		–	1.78	2.09	dB		
<b>Return Loss</b>							
All Ports @ 698 - 915 MHz	<i>RL</i>	23	27	–	dB		
All Ports @ 1710 - 1980 MHz		17	20	–	dB		
All Ports @ 1981 - 2170 MHz		14	18	–	dB		
All Ports @ 2171 - 2690 MHz		11	15	–	dB		
All Ports @ 3400 - 3800 MHz		7	9	–	dB		
All Ports @ 5150 - 5850 MHz		6	8	–	dB		
<b>Isolation RFC</b>							
698 - 915 MHz	<i>ISO</i>	34	41	–	dB		
1710 - 1980 MHz		27	32	–	dB		
1981 - 2170 MHz		26	30	–	dB		
2171 - 2690 MHz		24	28	–	dB		
3400 - 3800 MHz		20	24	–	dB		
5150 - 5850 MHz		14	18	–	dB		
<b>Isolation RF1,2,3 - RF3,2,1</b>							
698 - 915 MHz	<i>ISO</i>	43	50	–	dB		
1710 - 1980 MHz		34	38	–	dB		
1981 - 2170 MHz		33	36	–	dB		
2170 - 2690 MHz		30	33	–	dB		
3400 - 3800 MHz		24	28	–	dB		
5150 - 5850 MHz		18	21	–	dB		

## 8 RF large signal parameter

**Table 8: RF large signal specifications for RF1 and RF3**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Max. RF input power	–	–	–	38	dBm	for typical $H_x$ behavior
<b>Harmonic Generation up to 12.75 GHz<sup>(1,2,3)</sup></b>						
Second Order Harmonics	$P_{H2}$	–	-100	–	dBc	25 dBm, 50Ω, CW mode
Third Order Harmonics	$P_{H3}$	–	-115	–	dBc	25 dBm, 50Ω, CW mode
All RF Ports	$P_{Hx}$	–	-100	–	dBc	25 dBm, 50Ω, CW mode
<b>Intermodulation Distortion IMD2<sup>(1,2,3)</sup></b>						
IIP2, low	IIP2,l	–	110	–	dBm	IIP2 conditions table 8
IIP2, high	IIP2,h	–	125	–	dBm	
<b>Intermodulation Distortion IMD3<sup>(1,2,3)</sup></b>						
IIP3	IIP3	–	72	–	dBm	IIP3 conditions table 9
<b>SV LTE Intermodulation<sup>(1,2,3)</sup></b>						
IIP3,SVLTE	IIP3,SV	–	73	–	dBm	SV-LTE conditions table 10

<sup>1</sup>Terminating Port Impedance:  $Z_0 = 50 \Omega$  <sup>2</sup>Supply Voltage:  $V_{DD} = 1.8 - 3.6 V$  <sup>3</sup>On application board without any matching components

**Table 9: RF large signal specifications for RF2 and RF4**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Max. RF input power	–	–	–	38	dBm	for typical $H_x$ behavior
<b>Harmonic Generation up to 12.75 GHz<sup>(1,2,3)</sup></b>						
Second Order Harmonics	$P_{H2}$	–	-105	–	dBc	25 dBm, 50Ω, CW mode
Third Order Harmonics	$P_{H3}$	–	-105	–	dBc	25 dBm, 50Ω, CW mode
All RF Ports	$P_{Hx}$	–	-105	–	dBc	25 dBm, 50Ω, CW mode
<b>Intermodulation Distortion IMD2<sup>(1,2,3)</sup></b>						
IIP2, low	IIP2,l	–	110	–	dBm	IIP2 conditions table 8
IIP2, high	IIP2,h	–	130	–	dBm	
<b>Intermodulation Distortion IMD3<sup>(1,2,3)</sup></b>						
IIP3	IIP3	–	74	–	dBm	IIP3 conditions table 9
<b>SV LTE Intermodulation<sup>(1,2,3)</sup></b>						
IIP3,SVLTE	IIP3,SV	–	74	–	dBm	SV-LTE conditions table 10

<sup>1</sup>Terminating Port Impedance:  $Z_0 = 50 \Omega$  <sup>2</sup>Supply Voltage:  $V_{DD} = 1.8 - 3.6 V$  <sup>3</sup>On application board without any matching components

**Table 10: IIP2 conditions table**

Band	In-Band Frequency [MHz]	Blocker Frequency 1 [MHz]	Blocker Power 1 [dBm]	Blocker Frequency 2 [MHz]	Blocker Power 2 [dBm]
Band 1 Low	2140	1950	20	190	-15
Band 1 High	2140	1950	20	4090	-15
Band 5 Low	881.5	836.5	20	45	-15
Band 5 High	881.5	836.5	20	1718	-15

**Table 11: IIP3 conditions table**

Band	In-Band Frequency [MHz]	Blocker Frequency 1 [MHz]	Blocker Power 1 [dBm]	Blocker Frequency 2 [MHz]	Blocker Power 2 [dBm]
Band 1	2140	1950	20	1760	-15
Band 5	881.5	836.5	20	791.5	-15

**Table 12: SV-LTE conditions table**

Band	In-Band Frequency [MHz]	Blocker Frequency 1 [MHz]	Blocker Power 1 [dBm]	Blocker Frequency 2 [MHz]	Blocker Power 2 [dBm]
Band 5	872	827	23	872	14
Band 13	747	786	23	747	14
Band 20	878	833	23	2544	14

## 9 Package Outline and Pin Configuration

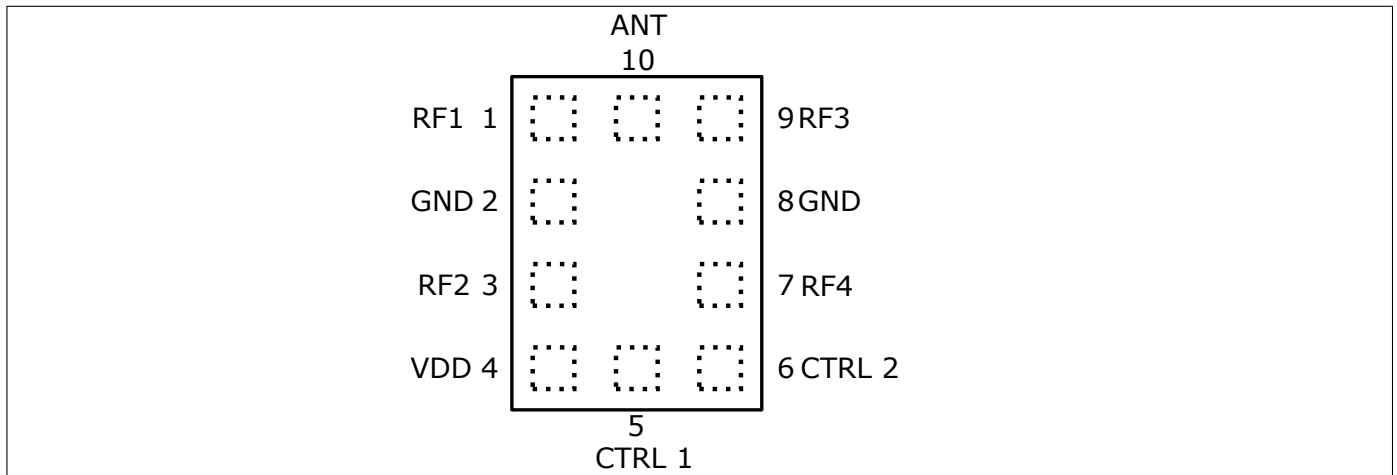


Figure 2: Pinout (top view)

Table 13: Pin Description

Pin No.	Name	Pin Type	Buffer Type	Function
1	RF1	I/O		RF1
2	GND	GND		Ground
3	RF2	I/O		RF2
4	VDD	PWR		Supply voltage
5	CTRL 1	I		Control Pin 1
6	CTRL 2	I		Control Pin 2
7	RF4	I/O		RF4
8	GND	GND		Ground
9	RF3	I/O		RF3
10	ANT	I/O		Common RF / Antenna

Table 14: Mechanical Data

Parameter	Symbol	Value	Unit
X-Dimension	<i>X</i>	1.1 ± 0.05	mm
Y-Dimension	<i>Y</i>	1.5 ± 0.05	mm
Size	<i>Size</i>	1.65	mm <sup>2</sup>
Height	<i>H</i>	0.375	mm

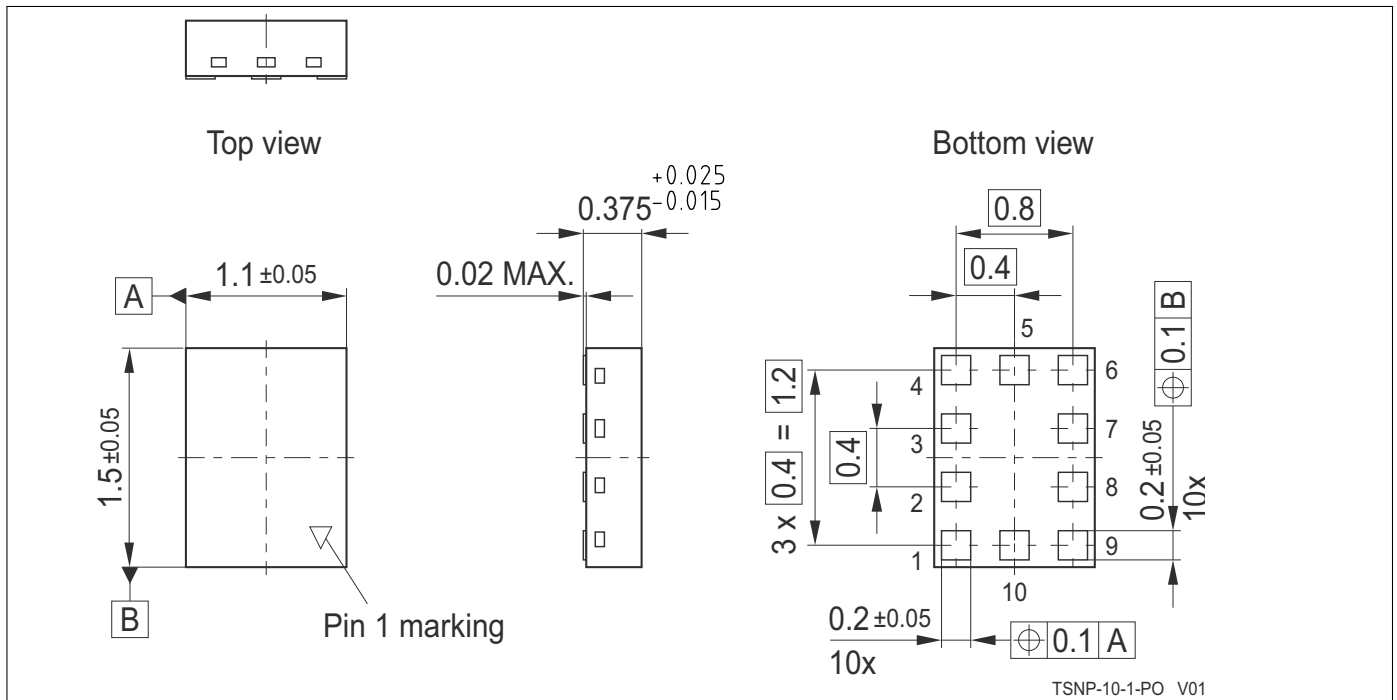


Figure 3: Package Dimensions Drawing

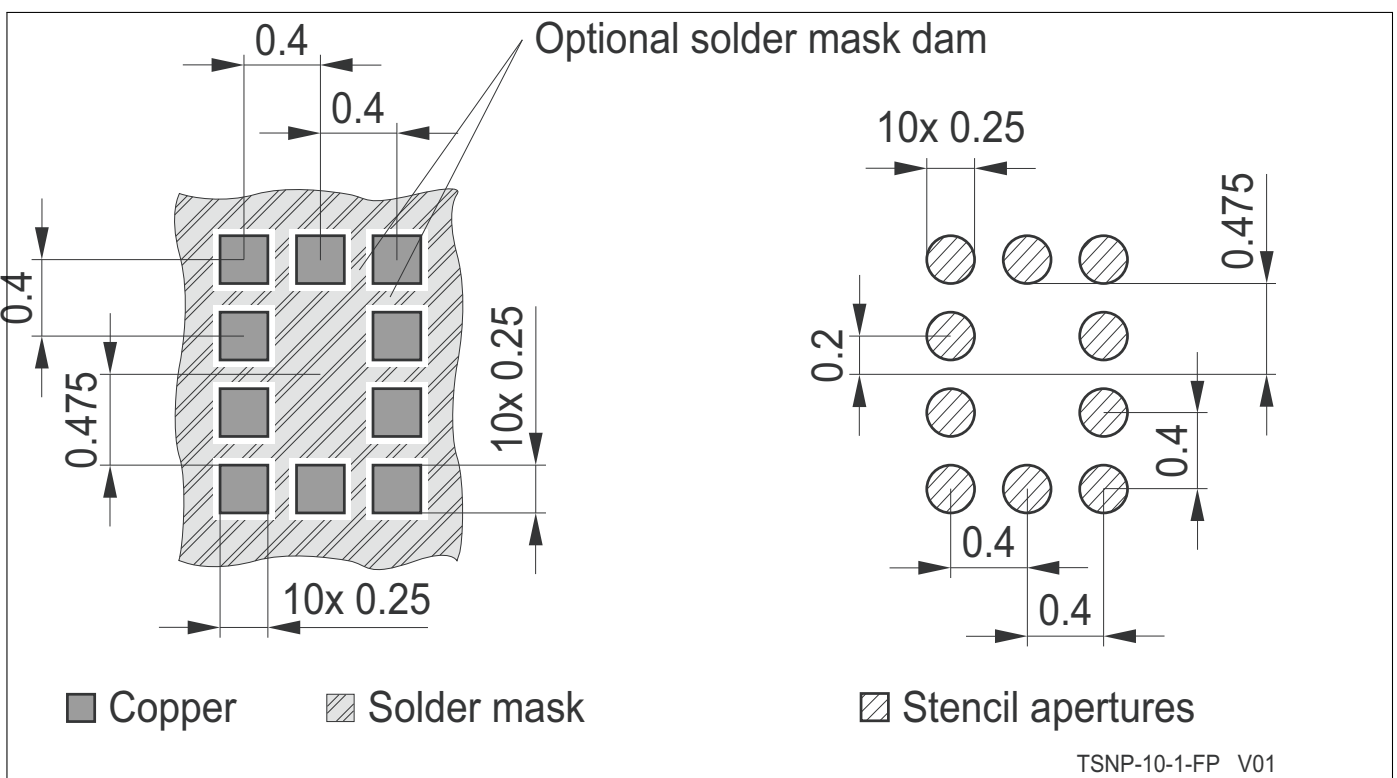


Figure 4: Land pattern and stencil mask

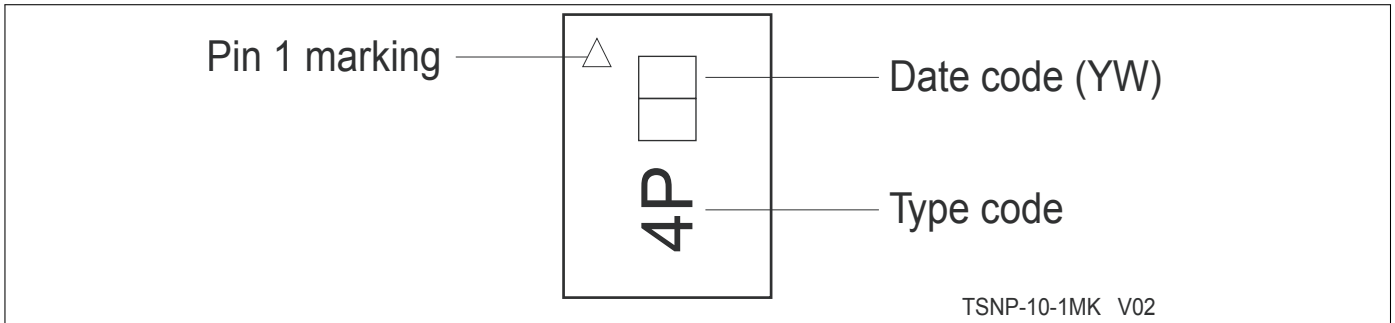


Figure 5: Marking

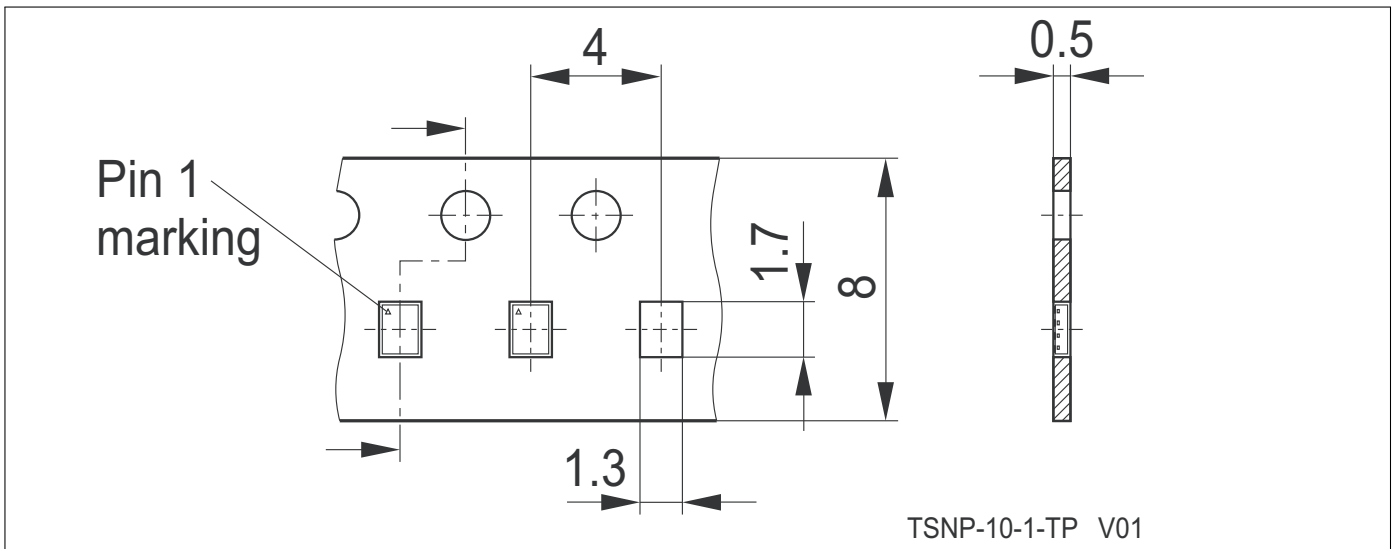


Figure 6: Tape drawing

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