ISSC Technologies Corp.

IS1690S SoC

Bluetooth® 3.0 Multi-Speaker Stereo Audio SOC

Features

System Specification

- Compliant with Bluetooth Specification v.3.0 + EDR in 2.4 GHz ISM band
- It supports following profiles :
  - Hands Free 1.5
  - Headset 1.0
  - A2DP 1.0
  - AVRCP 1.0

Baseband Hardware

- 16MHz main clock input
- Built-in internal ROM for program memory
- Support to connect to two hosts (phones, tablets…) with HFP or A2DP profiles simultaneously
- Adaptive Frequency Hopping (AFH) avoids occupied RF channels
- Fast Connection supported

RF Hardware

- Fully Bluetooth 3.0 + EDR system in 2.4 GHz ISM band.
- Combined TX/RX RF terminal simplifies external matching and reduces external antenna switches.
- Max. +4dBm output power with 20 dB level control from register control.
- Built-in T/R switch for Class 2/3 application
- To avoid temperature variation, temperature sensor with temperature calibration is utilized into bias current and gain control.
- Fully integrated synthesizer has been created. There requires no external VCO, varactor diode, resonator and loop filter.
- Crystal oscillation with built-in digital trimming for temperature/process variations.

Audio processor

- Support A-Law or μ-Law PCM format, or CVSD (Continuous Variable Slope Delta Modulation) for SCO channel operation.
- Noise suppression
- Echo suppression
- SBC decoding
- Packet loss concealment
- Build-in one languages (English) voice prompts and 20 events for each one
- Support SCMS-T

Audio Codec

- 16 bit DAC and 16 bit ADC codec
- 94dB SNR DAC playback
- 85 dB SNR ADC.

Peripherals

- Built-in Lithium-ion battery charger (up to 350mA)
- Integrate 3V, 1.8V configurable switching regulator and LDO
- Built-in ADC for battery monitor and voltage sense.
- A aux-in port for external audio input
- Two LED drivers

Flexible HCI interface

- High speed HCI-UART (Universal Asynchronous Receiver Transmitter) interface (up to 921600bps)

Package

- 7x7mm^2 56QFN package

Description

IS1690S multi-speaker stereo audio chip is a compact, highly integrated, CMOS single-chip RF and baseband IC for Bluetooth v3.0 with Enhanced Data Rate 2.4GHz applications. This chip is fully compliant with Bluetooth specification and completely backward-compatible with Bluetooth 2.0 or 1.2 systems.

It incorporates Bluetooth 1M/2M/3Mbps RF, single-cycle 8bit MCU, TX/RX modem, 5-port memory controller, task/hopping controller, UART interface, and ISSC's own Bluetooth software stack to achieve the required BT v3.0 with EDR functions.

To provide the superior audio and voice quality, it also integrates a DSP co-processor, a PLL, and a CODEC dedicated for voice and audio applications.

For voice, not only basic CVSD encoding and decoding but also enhanced noise reduction and echo cancellation are implemented by the built-in DSP to achieve better quality in both sending and receiving sides. For the enhanced audio applications, SBC decoding functions can be also carried out by DSP to satisfy Bluetooth A2DP requirements.

In addition, to minimize the external components required for portable devices, a battery voltage sensor , battery charger, a switching regulator and LDO are integrated to reduce system BOM cost for various Bluetooth applications.

Applications

- Stereo headsets
- Portable speakerphones
- Multi speaker.

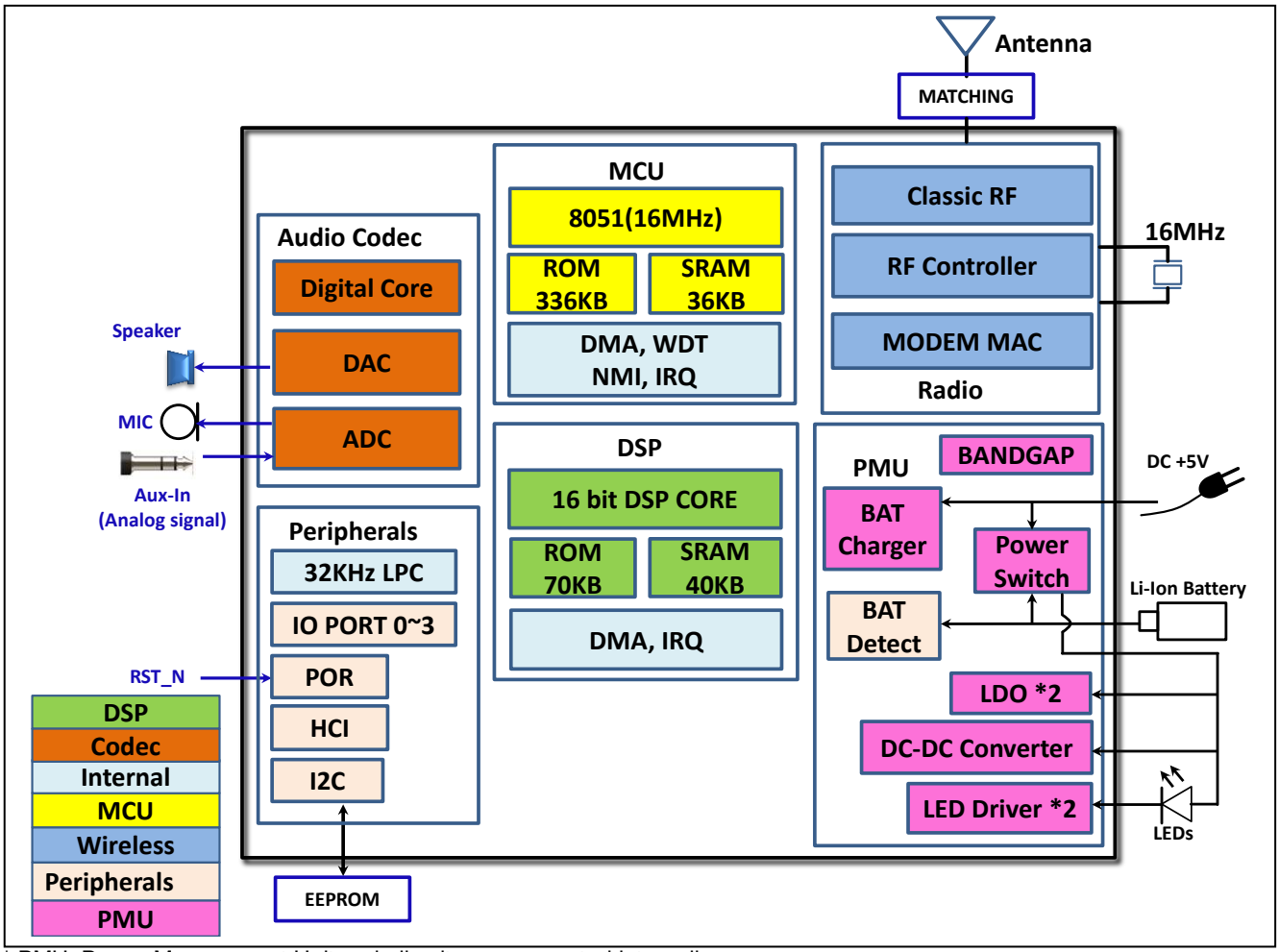
Table of Contents

Abbreviations List:
HFP: Hands-free Profile
AVRCP: Audio Video Remote Control Profile
A2DP: Advanced Audio Distribution Profile
PBAP: Phone Book Access Profile
HSP: Headset Profile
SPP: Serial Port Profile
NFC: Near Field Communication
SCMS-T:Serial Copy Management System

1.0 DEVICE OVERVIEW

IS1690S multi-speaker stereo audio chip integrate Bluetooth 3.0 radio transceiver, PMU and DSP . Figure 1-1 shows the block diagram.

FIGURE 1-1: BLOCK DIAGRAM



* PMU: Power Management Unit and all voltages generated internally.
* Aux in: analog aux-in signal.

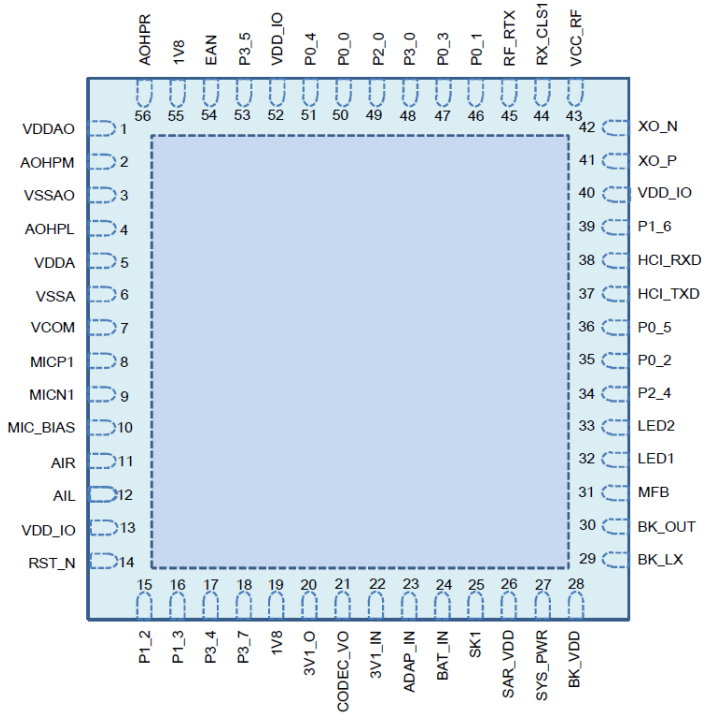
2.0 KEY FEATURES TABLE

SPEC / Chip	IS1690S
Application	Multi-SPK
Stereo/Mono	Stereo
Pin count	56
Dimension (mm^2)	7X7
Audio DAC output	2-ch
DAC (cap-less) SNR@2.8V (dB)	-94
ADC SNR @2.8V (dB)	-85
I^2S digital interface	X
Analog aux-in	√
Mono MIC	1
Support external audio amplifier	√
Built-in class-D audio amplifier	X
UART	X
LED Driver	2
Internal DC-DC step-down regulator	√
DC 5V ADAPTER	√
Battery charger (350mA max)	√
IO for application	10
Switches support	6
Support NFC application	√
Voice prompt	√
Multi-tone	√
DSP sound effects	√
Built-in EEPROM	X
Profile	
A2DP	1.0
AVRCP	1.0
HFP	1.5
HSP	1.0
PBAP	X
SPP	X

√ :Support the feature

3.0 PIN DESCRIPTION

TABLE 3-1: IS1690S PIN DESCRIPTION



Pin No.	Pin Type	Name	Description
1	P	VDDAO	Positive power supply dedicated to CODEC output amplifier.
2	AO	AOHPM	Headphone common mode output/sense input. Cap-less application only.
3	P	VSSAO	Negative power supply dedicated to CODEC output amplifier
4	AO	AOHPL	L-channel analog headphone output, for cap-less and single-ended application both
5	AP	VDDA	Positive power supply/reference voltage for CODEC
6	P	VSSA	Negative reference/power supply for CODEC
7	AO	VCOM	Internal biasing voltage for CODEC
8	AI	MICP1	Mic 1 mono differential analog positive input
9	AI	MICN1	Mic 1 mono differential analog negative input
10	P	MIC_BIAS	Electric microphone biasing voltage
11	AI	AIR	Stereo analog aux in, R-channel
12	AI	AIL	Stereo analog aux in, L-channel
13	P	VDD_IO	I/O power supply input
14	AI	RST_N	KEY PIN for FT Test System Reset Pin
15	I/O	P1_2	IO, default pull-high input KEY PIN for FT Test EEPROM clock SCL
16	I/O	P1_3	IO, default pull-high input KEY PIN for FT Test EEPROM data SDA

17	I/O	P3_4	IO, default pull-high input SLIDE SWITCH
18	I/O	P3_7	IO, default pull-high input FWD button
19	P	1V8	Core 1.8V power input
20	P	3V1_O	3.1V LDO output
21	P	CODEC_VO	3.1V LDO output for CODEC power
22	P	3V1_VIN	3.1V LDO input
23	P	ADAP_IN	Power adaptor DC 5V input
24	P	BAT_IN	Li-Ion Battery input, should be always connected even if the power is given on power Adaptor input.
25	AI	SK1	Default SAR input Aux-in detection
26	P	SAR_AVDD	SAR 1.8V input
27	P	SYS_PWR	System Power Output
28	P	BK_VDD	Buck VDD Power Input
29	P	BK_LX	Buck pin for switch
30	P	BK_OUT	Buck feedback sense pin
31	P	MFB	Multi-Function Push Button and power on key, push high
32	AI	LED1	LED Driver 1
33	AI	LED2	LED Driver 2
34	I/O	P2_4	IO, default pull-high input System Configuration , Hi: Boot Mode Lo: N_SPK Role Master/Slave
35	I/O	P0_2	IO, default pull-high input PLAY/PAUSE button
36	I/O	P0_5	IO, default pull-high input REV button
37	O	HCI_TXD	HCI TX data
38	I	HXI_RXD	HCI RX data
39	I/O	P1_6	IO, default pull-high input Volume down button
40	P	VDD_IO	I/O power supply input
41	I	XO_P	16MHz Crystal input positive
42	I	XO_N	16MHz Crystal input negative
43	RP	VCC_RF	RF power input for both synthesizer and TX/RX block
44	I	RX_CLASS1	Class1 RF RX path
45	I/O	RF_RTX	Class2 RTX path; Class1/Class2 TX path
46	I/O	P0_1	IO, default pull-high input Volume up button
47	I/O	P0_3	IO, default pull-high input KEY PIN for FT Test 3rd LED / DRC INDICATION
48	P	P3_0	IO, default pull-high input Low: N_SPK Role Master/Slave
49	I/O	P2_0	IO, default pull-high input System Configuration, H: Application L: Baseband(IBDK Mode)
50	I/O	P0_0	IO, default pull-low input. Audio amplifier enable

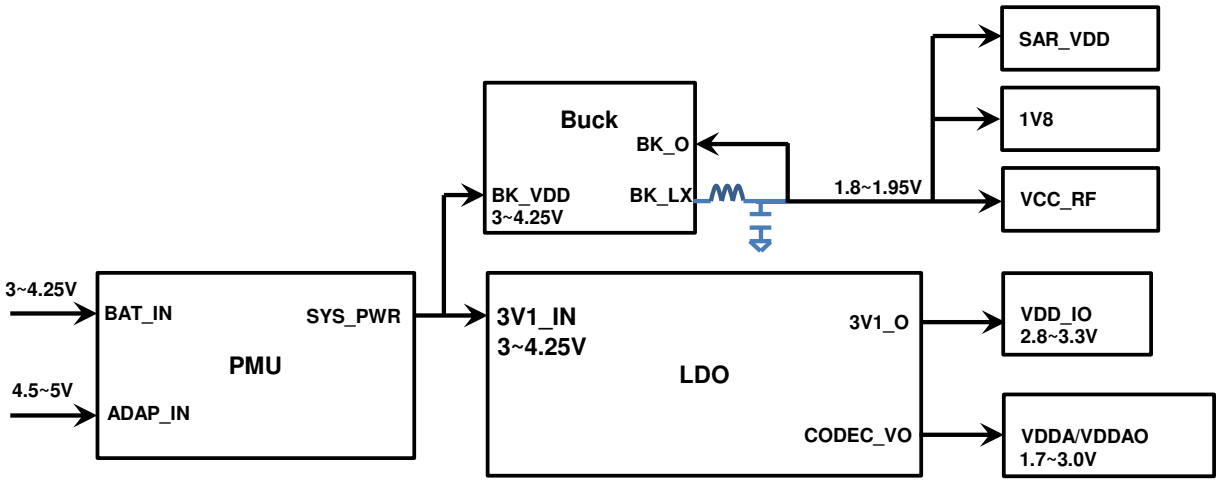
51	I/O	P0_4	IO, default pull-high input NFC Detection
52	P	VDD_IO	I/O power supply input
53	I/O	P3_5	IO 3_5, default pull-high input. Phone button
54	I	EAN	Embedded ROM/External Flash enable H: Embedded; L: External Flash
55	P	1V8	Core 1.8V power input
56	AO	AOHPR	R-channel single ended analog headphone output
57	P	GND	Exposed pad as ground

* I: signal input pin
*AI: analog signal input pin
* O: signal output pin
*AO: analog signal output pin
* I/O: signal input/output pin
* P: power pin
*AP: analog power pin
*RP: RF power pin

3.1 POWER SUPPLY

The device is powered by BAT pin. If a Battery is not connected to BAT_IN input external power supply can be provided as per the BAT voltage specification. Connections show below need to be made on the PCB from the BAT pin to other supply voltage pins on the chip.

FIGURE 3-1: POWER TREE DIAGRAM



4.0 TRANSCEIVER

IS1690S is designed and optimized for Bluetooth 2.4 GHz system. It contains a complete radio frequency transmitter/receiver section. An internal synthesizer generates a stable clock for synchronize with another device.

4.1 TRANSMITTER

The internal PA has a maximum output power of +4dBm with level control 20dB from the amplitude control. This is applied into Class2/3 radios without external RF PA.

The transmitter directly performs IQ conversion to minimize the frequency drift, and it can excess 20dB power range with temperature compensation mechanism.

4.2 RECEVIER

The LNA operates with TR-combined mode for single port application. It can save a pin on package and without an external TX/RX switch.

The ADC is utilized to sample the input analog wave and convert into digital signal for de-modulator analysis. A channel filter has been integrated into receiver channel before the ADC, which to reduce the external component count and increase the anti-interference capability.

The image rejection filter is used to reject image frequency for low-IF architecture. This filter for low-IF architecture is intent to reduce external BPF component for super heterodyne architecture.

RSSI signal is feedback to the processor to control the RF output power to make a good tradeoff for effective distance and current consumption.

4.3 SYNTHESIZER

A synthesizer generates a clock for radio transceiver operation. There is a VCO inside with tunable internal LC tank. It can reduce variation for components. A crystal oscillation with internal digital trimming circuit provides a stable clock for synthesizer.

4.4 MODEM

For Bluetooth v1.2 specification and below, 1 Mbps was the standard data rate based on Gaussian Frequency Shift Keying (GFSK) modulation scheme. This basic rate modem meets BDR requirements of Bluetooth v2.0 with EDR specification.

For Bluetooth v2.0 with EDR specification, Enhanced Data Rate (EDR) has been introduced to provide 2 and 3 Mbps data rates as well as 1 Mbps. This enhanced data rate modem meets EDR requirements of Bluetooth v2.0 with EDR specification. For the viewpoint of baseband, both BDR and EDR utilize the same 1MHz symbol rate and 1.6 KHz slot rate. For BDR, 1 symbol represents 1 bit. However each symbol in the payload part of EDR packets represents 2 or 3 bits. This is achieved by using two different modulations, π/4 DQPSK and 8DPSK.

4.5 Adaptive Frequency Hopping (AFH)

FW will scan and use background noise power to determine 20 channels to stand for good channels. Adaptive Frequency Hopping (AFH) avoids occupied RF channels

5.0 MICROPROCESSOR

A single-cycle 8-bit MCU is built into IS1690S multi-speaker chip to execute the Bluetooth protocols. It operates from 16MHz to 48MHz where the firmware can dynamically adjust the tradeoff between the computing power and the power consumption. The MCU firmware is hard-wired in ROM to minimize the firmware execution power consumption and to save the external flash cost.

5.1 MEMORY

A synchronous single port RAM interface is used. There are sufficient ROM (336KB) and RAM (36KB) to fulfill the requirement of processor. A register bank, a dedicated single port memory and a flash memory are connected to the processor bus. The processor coordinates all the link control procedures and data movement using a set of pointers registers.

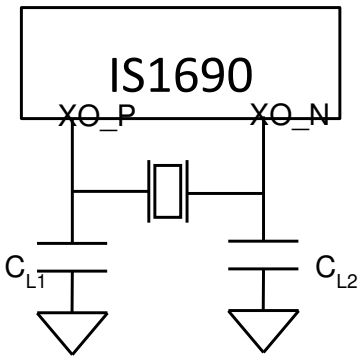
5.2 EXTERNAL RESET

The chip provides a watchdog timer to reset the chip. It has an integrated Power-On Reset (POR) circuit that resets all circuits to a known power-on state. This action can also be driven by an external reset signal that can be used to externally control the device, forcing it into a power-on reset state. The RST signal input is active low and no connection is required in most applications.

5.3 REFERENCE CLOCK

IS1690S chip is composed of an integrated crystal oscillation function. It uses a 16 MHz external crystal and two specified loading capacitors to provide a high quality system reference timer source. This feature is typically used to remove the initial tolerance frequency errors associated with the crystal and its equivalent loading capacitance in mass production. Frequency trim is achieved by adjusting the crystal loading capacitance through the on-chip trim capacitors C_{TRIM}..

The value of trimming capacitance is around 200fF ($200x10^{-15}$ F) per LSB at 5 bits word, therefore the overall adjustable clock frequency is around 40 KHz.



C_{TRIM}= 200fF*(1~31)

$C_L=[(C_{L1}*C_{L2})/(C_{L1}+C_{L2})]+C_{TRIM}$

* For C_L selection, please refer to the datasheet of crystal vendor

6.0 AUDIO

There are a few stages for input audio and output audio. Each stage can be programmed to vary the gain response characteristics. For microphone input, both single-end input and differential input are supported. One of the important points in maintaining a high quality signal is to provide a stable bias voltage source to the condenser microphone's FET. DC blocking capacitors may be used at both positive and negative sides of input. Internally, this analog signal is converted to 16-bit 8 kHz linear PCM data.

6.1 DIGITAL SIGNAL PROCESSOR

A digital signal processor (DSP) cooperates with MCU to perform digital audio processing with some advanced features such as noise cancellation, audio output level suppression and etc. It provides audio processing with some advanced features. The DSP cancels the acoustic echo that may present in headset or speaker. All the audio processing is performed by the DSP with low power consumption. This technique effectively cancels the incoming echo signal without impact to the desired voice signal. An outgoing signal to the speaker which level exceeds the threshold (and therefore deemed likely to create echo) will be result in suppression of the signal along the input path from the microphone. Filtering is also applied to provide a smoother transition for more natural user experience.

6.2 CODEC

The built-in codec has a high Signal to Noise ratio performance. This built-in codec consist of an analog to digital converter (ADC), a digital to analog converter (DAC) and additional analog circuitry.

6.3 AUX-IN

There is an analog audio input for external audio source. This source can flow through analog loopback.

7.0 POWER MANAGEMENT UNIT

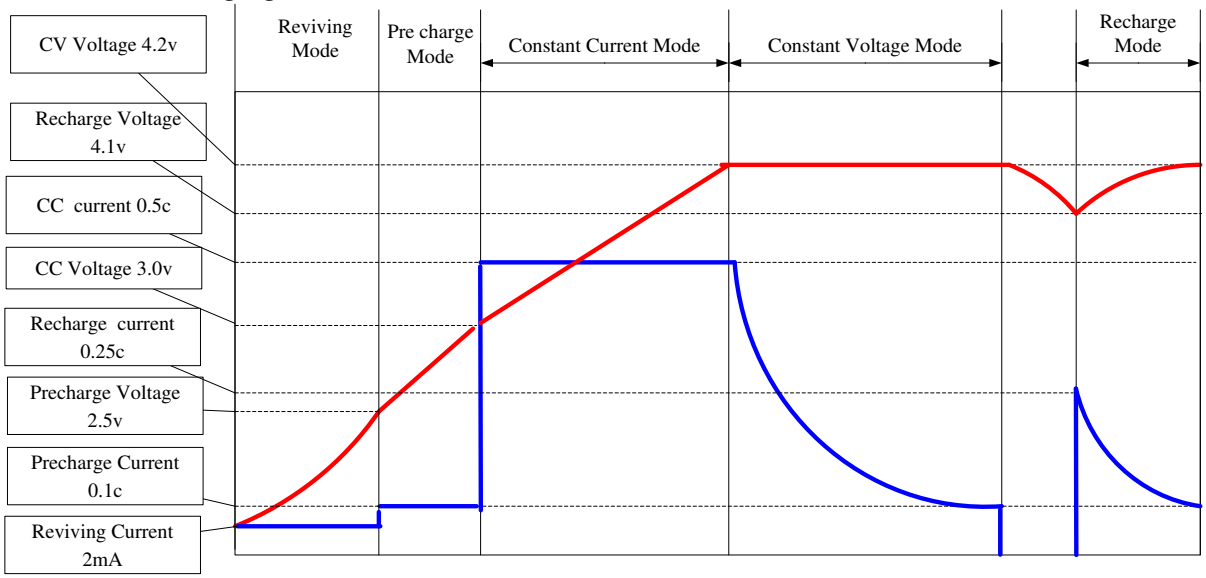
The on-chip Power management Unit (PMU) has two main feature; Li-Ion battery charging and voltage regulation. A power switch is used to switch over the power source between battery and adaptor automatically. The PMU also provides driving current for 2 LEDs.

7.1 CHARGING A BATTERY

IS1690S chip has a built-in battery charger which is optimized for Li-ion batteries. The charger includes a current sensor for charging control, user programmable current regulation and high accuracy voltage regulation.

The charging current parameters are configured in the EEPROM. Whenever the adaptor is plug-in, the charging circuit will be activated. Reviving, Pre-charging, Constant Current and Constant Voltage modes are implemented and re-charging function is also included. The maximum charging current is 350mA.

FIGURE 7-1: Charging curve



7.2 VOLTAGE MONITORING

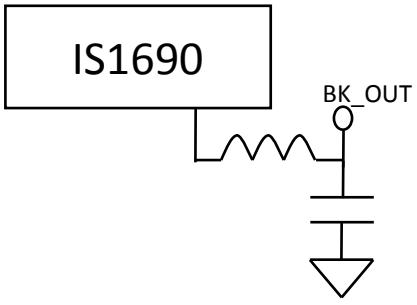
A 10-bit Successive-Approximation-Register analog to digital converter (SAR ADC) provides one dedicated channel for battery voltage level detection. The warning level is programmable and stored in the EEPROM. This ADC provides a good resolution that MCU can control the charging process.

7.3 LDO

The built-in LDO is used to convert the battery or adaptor power for power supply. It also integrates hardware architecture to control power on/off procedure. The built-in programmable LDOs provide power for codec and digital IO pads. It is used to buffer the high input voltage from battery or adapter. This LDO needs 1uF bypass capacitor.

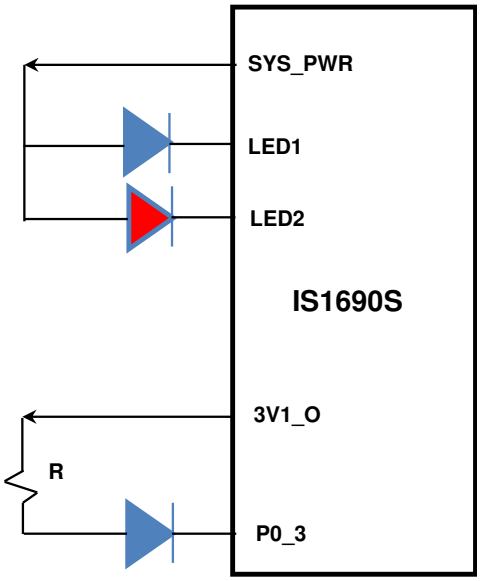
7.4 SWITCHING REGULATOR

The built-in programmable output voltage regulator can convert battery voltage for RF and baseband core power supply. This converter has high conversion efficiency and fast transient response.



7.5 LED DRIVER

There are two dedicate LED drivers to control the LEDs. They provide enough sink current (16 step control and 0.35mA for each step) that LED can be connected directly with IS1690S. If the third LED is necessary, use P0_3 to light up LED, an external resistor to fine tune the driving current is necessary. Under this configuration, the power source must be VDD_IO, and the LED brightness could be adjusted by R(resister).



8.0 FUNCTION OF PIN

IS1690S audio chip provides six pins for key functions. The corresponding key functions are saved in EEPROM. The first button must be power key. The power on/off functions only can be set on MFB pin. There are four different operations for every button. They are short click, long click, double click and combinations.

TABLE 8-1: PINs for Buttons

Button Name	Default Functions	PIN name
Button 0	Power / MFB	PWR
Button 1	Volume UP	P0_1
Button 2	Volume DN	P1_6
Button 3	PLAY/PAUSE	P0_2
Button 4	REV	P0_5
Button 5	FWD	P3_7

Some signals were generated to indicate or control outside devices. The most popular applications are NFC for easy pairing, external audio amplifier for louder speaker.

TABLE 8-2: PINs for added functions

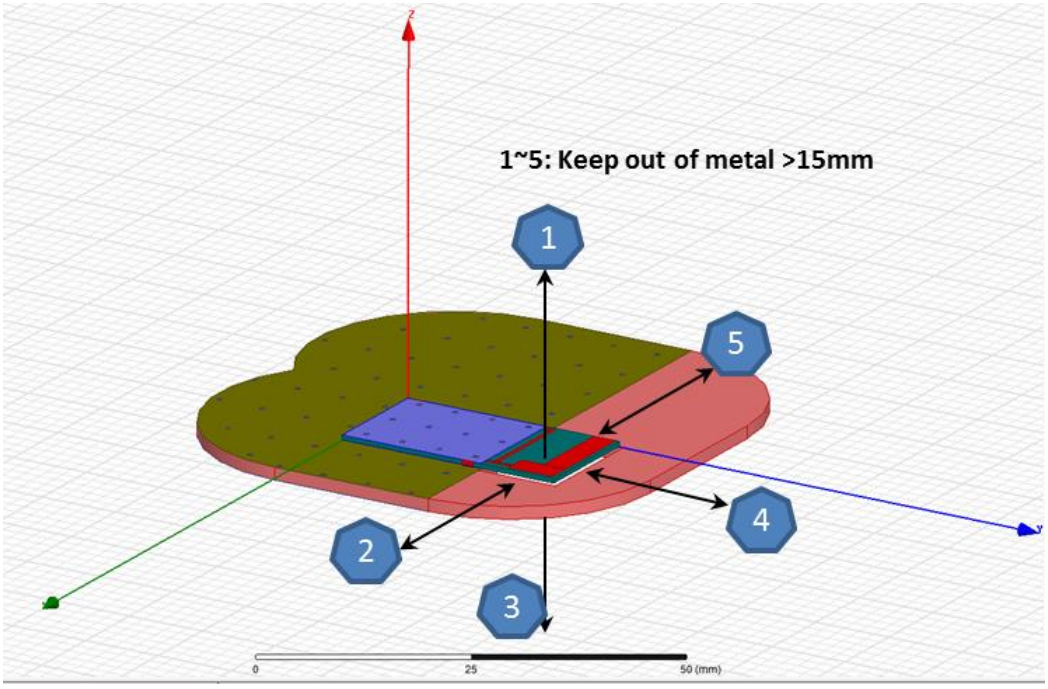
Functions	PIN configurable features
Slide switch	P3_4
PHONE	P3_5
NFC detect	P0_4
External amplifier enable	P0_0
3rd LED	P0_3

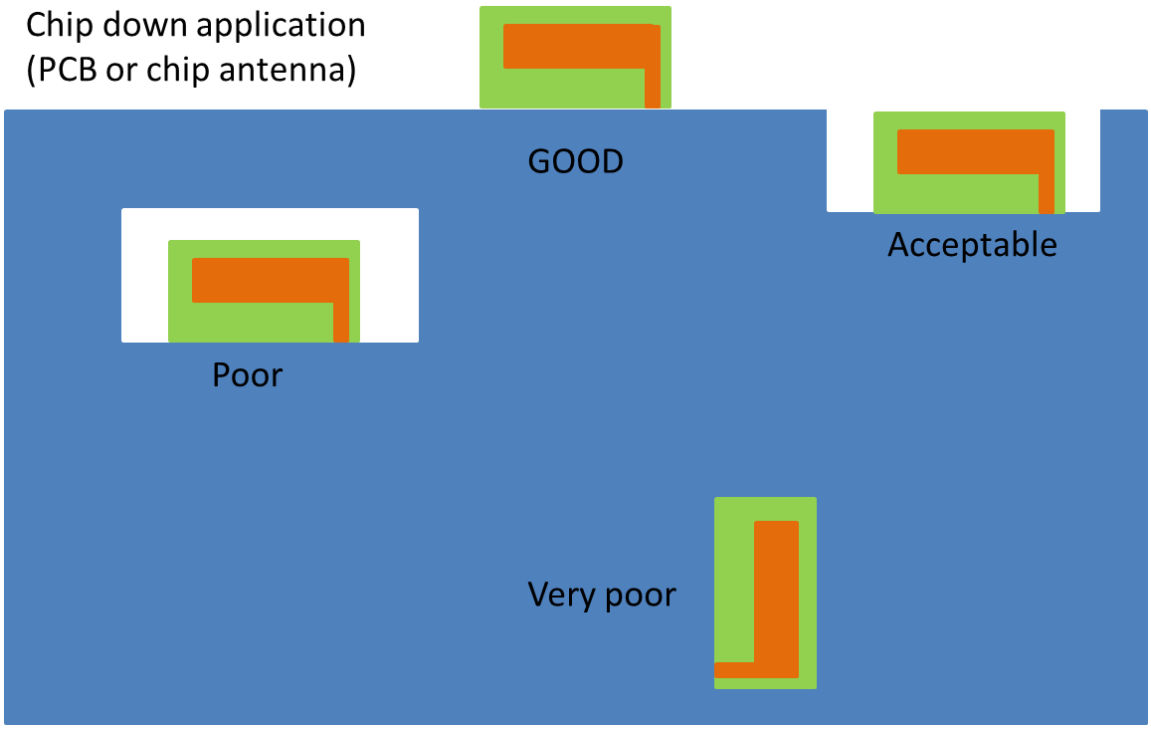
9.0 ANTENNA PLACEMENT RULE

For Bluetooth product, antenna placement will affect whole system performance.
Antenna need free space to transmit RF signal, it can't be surround by GND plane.

Here are some examples of good and poor placement on a PCB with GND plane.

FIGURE 9-1: ANTENNA PLACEMENT EXAMPLES





For more detail free space of antenna placement design, you can reference the design rule of antenna produce vendor.

10.0 SPECIFICATIONS

Table 10-1: Absolute Maximum Specifications

Symbol	Parameter	Min	Max	Unit
1V8	Digital core supply voltage	0	2.1	V
VCC_RF	RF supply voltage	0	2.1	V
SAR_VDD	SAR ADC supply voltage	0	2.1	V
VDDA/VDDAO	CODEC supply voltage	0	3.3	V
VDD_IO	I/O supply voltage	0	3.6	V
BK_VDD	BUCK supply voltage	0	4.3	V
3V1_IN	LDO Supply voltage	0	4.3	V
BAT_IN	Input voltage for battery	0	4.3	V
ADAP_IN	Input voltage for adaptor	0	7.0	V
T_{STORE}	Storage temperature	-65	+150	ºC
$T_{OPERATION}$	Operation temperature	-20	+70	ºC

Table 10-2: Recommended Operating Condition

Symbol	Parameter	Min	Typical	Max	Unit
1V8	Digital core supply voltage	1.8	1.85	1.95	V
VCC_RF	RF supply voltage	1.8	1.85	1.95	V
SAR_VDD	SAR ADC supply voltage	1.8	1.85	1.95	V
VDDA/VDDAO	CODEC supply voltage	1.7	2.8	3.0	V
VDD_IO	I/O supply voltage	2.8	3.0	3.3	V
BK_VDD	BUCK supply voltage	3	3.7	4.25	V
3V1_IN	LDO Supply voltage	3	3.7	4.25	V
BAT_IN	Input voltage for battery	3	3.7	4.25	V
ADP_IN	Input voltage for adaptor	4.5	5	5.5	V

*Absolute and Recommended operating condition tables reflect typical usage for device.
*All these supply voltage are programmable by EEPROM parameters.

Table 10-3: BUCK Switching Regulator

Parameter	Min	Typical	Max	Unit
Input Voltage	3.0	3.7	4.25	V
Output Voltage (I_{load}=70mA, Vin=4V)	1.71	1.85	1.89	V
Output Voltage Accuracy		±5		%
Output Voltage Adjustable Step		50		mV /Step
Output ripple		10		mV_{RMS}
Conversion efficiency (BAT=3.8V, I_{load} = 50mA)		86		%
Switching frequency		800		KHz
Quiescent Current (PFM)			80	µA
Output Current (peak)	200			mA
Load Regulation (I_{load} = 10 ~ 100mA)		1		mV/ mA
Line Regulation (3.2V < Vin < 4.2V)		0.03 (30)		%/V (mV/V)
Shutdown Current			<1	µA

*Test condition: SAR_VDD=1.8V, temperature=25 ºC.
*These parameters are characterized but not tested in manufacturing.

Table 10-4: Low Drop Regulator

Parameter		Min	Typical	Max	Unit
Input Voltage		3.0		4.25	V
Output Voltage	$V_{OUT\ CODEC}$ = 2.7V		2.8		V
	$V_{OUT\ CODEC}$ = 1.8V		1.8		
	$V_{OUT\ IO}$ = 3.1V		3.1		
	$V_{OUT\ IO}$ = 1.8V		1.8		
Output Accuracy (V_{IN}=3.7V, I_{LOAD}=100mA, 27'C)			±5		%
Output current (average)				100	mA
Drop-out voltage (I_{load} = maximum output current)				300	mV
Quiescent Current (excluding load, I_{load} < 1mA)			45		µA
Load Regulation (Iload = 0mA to 100mA)				40	mV
Line Regulation (Vout+0.3V<Vin<4.5V)			7	10	mV/V
Shutdown Current				<1	µA

*Test condition: SAR_VDD=1.8V, temperature=25 ºC.
*These parameters are characterized but not tested in manufacturing.

Table 10-5: Battery Charger

Parameter		Min	Typical	Max	Unit
Input Voltage		4.5	5.0	5.5	V
Battery trickle charge current (BAT_IN < trickle charge voltage threshold)			0.1C		mA
Maximum Battery Fast Charge Current Note: ENX2=0	Headroom > 0.7V (ADAP_IN=5V)	170	200	240	mA
	Headroom = 0.3V (ADAP_IN=4.5V)	160	180	240	mA
Maximum Battery Fast Charge Current Note: ENX2=1	Headroom > 0.7V (ADAP_IN=5V)	330	350	420	mA
	Headroom = 0.3V (ADAP_IN=4.5V)	180	220	270	mA
Trickle Charge Voltage Threshold			3		V
Float Voltage		4.158	4.2	4.242	V
Battery Charge Termination Current, (% of Fast Charge Current)			10		%

Note:
(1) C is set in EEPROM
(2) Headroom = $V_{ADAP\_IN} – V_{BAT}$
(3) ENX2 is not allowed to be enabled when $V_{ADAP\_IN} – V_{BAT} > 2V$
(4)These parameters are characterized but not tested in manufacturing.

Table 10-6: LED Driver

Parameter	Min	Typical	Max	Unit
Open-drain Voltage			3.6	V
Open-drain Current	0		5.25	mA
Intensity Control		16		step
Current Step		0.35		mA
Power Down Open-drain Current			1	µA
Shutdown Current			1	µA

*Test condition: SAR_VDD=1.8V, temperature=25 ºC.
*These parameters are characterized but not tested in manufacturing.

Table 10-7: Audio Codec Digital To Analogue Converter

T= 25°C, VDDA/VDDAO=2.8V, 1KHz sine wave input, Bandwidth = 20~20KHz					
Parameter (Condition)		**Min.**	**Typ.**	**Max.**	**Unit**
Over-sampling rate			128		f_s
Resolution			16		Bits
Output Sample Rate		8		48	KHz
Signal to Noise Ratio **Note: 1** (SNR @line-load) for 48kHz			94		dB
Signal to Noise Ratio (SNR @earphone load 16Ω load, 0dBFS input relative to digital silence)				94	dB
Digital Gain		-54		0	dB
Analog Gain		-28		3	dB
Analog Gain Resolution			1		dB
Output Voltage Full-scale Swing (AVDD=2.8V)			792		mV rms
Maximum Output Power (16Ω load)			34		mW
Maximum Output Power (32Ω load)			17		mW
Allowed Load	Resistive	8	16	O.C.	Ω
	Capacitive			500	pF
THD+N (16Ω load)				0.05	%

Note:
(1) f_{in}=1KHz, B/W=20~20KHz, A-weighted, THD+N < 0.01%, 0dBFS signal, Load=100KΩ
(2) These parameters are characterized but not tested in manufacturing.
* O.C. : open circuit.

Table 10-8: Audio Codec Analogue To Digital Converter

T= 25°C, VDDA/VDDAO=2.8V, 1KHz sine wave input, Bandwidth = 20~20KHz					
Parameter (Condition)		**Min.**	**Typ.**	**Max.**	**Unit**
Resolution				16	Bits
Output Sample Rate		8		48	KHz
Signal to Noise Ratio **Note: 1** (SNR @MIC or Line-in mode)	8KHz		85		dB
	44.1KHz/48KHz		85		
Digital Gain		-54		4.85	dB
MIC Boost Gain			20		
Analog Gain				26	dB
Input full-scale at maximum gain (differential)			4		mV rms
Input full-scale at minimum gain (differential)			800		mV rms
3dB bandwidth			20		KHz
Microphone mode (input impedance)			6	10	KΩ
THD+N (microphone input) @30mVrms input			0.04		%

Note:
(1) f_{in}=1KHz, B/W=20~20KHz, A-weighted, THD+N < 1%, 150mVpp input
(2)These parameters are characterized but not tested in manufacturing.

Table 10-9: Transmitter section for BDR

Parameter	Min	Typ	Max	Bluetooth specification	Unit
Maximum RF transmit power		3	4.0	-6 to 4	dBm
RF power control range		20		≥16	dB
20dB bandwidth for modulated carrier		900		≤1000	KHz

*Test condition: VCC_RF= 1.8V, temperature=25 ºC.
*The RF Transmit power is calibrated during production using MP Tool software and MT8852 Bluetooth Test equipment.

Table 10-10: Transmitter section for EDR

	Min	Typ	Max	Bluetooth specification	Unit
Relative transmit power		-1.6		-4 to 1	dB

*Test condition: VCC_RF= 1.8V, temperature=25 ºC.
*The RF Transmit power is calibrated during production using MP Tool software and MT8852 Bluetooth Test equipment.

Table 10-11: Receiver section for BDR

	Min	Typ	Max	Bluetooth specification	Unit
Sensitivity at 0.1% BER		-91		≤-70	dBm

Table 10-12: Receiver section for EDR

	Modulation	Min	Typ	Max	Bluetooth specification	Unit
Sensitivity at 0.01% BER	π/4 DQPSK		-92		≤-70	dBm
	8DPSK		-84		≤-70	dBm

*Test condition: VCC_RF= 1.8V, temperature=25 ºC.

11.0 MULTI-SPEAKER

IS1690S is designed for stereo Bluetooth multi speaker & speaker phone application with stereo aux in input function.

11.1 TWIN SPEAKER LINK TECHNOLOGY INTRODUCTION

Twin Speaker can be configured as

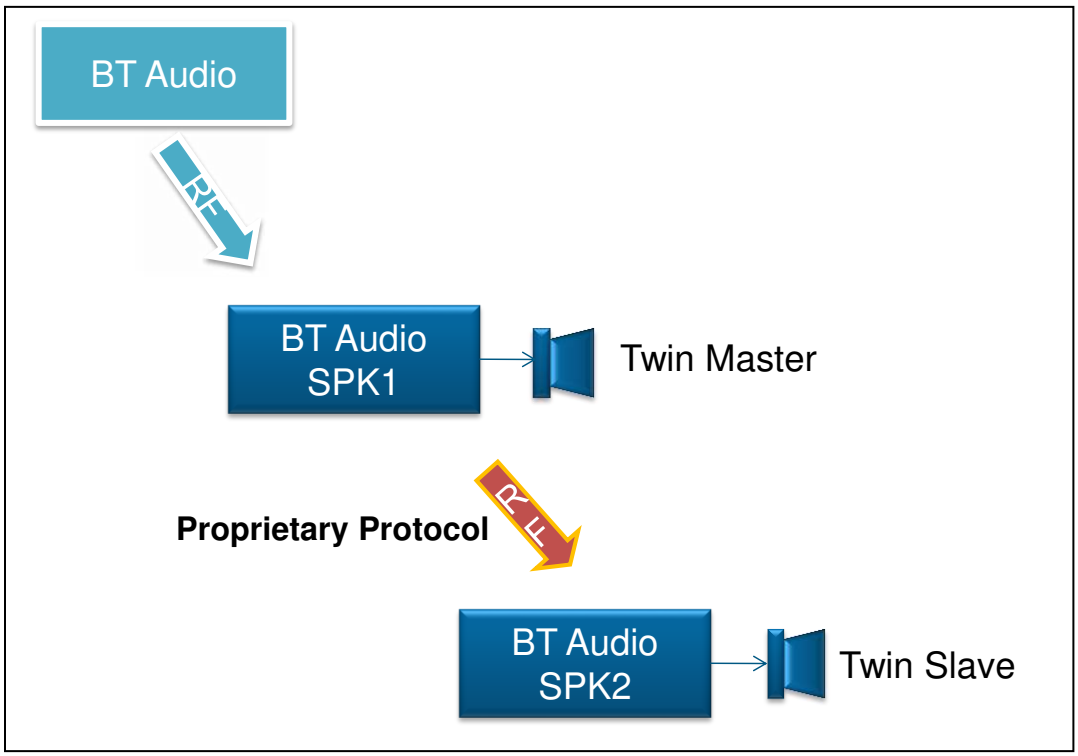
- Double Mode: Both Speakers output the mixed L and R channel.
- Stereo Mode: Both Speakers output the separated L and R channel

11.1.1 TWIN SPEAKER LINK

Figure 11-1 illustrates the concept of Twin Speaker link technology. In order to speed up the Twin Speaker link establishment and optimize the audio synchronization, Twin Speaker Link is a Bluetooth proprietary A2DP link between both Twin Master and Twin Slave Speakers.

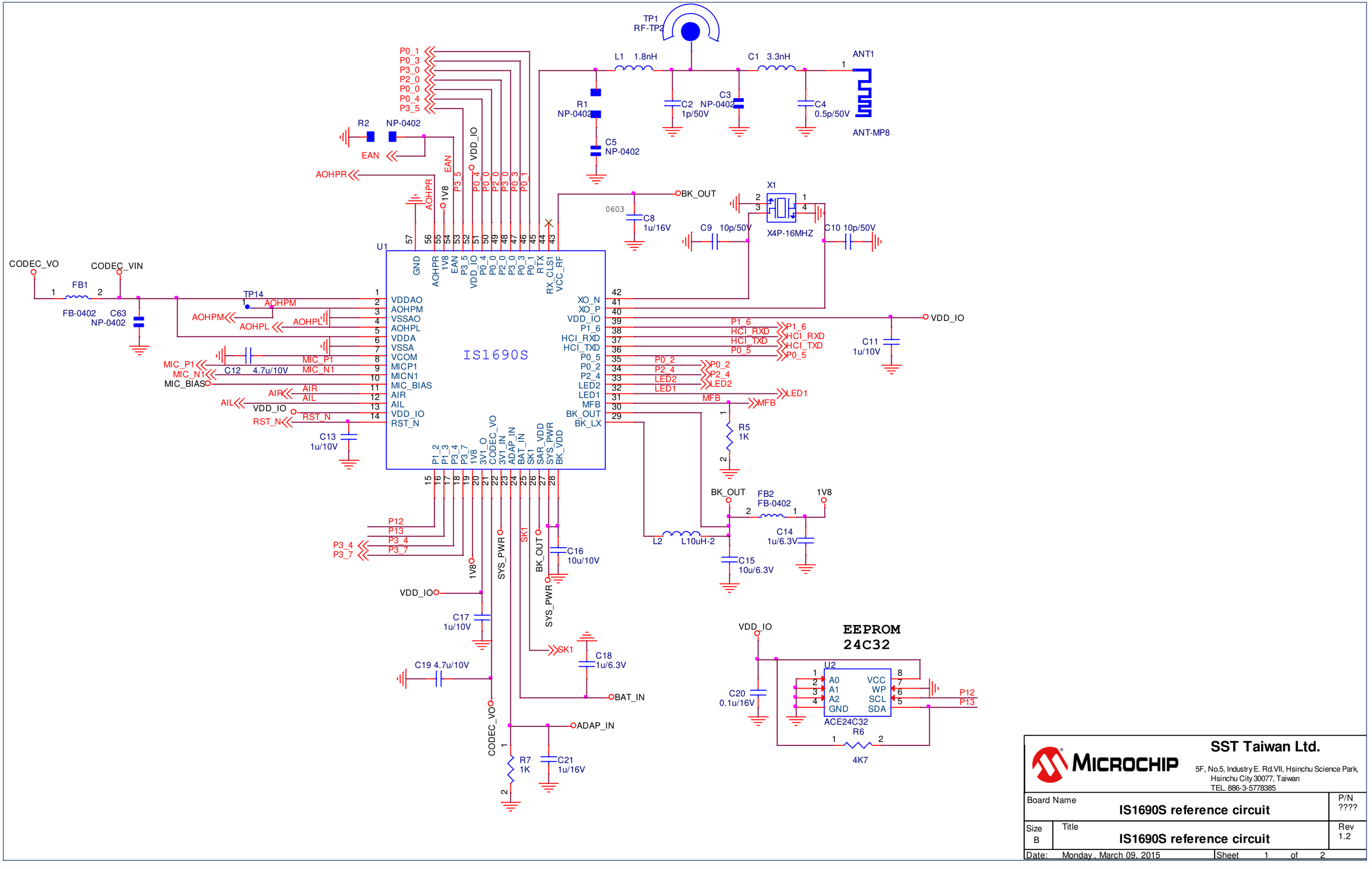
- **Twin_Master:**
  - It can be setup the standard HF, A2DP and AVRCP link with host Bluetooth devices like mobile phone and Notebook.
  - It will also take the responsibility to setup proprietary A2DP link with the other Twin_Slave speaker.
  - Once the Twin Speaker Link is established, Twin_Master will redirect the A2DP media packets and control signaling to Twin_Slave Speaker.
  - Notice: The voice channel (SCO link) and HF operation can be executed by Twin_Master operating only.
- **Twin_Slave:**
  - It can only be operated with Twin_Master by proprietary A2DP protocol. It cannot be connected by standard A2DP protocol.
  - Once the Twin Speaker Link is established, it can feedback the specific status and event to Twin_Master. These status and events include button operation, low battery voltage, power off event etc.

Figure 11-1 A2DP Twin Speaker Link Diagram



12.0 REFERENCE CIRCUIT

FIGURE 12-1: IS1690S reference circuit



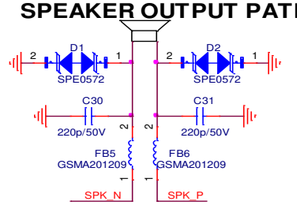
MICROCHIP

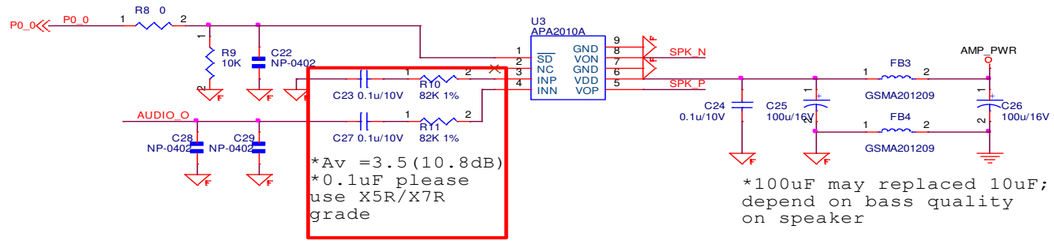
SST Taiwan Ltd.

5F, No.5, Industry E. Rd.VII, Hsinchu Science Park,
Hsinchu City 30077, Taiwan
TEL. 886-3-5778385

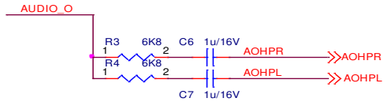
Board Name: **IS1690S reference circuit**		P/N: ????
Size: B	Title: **IS1690S reference circuit**	Rev: 1.2
Date: Monday, March 09, 2015	Sheet 1 of 2	

SPEAKER OUTPUT PATH



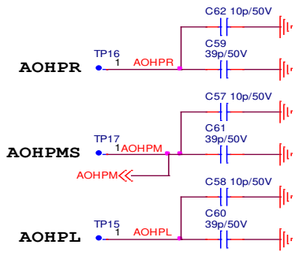


*AMP GND should be layout out independantly

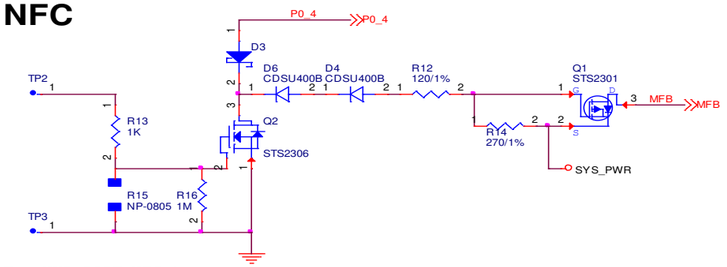


Single-ended input mode AMP (OPTION)

STEREO OUTPUT

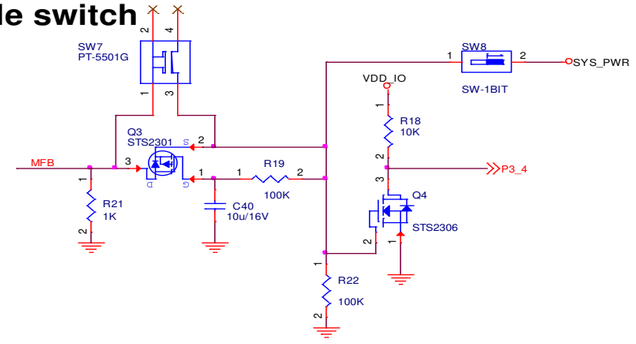


NFC

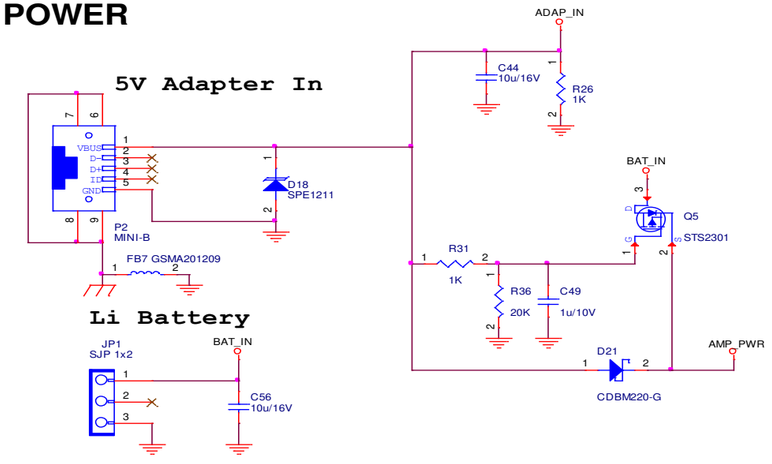


For NXP 203F NFC type, which build-in rectifier circuit

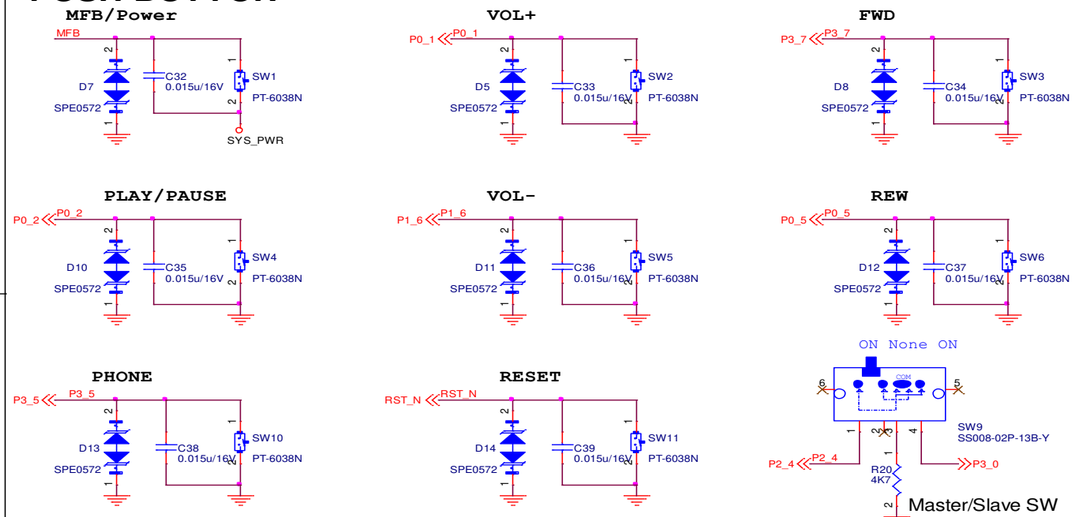
Slide switch



POWER

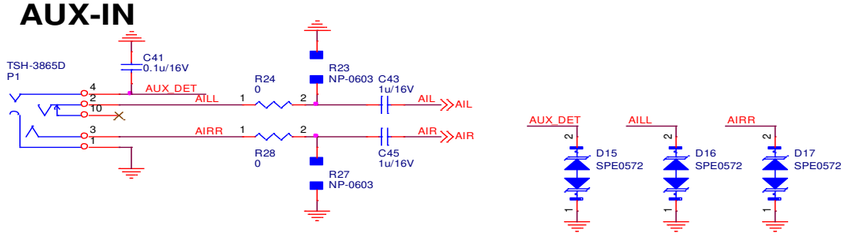


PUSH BUTTON

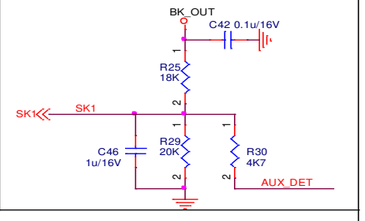


All ESD diodes in this schematics are reserved for testingand canbe removed if ESD can be pass without adding it.

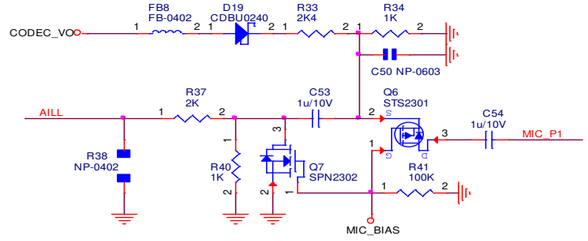
AUX-IN



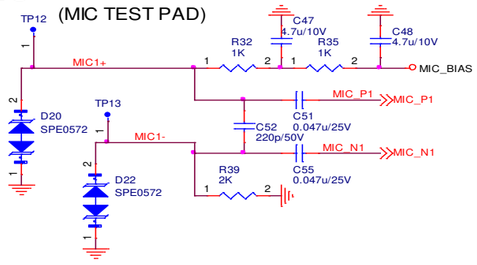
LINE-IN DETECTION



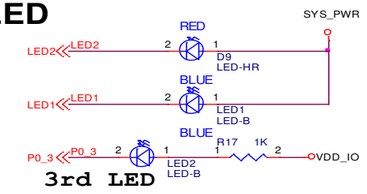
Line In Silence Detect



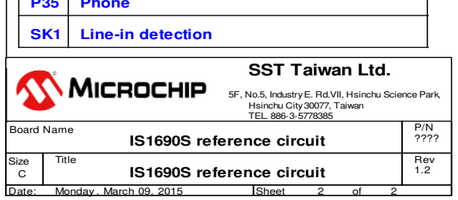
MIC



LED



TEST PAD



GPIO vs. APPLICATIO FUNCTION

P00	Audio AMP Enable
P01	Volume up
P02	Play/Pause
P03	3rd LED / DRC INDICATION
P04	NFC
P05	REW
P16	Volume down
P20	System Configuration
P24	System Configuration / N_SPK Role / L-CH
P30	N_SPK Role / R-CH
P34	SLIDE SWITCH
P37	FWD
P35	Phone
SK1	Line-in detection

MICROCHIP
SST Taiwan Ltd.
5F, No.5, Industry E. Rd.VII, Hsinchu Science Park, Hsinchu City 30077, Taiwan
TEL: 886-3-5778385

Board Name	IS1690S reference circuit	P/N ????
Size C	Title IS1690S reference circuit	Rev 1.2
Date: Monday, March 09, 2015	Sheet 2 of 2	

13.0 PACKING INFORMATION
13.1 CHIP IDENTIFICATION SYSTEM

PART NO.	X	-Y
(Chip Name)	(Package Type)	(Version)

Chip name: IS1690

Package Type: S = QFN (Saw Type) Package
GM = LGA Type and Flash Embedded Package

Version: e.g. “-203” is means the chip version is 203.

Examples:

IS1690S-205: 205 version ROM type IS1690 chip in QFN type package.

.

13.2 PACKAGE MARKING INFORMATION

56 Lead QFN (7x7x0.9 mm)

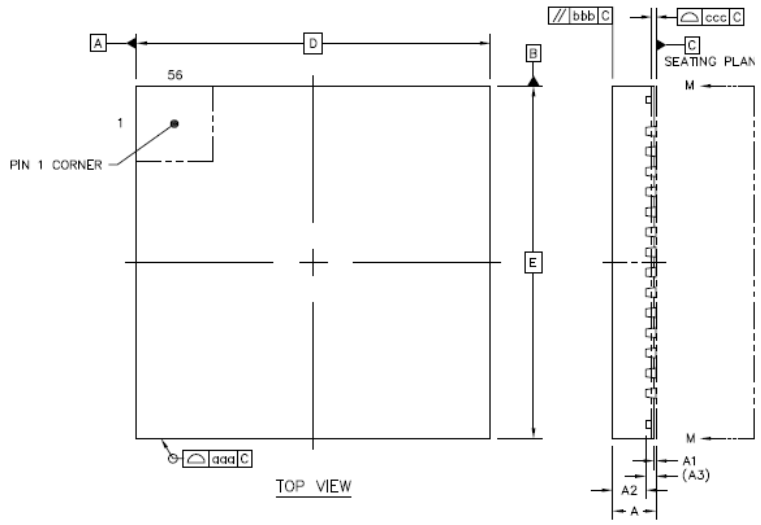
Example

Legend:

XXX: Chip serial number version and e3 Pb-free JEDEC designator for Matte Tin (Sn)
YY: Year code (last 2 digits of calendar year)
WW: Week code (week of January 1 is week “1”)
NNN: Alphanumeric traceability code

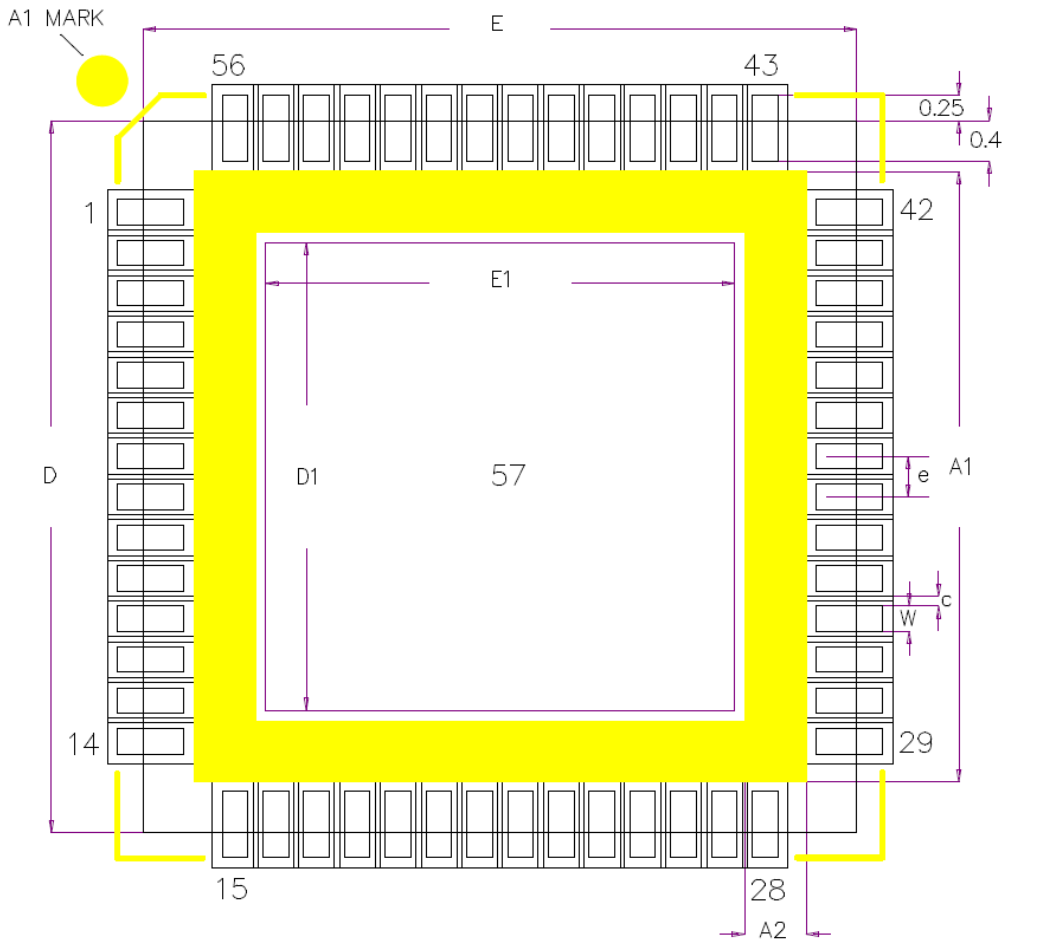
13.3 PACKAGE DETAIL

QFN56 7x7 Chip Outline



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.8	0.85	0.9
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.65	0.67
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.15	0.2	0.25
BODY SIZE	X	D		7 BSC	
	Y	E		7 BSC	
LEAD PITCH		e		0.4 BSC	
EP SIZE	X	J	4.5	4.6	4.7
	Y	K	4.5	4.6	4.7
LEAD LENGTH		L	0.35	0.4	0.45
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	

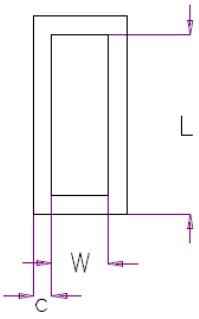
QFN56 7x7 PCB Footprint



TOP VIEW

	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOR.	MAX.
SILKSCREEN TOP L	A1		6	REF
SILKSCREEN TOP W	A2		0.6	REF
BODY SIZE	D		7	BSC
	E		7	BSC
EXPOSED PAD SIZE	D1		4.6	BSC
	E1		4.6	BSC
LEAD LENGTH	L		0.65	
LEAD WIDTH	W		0.25	
SOLDER MASKER OPEN	c		0.1	
LEAD PICTH	e		0.4	
LEAD COUNT	n1		56	

UNIT : MM



SOLDERMASK OPENING OUTSIDE OF LAND

SCALE 2:1

14.0 REFLOW PROFILE AND STORAGE CONDITION

14.1 STENCIL OF SMT ASSEMBLY SUGGESTION

14.1.1 STENCIL TYPE & THICKNESS

- Laser cutting
- Stainless steel
- Thickness

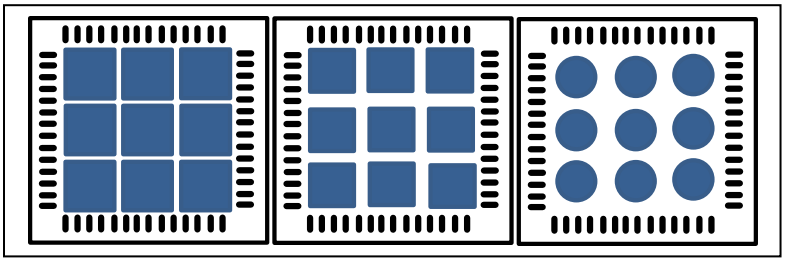
  0.5 mm Pitch : thickness < 0.15 mm

14.1.2 APERTURE SIZE AND SHAPE FOR TERMINAL PAD

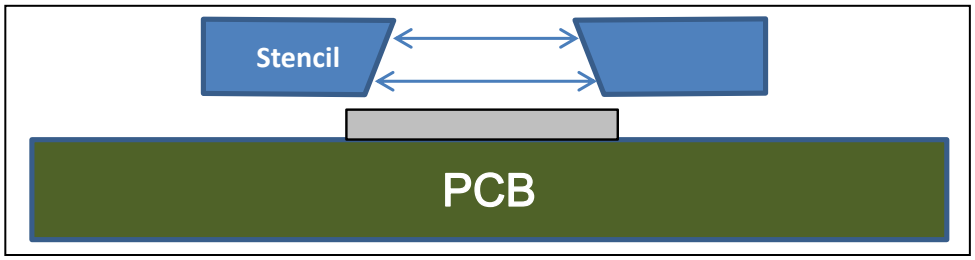
- Aspect ratio (width/thickness) > 1.5
- Aperture shape
  - The stencil aperture is typically designed to match the pad size on the PCB.
  - Oval-shaped opening should be used to get the optimum paste release.
  - Rounded corners to minimize clogging.
  - Positive taper walls (5o tapering) with bottom opening larger than the top.

14.1.3 APERTURE DESIGN FOR THERMAL PAD

- The small multiple openings should be used in steady of one big opening.
- 60~80% solder paste coverage
- Rounded corners to minimize clogging
- Positive taper walls (5° tapering) with bottom opening larger than the top



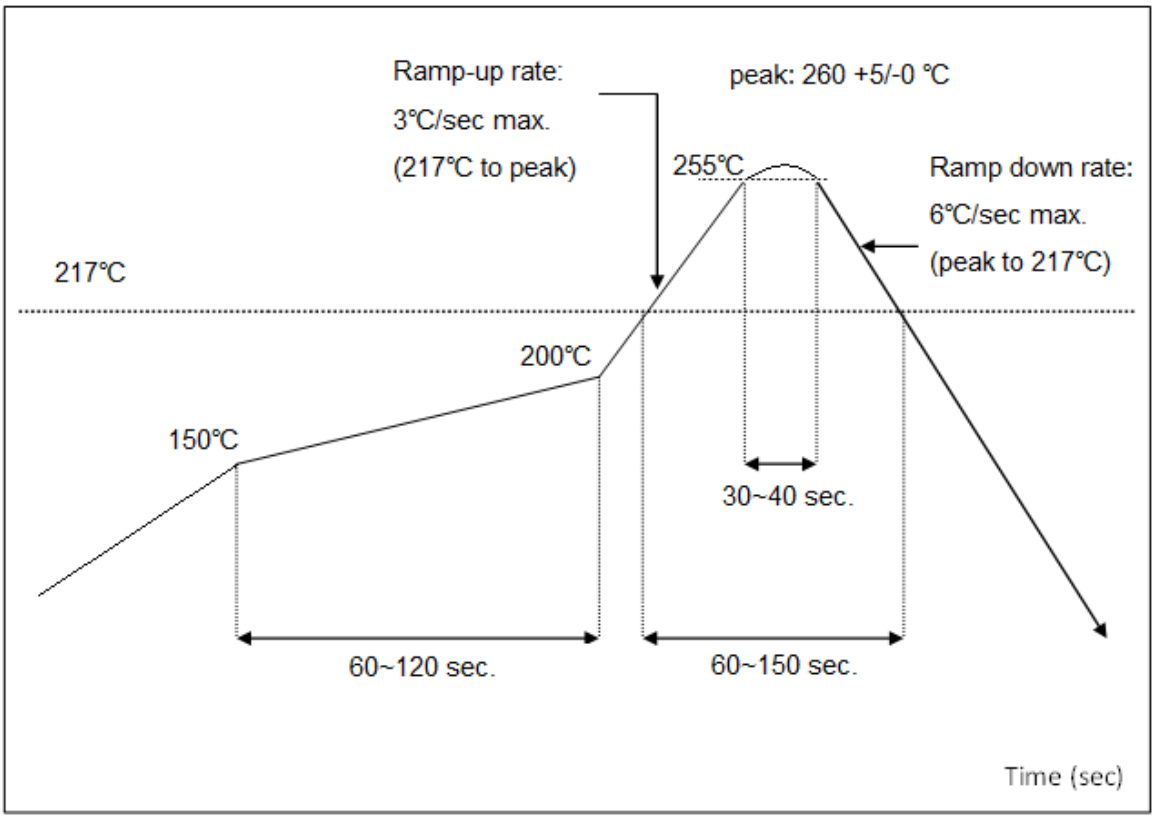
Don't recommend Coverage 91%　　Recommend Coverage 77%　　Recommend Coverage 65%



14.2 REFLOW CONDITION

Standard : IPC/JEDEC J-STD-020
Condition :
Preheat：150~200℃、60~120 seconds
Average ramp-up rate (217℃ to peak): 3℃/sec max.
Temperature maintained above 217℃ : 60~150 seconds
Time within 5℃ of peak temperature: 30 ~ 40 seconds.
Peak temperature：260 +5/-0 ℃
Ramp-down rate (peak to 217℃) : 6℃/sec. max.
Time 25℃ to peak temperature : 8 minutes max.
Cycle interval：5 minutes

FIGURE 14-1: Reflow Profile



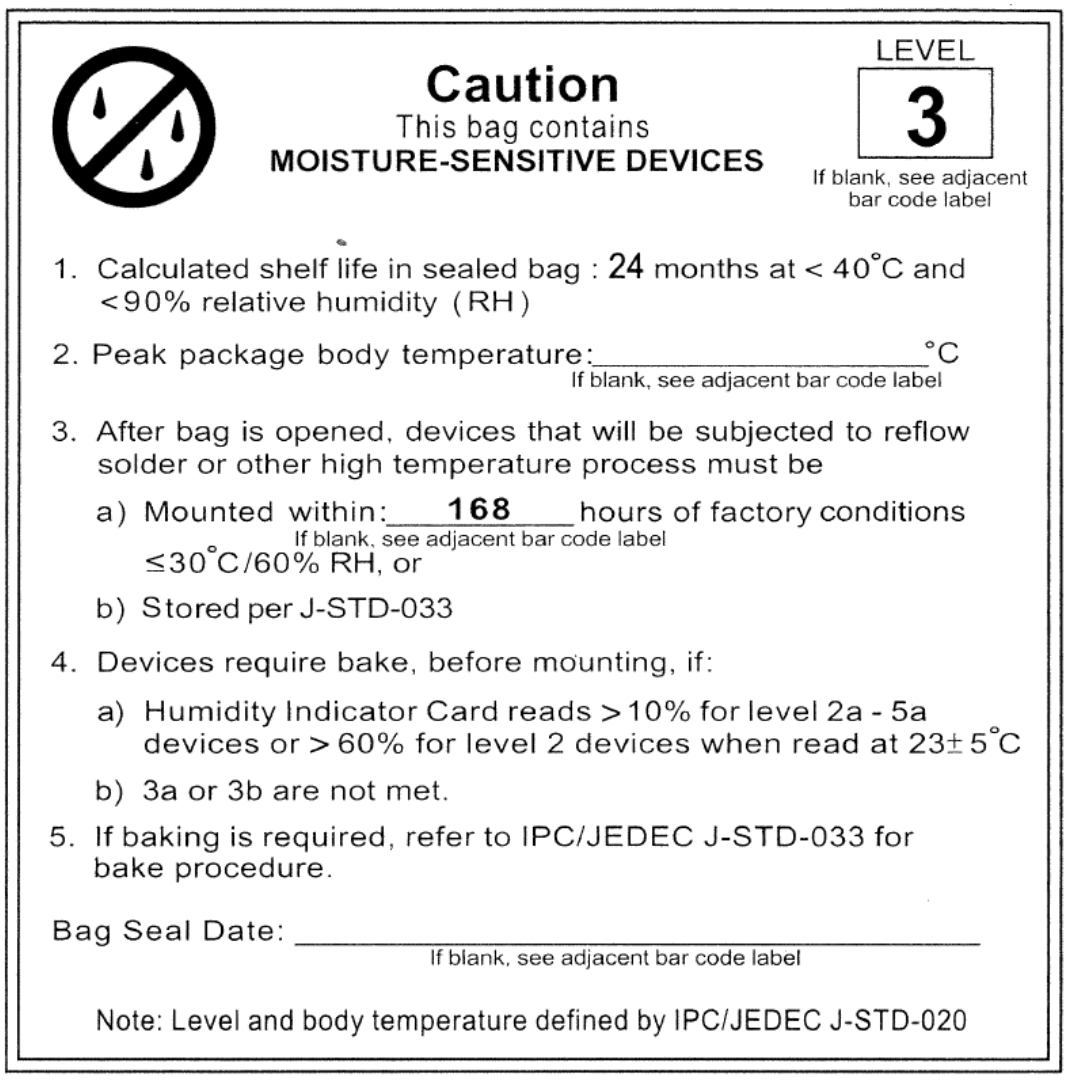
* For reference.

14.3 STORAGE CONDITION

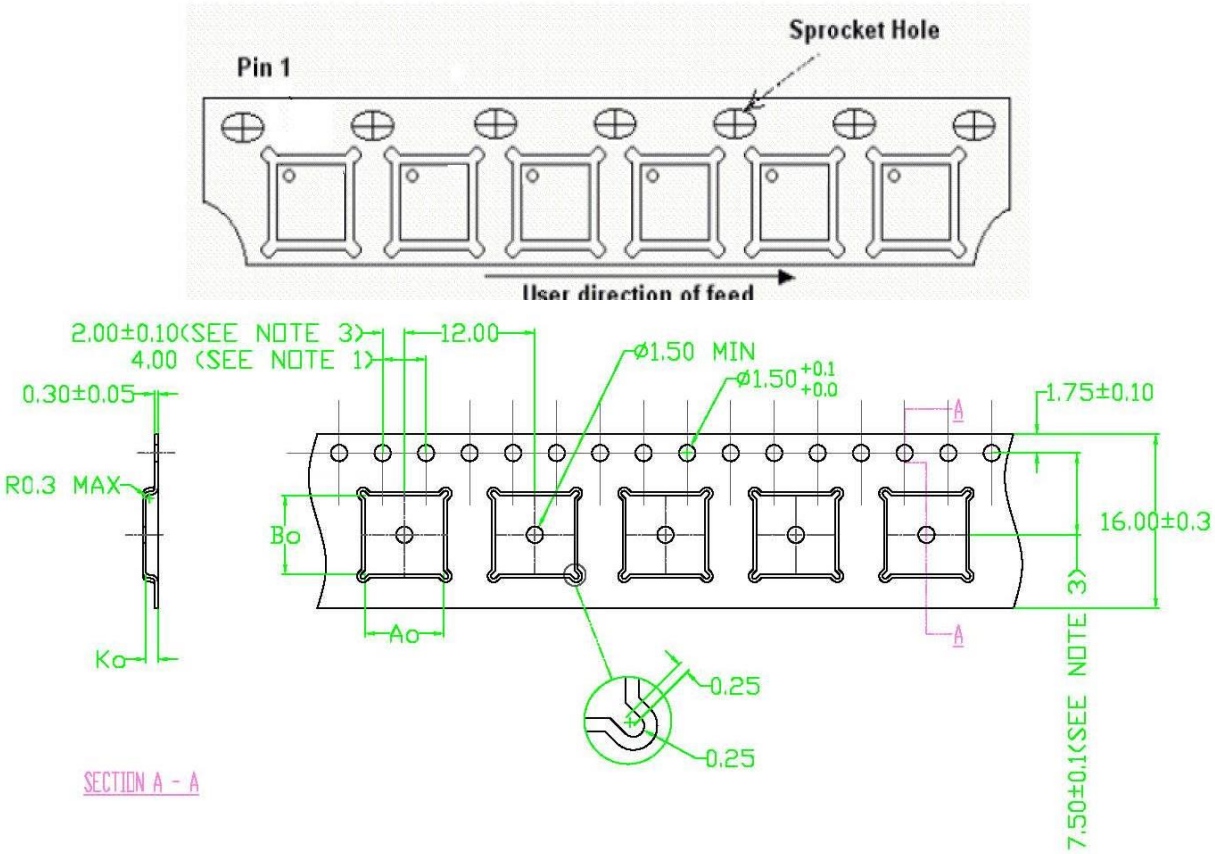
1. Calculated shelf life in sealed bag: 24 months at < 40 ℃ and <90% relative humidity (RH)
2. After bag is opened, devices that will be subjected to reflow solder or other high temperature process must be Mounted within 168 hours of factory conditions <30℃/60% RH

FIGURE 14-2: LABEL OF CHIP BAG

(Please notice the baking requirement)

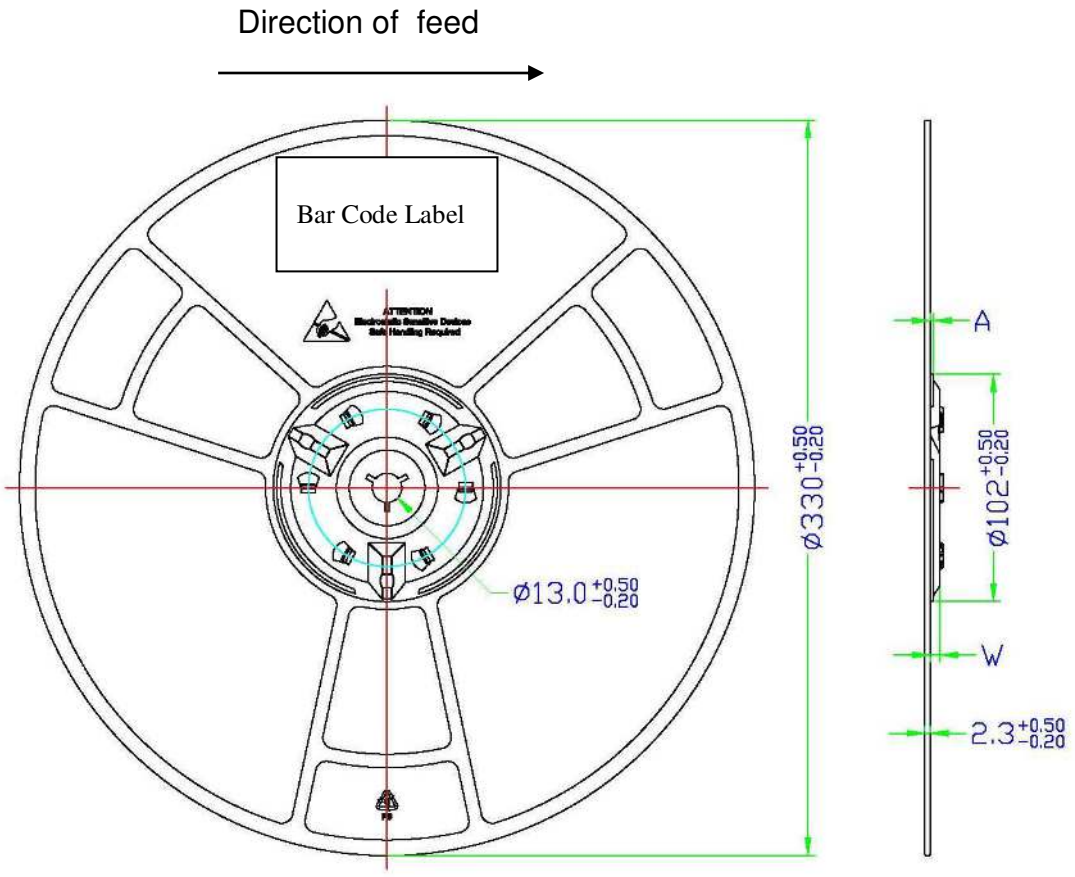


14.4 TAPE DIMENSION



A_0	B_0	K_0	Unit	Notes
7.25	7.25	1.10	mm	1. 10 sprocket hole pitch cumulative tolerance ±0.2 2. Material: PS + C 3. Camber not to exceed 1mm in 100 mm 4. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.

14.5 Reel Information



Package Type	Nominal Hub Width (Tape Width)	A	W	Units
QFN 7x7x0.9 mm	16	4.5	16.4 (+0.3/-0.2)	mm

Note:

Minimum Order Quantity is 3000 Tape & Reel