

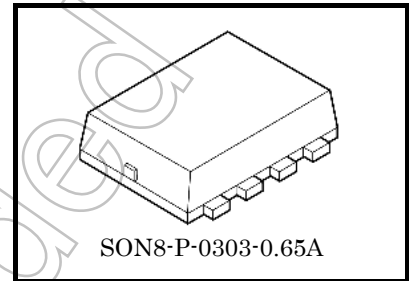
# TB7107FN

## Buck DC-DC Converter IC

The TB7107FN is a single-chip buck DC-DC converter IC utilizing a chopper circuit. The TB7107FN adopts bootstrap system and contains high-speed and low-on-resistance N-channel MOSFETs for the high side main switch to achieve high efficiency.

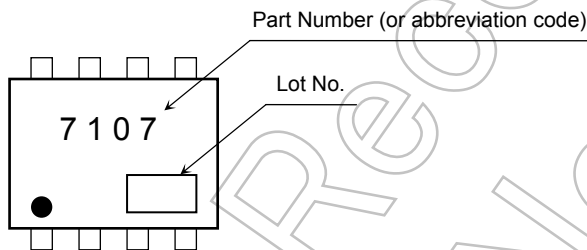
### Features

- Enables up to 2 A of load current (I<sub>OUT</sub>) with a minimum of external components.
- High efficiency:  $\eta = 87\%$  (typ.) (@V<sub>IN</sub> = 12 V, V<sub>OUT</sub> = 3.3 V and I<sub>OUT</sub> = 0.7A)
- Operating voltage range: V<sub>IN</sub> = 4.5 V to 20 V
- Low ON-resistance: R<sub>DS (ON)</sub> = 0.2  $\Omega$  (high-side) typical (@V<sub>IN</sub> = 12 V, T<sub>j</sub> = 25°C)
- Oscillation frequency: f<sub>OSC</sub> = 380 kHz (typ.)
- Reference voltage: V<sub>FB</sub> = 0.8 V  $\pm 2.25\%$  (@ T<sub>j</sub> = 25 °C)
- Because of an external phase compensation element, the optimal phase compensation according to the output filter capacitor can be realized.
- Allows the use of a small surface-mount ceramic capacitor as an output filter capacitor.
- Housed in a small surface-mount package (PS-8) with low thermal resistance.
- Soft-start time adjustable by an external capacitor



Weight: 0.017 g (typ.)

### Part Marking



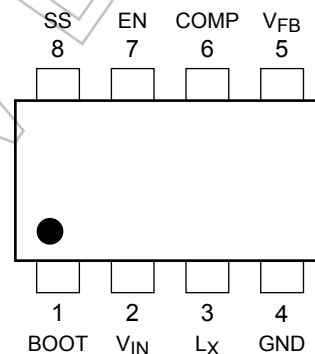
The dot (•) on the top surface indicates pin 1.

\*: The lot number consists of three digits. The first digit represents the last digit of the year of manufacture, and the following two digits indicates the week of manufacture between 01 and either 52 or 53.



Manufacturing week code  
(The first week of the year is 01; the last week is 52 or 53.)  
Manufacturing year code (last digit of the year of manufacture)

### Pin Assignment



This product has a MOS structure and is sensitive to electrostatic discharge. Handle with care.

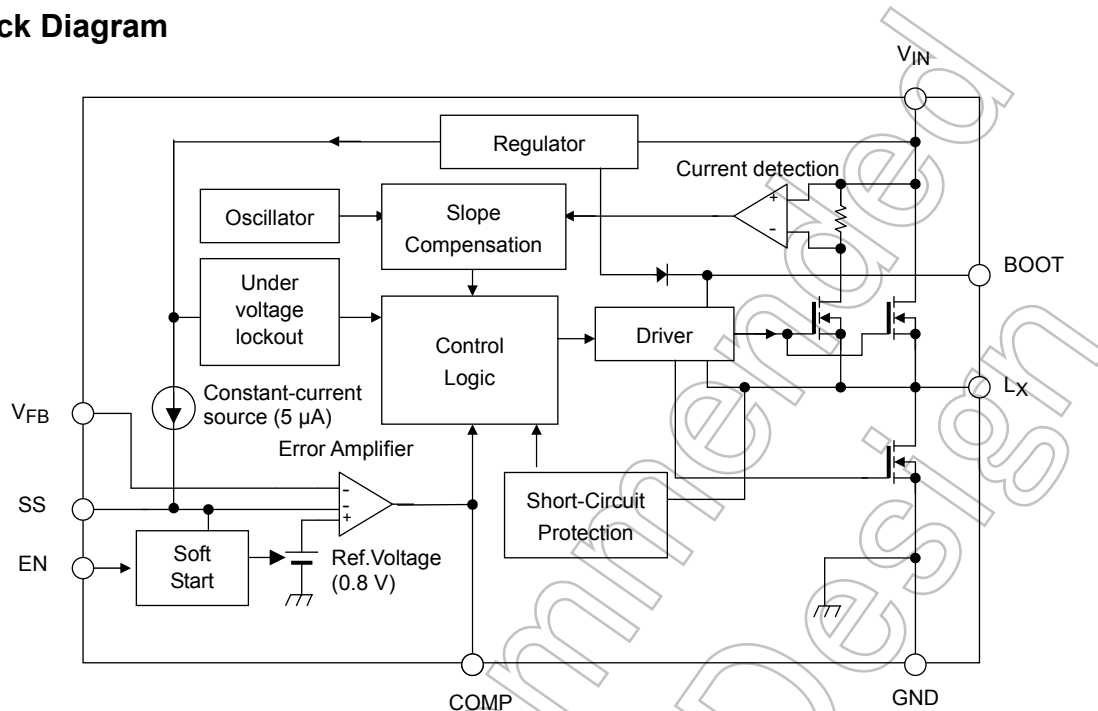
The product(s) in this document (“Product”) contain functions intended to protect the Product from temporary small overloads such as minor short-term overcurrent, or overheating. The protective functions do not necessarily protect Product under all circumstances. When incorporating Product into your system, please design the system to avoid such overloads upon the Product, and to shut down or otherwise relieve the Product of such overload conditions immediately upon occurrence. For details, please refer to the notes appearing below in this document and other documents referenced in this document.

Start of commercial production  
2009-10

## Ordering Information

Part Number	Shipping
TB7107FN (TE85L, F)	Embossed tape (3000 units per reel)

## Block Diagram



## Pin Description

Pin No.	Symbol	Description
1	BOOT	Bootstrap pin This pin is connected to Bootstrap capacitor. A 0.1 $\mu\text{F}$ bootstrap capacitor is required between BOOT pin and LX pin.
2	V <sub>IN</sub>	Input pin This pin is placed in the standby state if EN = low. Standby current is 60 $\mu\text{A}$ (@V <sub>IN</sub> =12V) or less.
3	L <sub>X</sub>	Switch pin This pin is connected to high-side N-channel MOSFET.
4	GND	Ground pin
5	V <sub>FB</sub>	Feedback pin This input is fed into an internal error amplifier with a reference voltage of 0.8 V (typ.).
6	COMP	Phase compensation pin Pin for connecting an error amplifier phase compensation resistor and capacitor.
7	EN	Enable pin When V <sub>EN</sub> $\geq$ 1.8 V (@ V <sub>IN</sub> = 12 V), the internal circuitry is allowed to operate and thus enable the switching operation of the output section. When V <sub>EN</sub> $\leq$ 0.5 V (@ V <sub>IN</sub> = 12 V), the internal circuitry is disabled, putting the TB7107FN in Standby mode. This pin has an internal pull-up current of 15 $\mu\text{A}$ (typ.).
8	SS	Soft-start pin The soft-start time can be adjusted with an external capacitor. The external capacitor is charged from a 5 $\mu\text{A}$ (typ.) constant-current source, and the reference voltage of the error amplifier is regulated between 0 V and 0.8 V. The external capacitor is discharged when EN = low and in case of undervoltage lockout or thermal shutdown.

## Absolute Maximum Ratings (Ta = 25°C)

Characteristics	Symbol	Rating	Unit
Input pin voltage	V <sub>IN</sub>	-0.3 to 25	V
Bootstrap pin voltage	V <sub>BOOT</sub>	-0.3 to 28	V
Bootstrap pin - Switch pin voltage	V <sub>BOOT</sub> - V <sub>LX</sub>	-0.3 to 6	V
Switch pin voltage (Note 1)	V <sub>LX</sub>	-0.3 to 25	V
Feedback pin voltage	V <sub>FB</sub>	-0.3 to 6	V
Enable pin voltage	V <sub>EN</sub>	-0.3 to 25	V
Soft-start pin voltage	V <sub>SS</sub>	-0.3 to 6	V
Phase compensation pin voltage	V <sub>COMP</sub>	-0.3 to 6	V
Switch pin current	I <sub>LX</sub>	-2.3	A
Power dissipation (Note 2)	P <sub>D</sub>	0.9	W
Operating junction temperature	T <sub>jopr</sub>	-40 to 125	°C
Junction temperature (Note 3)	T <sub>j</sub>	150	°C
Storage temperature	T <sub>stg</sub>	-55 to 150	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

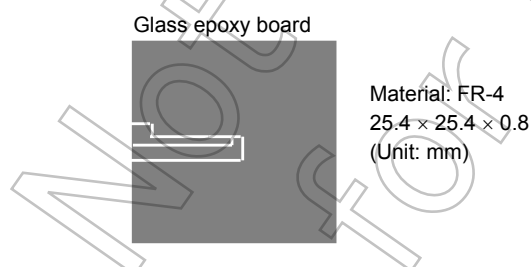
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc)

Note 1: The switch pin voltage (V<sub>LX</sub>) doesn't include the peak voltage generated by TB7107FN's switching.

## Thermal Resistance Characteristics

Characteristics	Symbol	Max	Unit
Thermal resistance, junction to ambient	R <sub>th(j-a)</sub>	110.2 (Note 2)	°C/W

Note 2:



Note 3: The TB7107FN may go into thermal shutdown at the rated maximum junction temperature. Thermal design is required to ensure that the rated maximum operating junction temperature, T<sub>jopr</sub>, will not be exceeded.

**Electrical Characteristics (T<sub>j</sub> = 25°C, V<sub>IN</sub> = 4.5 to 20 V, unless otherwise specified)**

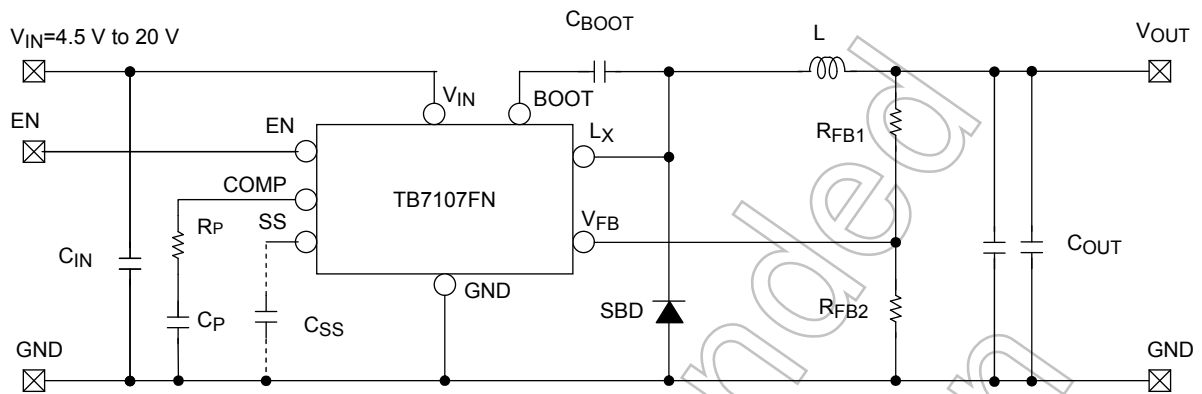
Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit	
Operating input voltage	V <sub>IN(OPR)</sub>	—	4.5	—	20	V	
Operating current	I <sub>IN</sub>	V <sub>IN</sub> = 12V, V <sub>EN</sub> = 5V, V <sub>F<sub>FB</sub></sub> = 2 V	—	1.8	2.5	mA	
Output voltage range	V <sub>OUT(OPR)</sub>	V <sub>EN</sub> = V <sub>IN</sub>	0.8	—	V <sub>IN</sub> - 2	V	
Standby current	I <sub>IN(STBY)</sub>	V <sub>IN</sub> = 12 V, V <sub>EN</sub> = 0 V V <sub>F<sub>FB</sub></sub> = 0.8 V	—	—	60	μA	
High-side switch leakage current	I <sub>LEAK(H)</sub>	V <sub>IN</sub> = 12 V, V <sub>EN</sub> = 0 V V <sub>F<sub>FB</sub></sub> = 0.8 V, V <sub>LX</sub> = 0 V	—	—	10	μA	
EN threshold voltage	V <sub>I<sub>H</sub>(EN)</sub>	V <sub>IN</sub> = 12 V	1.8	—	—	V	
	V <sub>I<sub>L</sub>(EN)</sub>	V <sub>IN</sub> = 12V	—	—	0.5		
EN input current	I <sub>I<sub>H</sub>(EN)</sub>	V <sub>IN</sub> = 12V, V <sub>EN</sub> = 5 V	-5	—	5	μA	
	I <sub>I<sub>L</sub>(EN)</sub>	V <sub>IN</sub> = 12V, V <sub>EN</sub> = 0 V	—	-15	—		
V <sub>F<sub>FB</sub></sub> input voltage	V <sub>F<sub>FB</sub></sub>	V <sub>IN</sub> = 12 V, V <sub>EN</sub> = 5 V	0.782	0.8	0.818	V	
V <sub>F<sub>FB</sub></sub> input current	I <sub>F<sub>FB</sub></sub>	V <sub>IN</sub> = 12 V, V <sub>EN</sub> = 5 V V <sub>F<sub>FB</sub></sub> = 2V	-1	—	1	μA	
Phase compensation input current	I <sub>COMP(H)</sub>	V <sub>IN</sub> = 12 V, V <sub>EN</sub> = 5 V V <sub>F<sub>FB</sub></sub> = 0.7V, V <sub>COMP</sub> = 0.5 V	—	-40	—	μA	
	I <sub>COMP(L)</sub>	V <sub>IN</sub> = 12 V, V <sub>EN</sub> = 5 V V <sub>F<sub>FB</sub></sub> = 0.9V, V <sub>COMP</sub> = 0.5 V	—	40	—		
High-side switch on-state resistance	R <sub>DS(ON)(H)</sub>	V <sub>IN</sub> = 12V, V <sub>EN</sub> = 5V I <sub>LX</sub> = - 1A	—	0.2	—	Ω	
Low-side switch on-state resistance	R <sub>DS(ON)(L)</sub>	V <sub>IN</sub> = 12 V, V <sub>EN</sub> = 5 V I <sub>LX</sub> = 100 mA	—	1.5	—	Ω	
Oscillation frequency	f <sub>OSC</sub>	V <sub>IN</sub> = 12V, V <sub>EN</sub> = 5V	300	380	460	kHz	
Internal soft-start time	t <sub>SS</sub>	V <sub>IN</sub> = 12 V, V <sub>EN</sub> = 5V, I <sub>OUT</sub> = 0A Measured between 0% and 90%points at V <sub>OUT</sub>	0.5	1	2	ms	
External soft-start charge current	I <sub>SS</sub>	V <sub>IN</sub> = 12 V, V <sub>EN</sub> = 5 V	-3	-5	-8	μA	
High-side switch duty cycle	D <sub>max</sub>	V <sub>IN</sub> = 12 V, V <sub>EN</sub> = 5 V	—	88	—	%	
Thermal shutdown (TSD)	Detection temperature	T <sub>SD</sub>	V <sub>IN</sub> = 12 V, V <sub>EN</sub> = 5 V	—	160	—	°C
	Hysteresis	ΔT <sub>SD</sub>	V <sub>IN</sub> = 12 V, V <sub>EN</sub> = 5 V	—	15	—	
Undervoltage lockout (UVLO)	Detection voltage	V <sub>UV</sub>	V <sub>EN</sub> = V <sub>IN</sub>	2.9	3.2	3.5	V
	Recovery voltage	V <sub>UVR</sub>	V <sub>EN</sub> = V <sub>IN</sub>	3.2	3.5	3.8	
	Hysteresis	ΔV <sub>UV</sub>	V <sub>EN</sub> = V <sub>IN</sub>	—	0.3	—	
L <sub>X</sub> current limit	I <sub>LIM</sub>	V <sub>IN</sub> = 4.5V to 20 V, V <sub>EN</sub> = 5V V <sub>OUT</sub> = 2 V	2.9	3.5	—	A	

**Note on Electrical Characteristics**

The test condition T<sub>j</sub> = 25°C means a state where any drifts in electrical characteristics incurred by an increase in the chip's junction temperature can be ignored during pulse testing.

**Application Circuit Example**

Figure 1 shows a typical application circuit using a low-ESR electrolytic or ceramic capacitor for C<sub>OUT</sub>.



**Figure 1 TB7107FN Application Circuit Example**

Component values (reference value@ V<sub>IN</sub> = 12 V, V<sub>OUT</sub> = 3.3 V, T<sub>a</sub> = 25°C)

C<sub>IN</sub>: Input filter capacitor = 10 μF

(ceramic capacitor: GRM31CR71E106K manufactured by Murata Manufacturing Co., Ltd.)

C<sub>OUT</sub>: Output filter capacitor = 10 μF

(ceramic capacitor: GRM31CR71E106K manufactured by Murata Manufacturing Co., Ltd.)

R<sub>FB1</sub>: Output voltage setting resistor = 7.5 kΩ

R<sub>FB2</sub>: Output voltage setting resistor = 2.4 kΩ

C<sub>p</sub>: Phase compensation capacitance

R<sub>p</sub>: Phase compensation resistance

L: Inductor = 10 μH (SLF10165T-100M3R83PF or SLF7055T-100M2R5-3PF manufactured by TDK-EPC Corporation)

SBD: Schottky barrier diode CRS30I30A (manufactured by Toshiba Corporation)

C<sub>BOOT</sub>: Bootstrap capacitor = 0.1 μF (GRM188R71H104J manufactured by Murata Manufacturing Co., Ltd.)

C<sub>SS</sub> is a capacitor for adjusting the soft-start time.

**Examples of Component Values (For Reference Only)**

Output Voltage Setting V <sub>OUT</sub>	Inductance L	Input Capacitance C <sub>IN</sub>	Output Capacitance C <sub>OUT</sub>	Feedback Resistor R <sub>FB1</sub>	Feedback Resistor R <sub>FB2</sub>	Phase Compensation Capacitance C <sub>p</sub>	Phase Compensation Resistance R <sub>p</sub>
1.2 V	10 μH	10 μF	20 μF	7.5 kΩ	15 kΩ	4700 pF	10 kΩ
1.51 V	10 μH	10 μF	20 μF	16 kΩ	18 kΩ	4700 pF	10 kΩ
1.8 V	10 μH	10 μF	20 μF	15 kΩ	12 kΩ	2200 pF	15 kΩ
2.5 V	10 μH	10 μF	20 μF	5.1 kΩ	2.4 kΩ	2200 pF	22 kΩ
3.3 V	10 μH	10 μF	20 μF	7.5 kΩ	2.4 kΩ	2200 pF	22 kΩ
5.0V	10 μH	10 μF	20 μF	27 kΩ	5.1 kΩ	2200 pF	33 kΩ

Component values need to be adjusted, depending on the TB7107FN's I/O conditions and the board layout.

**Application Notes**

**Inductor Selection**

The inductance required for inductor L can be calculated as follows:

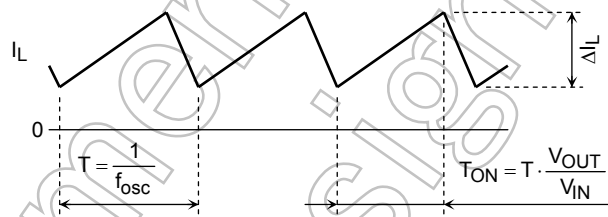
$$L = \frac{V_{IN} - V_{OUT}}{f_{OSC} \cdot \Delta I_L} \cdot \frac{V_{OUT}}{V_{IN}} \dots\dots\dots(1)$$

$V_{IN}$ : Input voltage (V)  
 $V_{OUT}$ : Output voltage (V)  
 $f_{OSC}$ : Oscillation frequency = 380 kHz (typ.)  
 $\Delta I_L$ : Inductor ripple current (A)

\*: Generally,  $\Delta I_L$  should be set to approximately 30% of the maximum output current. Since the maximum output current of the TB7107FN is 2.0 A,  $\Delta I_L$  should be 0.6 A or so. The inductor should have a current rating greater than the peak output current of 2.3 A. If the inductor current rating is exceeded, the inductor becomes saturated, leading to an unstable DC-DC converter operation.

When  $V_{IN} = 12\text{ V}$  and  $V_{OUT} = 3.3\text{ V}$ , the required inductance can be calculated as follows. Be sure to select an appropriate inductor, taking the input voltage range into account.

$$L = \frac{V_{IN} - V_{OUT}}{f_{OSC} \cdot \Delta I_L} \cdot \frac{V_{OUT}}{V_{IN}} = \frac{12\text{ V} - 3.3\text{ V}}{380\text{kHz} \cdot 0.6\text{ A}} \cdot \frac{3.3\text{ V}}{12\text{ V}} = 10.5\ \mu\text{H} \dots\dots\dots(2)$$

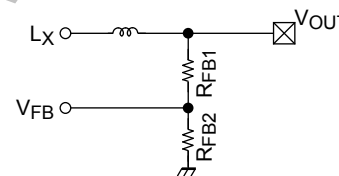


**Figure 2 Inductor Current Waveform**

**Setting the Output Voltage**

A resistive voltage divider is connected as shown in Figure 3 to set the output voltage; it is given by Equation 3 based on the reference voltage of the error amplifier (0.8 V typ.), which is connected to the Feedback pin, VFB. RFB1 should be up to 30 kΩ or so, because an extremely large-value RFB1 incurs a delay due to parasitic capacitance at the VFB pin. It is recommended that resistors with a precision of ±1% or higher be used for RFB1 and RFB2.

$$V_{OUT} = V_{FB} \cdot \left(1 + \frac{R_{FB1}}{R_{FB2}}\right) = 0.8\text{ V} \cdot \left(1 + \frac{R_{FB1}}{R_{FB2}}\right) \dots\dots\dots(3)$$



**Figure 3 Output Voltage Setting Resistors**

**Setting the Phase Compensation Circuit**

Connect a resistor (Rp) in series with a capacitor (Cp) to COMP pin as a phase compensation. The following calculated value provides an estimation of the constant of phase compensation.

$$F_0 = \frac{1}{2\pi} \cdot \frac{R_{FB2}}{R_{FB1} + R_{FB2}} \cdot G_m(EA)R_p \cdot \frac{G_m(IS)}{C_{OUT}}$$

$$F_z = \frac{1}{2\pi} \cdot \frac{1}{C_p \cdot R_p} \dots\dots\dots(4)$$

$F_0$ =Frequency in loop gain being 0dB  
 : Set approximately to one-tenth of the switching frequency  
 $F_z$ =Frequency of pole-zero  
 : Set approximately to one-tenth of the  $F_0$   
 Design value (reference):  
 $G_m(EA)$ =Error Amp  $G_m$  : 200(μS)  
 $G_m(IS)$ =Current detection circuit  $G_m$  : 4(S)

The optimum value of phase compensation may change with the characteristics of  $C_{OUT}$  and another. Carry out sufficient evaluation on an actual operating condition.

**Output Filter Capacitor Selection**

Use a low-ESR electrolytic or ceramic capacitor as the output filter capacitor. Since a capacitor is generally sensitive to temperature, choose one with excellent temperature characteristics. The large capacitance improves load response characteristics. As a rule of thumb, its capacitance should be 10 μF or greater for applications. The capacitance should be set to an optimal value that meets the system’s ripple voltage requirement and transient load response characteristics. Since the ceramic capacitor has a very low ESR value, it helps reduce the output ripple voltage; however, because the ceramic capacitor provides less phase margin, it should be thoroughly evaluated.

**Rectifier Selection**

A Schottky barrier diode should be externally connected to the TB7107FN as a rectifier between the L<sub>X</sub> and GND pins. It is recommended that either CRS30I30A, be used as the Schottky barrier diode. If a large voltage overshoot is on the L<sub>X</sub> pin, it reduces the voltage to connect a series CR network consisting of a resistor of R<sub>S</sub> = 4.7 Ω and a capacitor of C<sub>S</sub> = 470 pF with the Schottky barrier diode in parallel. Power loss of the Schottky barrier diode tends to increase due to an increased reverse current caused by the rise in ambient temperature and self-heating due to a supplied current. The rated current should therefore be derated to allow for such conditions in selecting an appropriate diode.

**Soft-Start Feature**

The TB7107FN has a soft-start feature.

If the SS pin is left open, the soft-start time, t<sub>SS</sub>, for V<sub>OUT</sub> defaults to 1 ms (typ.) internally.

The soft-start time can be extended by adding an external capacitor (C<sub>SS</sub>) between the SS and GND pins. The soft-start time can be calculated as follows:

$$t_{SS2} = 0.16 \cdot C_{SS} \dots\dots\dots(5)$$

t<sub>SS2</sub>: Soft-start time (in seconds) when an external capacitor is connected between SS and GND.  
 C<sub>SS</sub>: Capacitor value (μF)

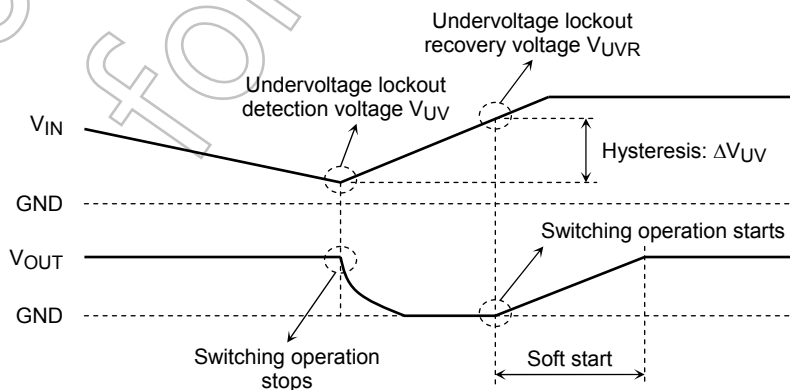
The soft-start feature is activated when the TB7107FN exits the undervoltage lockout (UVLO) state after power-up and when the voltage at the EN pin has changed from logic low to logic high.

**Overcurrent Protection (OCP)**

The TB7107FN has built-in overcurrent protection with pulse skip. When the peak current of L<sub>X</sub> pin exceeds I<sub>LIM</sub>=3.5A(typ.), the ON time of the high-side switch(internal) will be limited. Switching frequency will be reduced and output current will be restricted further if output voltage falls and the voltage of V<sub>FB</sub> pin drops below the overcurrent pulse skip detection voltage V<sub>LOC</sub> (0.3V typ.) during overcurrent protection .

**Undervoltage Lockout (UVLO)**

The TB7107FN has undervoltage lockout (UVLO) protection circuitry. The TB7107FN does not provide output voltage (V<sub>OUT</sub>) until the input voltage has reached V<sub>UVR</sub> (3.5 V typ.). UVLO has hysteresis of 0.3 V (typ.). After the switch turns on, if V<sub>IN</sub> drops below V<sub>UV</sub> (3.2 V typ.), UVLO shuts off the switch at V<sub>OUT</sub>.



**Figure 4 Undervoltage Lockout Operation**

### Thermal Shutdown (TSD)

The TB7107FN provides thermal shutdown. When the junction temperature continues to rise and reaches TSD (160°C typ.), the TB7107FN goes into thermal shutdown and shuts off the power supply. TSD has a hysteresis of about 15°C (typ.). The device is enabled again when the junction temperature has dropped by approximately 15°C from the TSD trip point. The device resumes the power supply when the soft-start circuit is activated upon recovery from TSD state.

Thermal shutdown is intended to protect the device against abnormal system conditions. It should be ensured that the TSD circuit will not be activated during normal operation of the system.

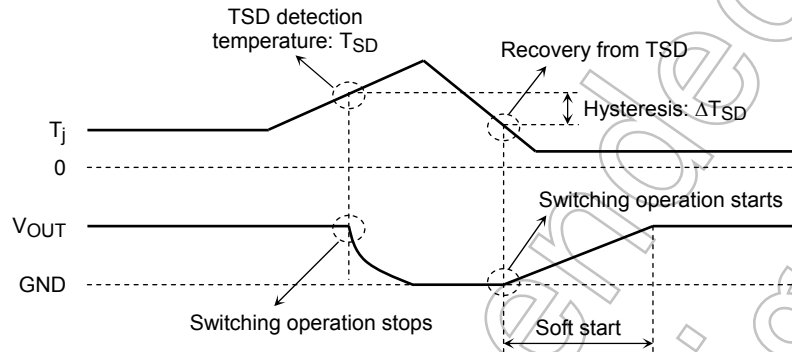


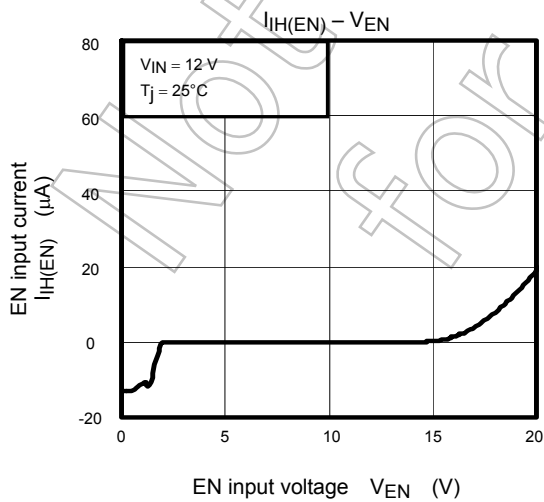
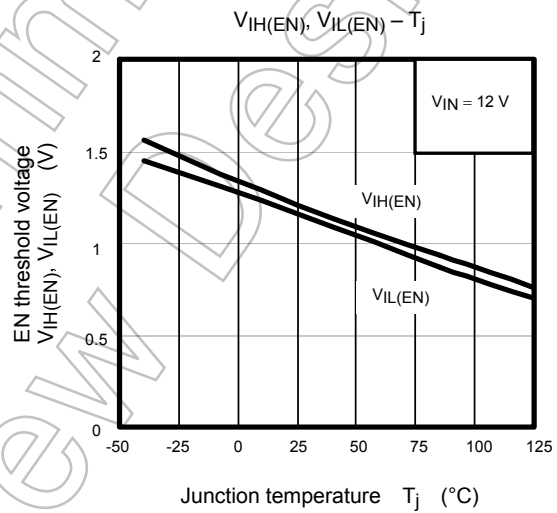
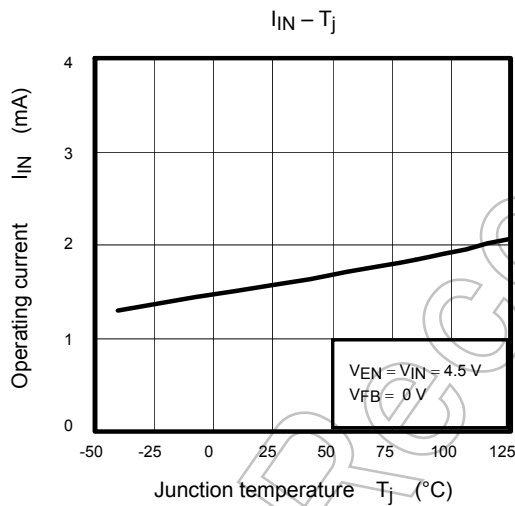
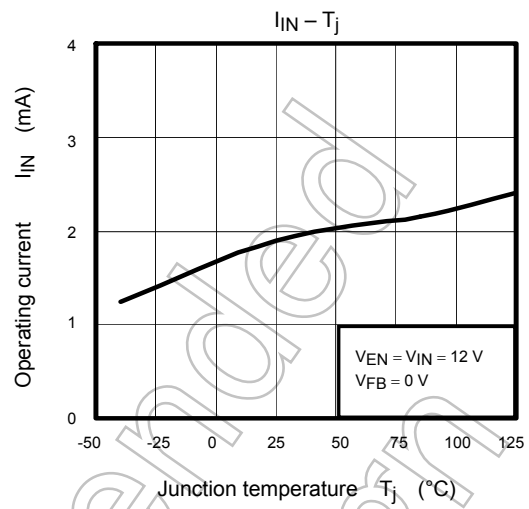
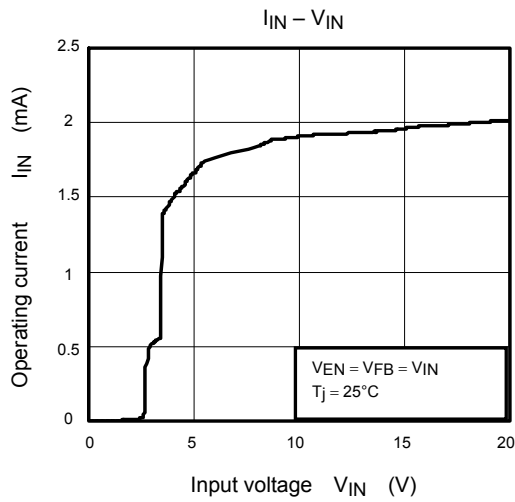
Figure 5 Thermal Shutdown Operation

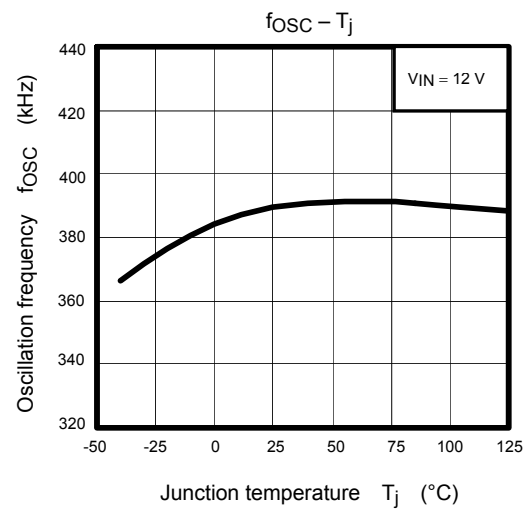
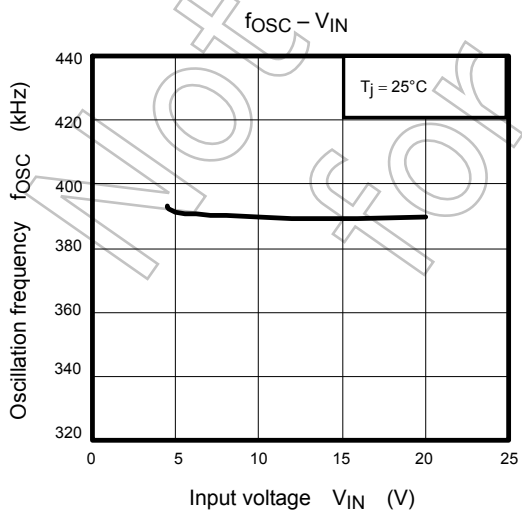
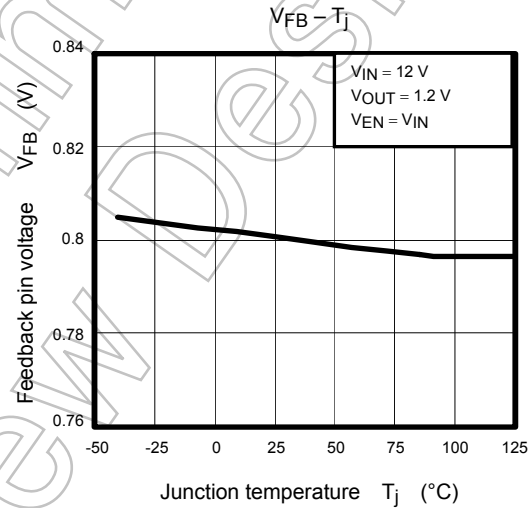
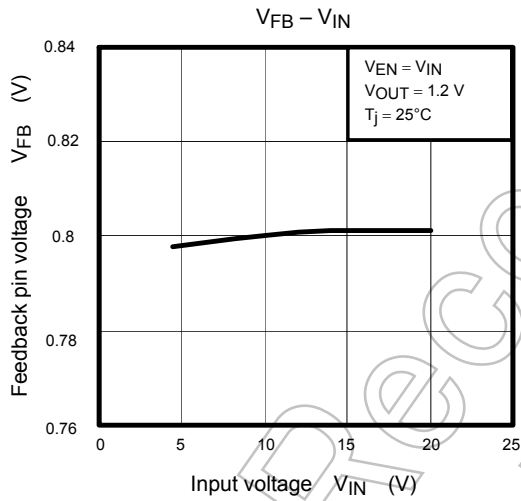
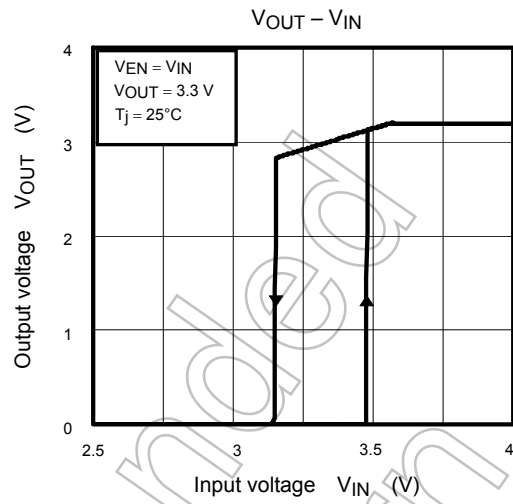
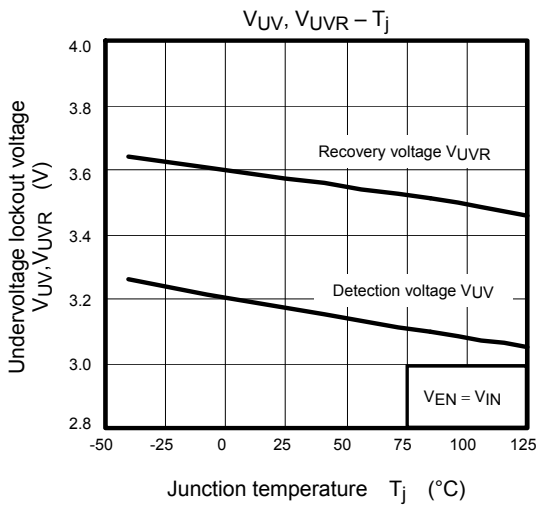
### Usage Precautions

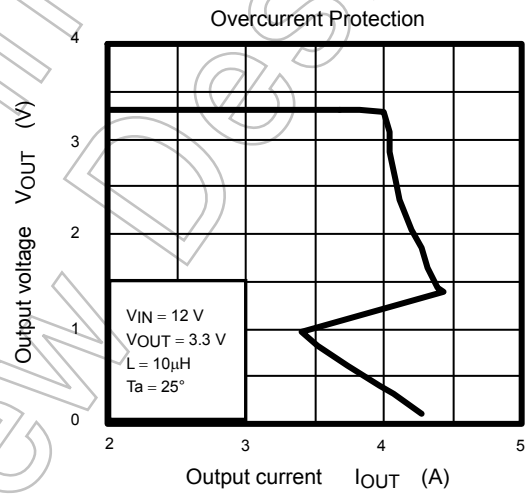
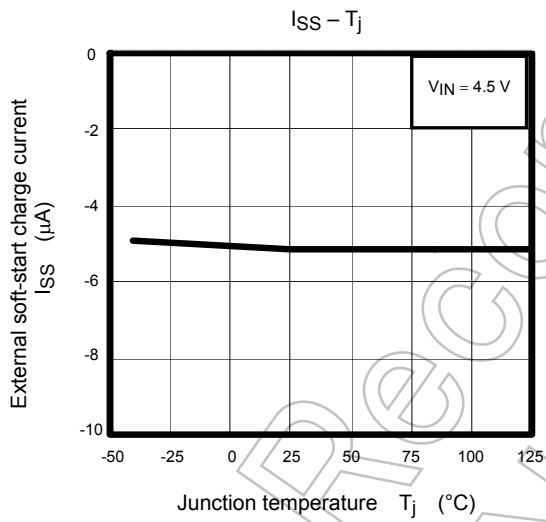
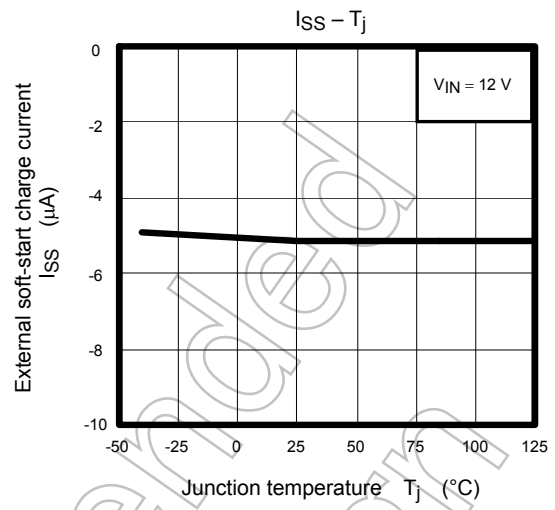
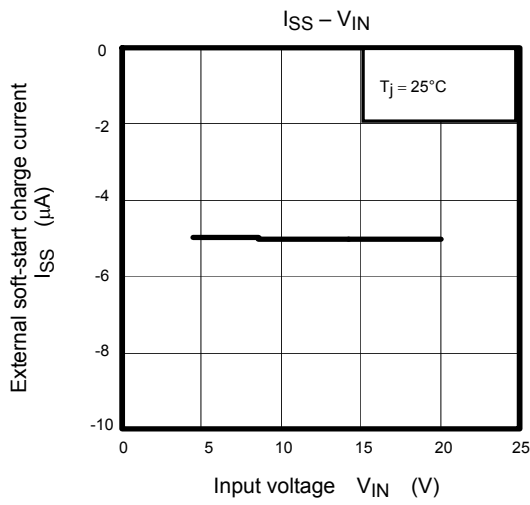
- The input voltage, output voltage, output current and temperature conditions should be considered when selecting capacitors, inductors and resistors. These components should be evaluated on an actual system prototype for best selection.
- External components such as capacitors, inductors and resistors should be placed as close to the TB7107FN as possible.
- CIN should be connected as close to the GND and VIN1 pins as possible. Operation might become unstable due to board layout.
- The minimum programmable output voltage is 0.8 V (typ.). If the difference between the input and output voltages is small, the output voltage might not be regulated accurately and fluctuate significantly.
- GND pin is connected with the back of IC chip and serves as the heat radiation pin. Secure the area of a GND pattern as large as possible for greater of heat radiation.
- The overcurrent protection circuits in the Product are designed to temporarily protect Product from minor overcurrent of brief duration. When the overcurrent protective function in the Product activates, immediately cease application of overcurrent to Product. Improper usage of Product, such as application of current to Product exceeding the absolute maximum ratings, could cause the overcurrent protection circuit not to operate properly and/or damage Product permanently even before the protection circuit starts to operate.
- The thermal shutdown circuits in the Product are designed to temporarily protect Product from minor overheating of brief duration. When the overheating protective function in the Product activates, immediately correct the overheating situation. Improper usage of Product, such as the application of heat to Product exceeding the absolute maximum ratings, could cause the overheating protection circuit not to operate properly and/or damage Product permanently even before the protection circuit starts to operate.

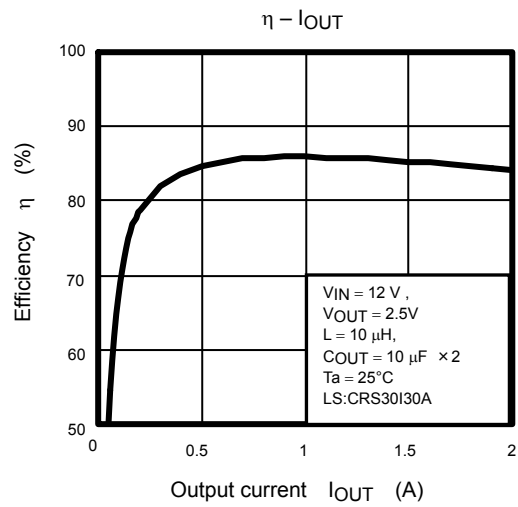
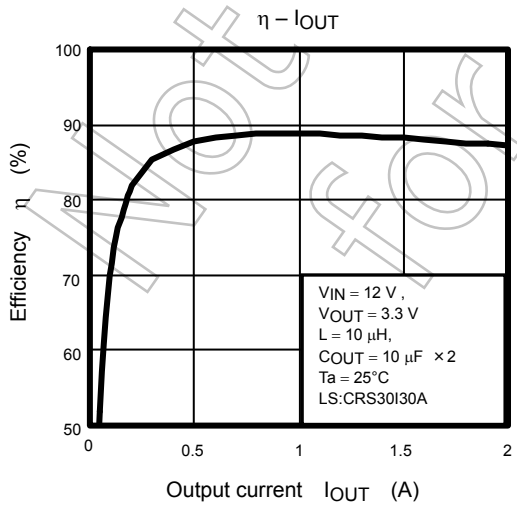
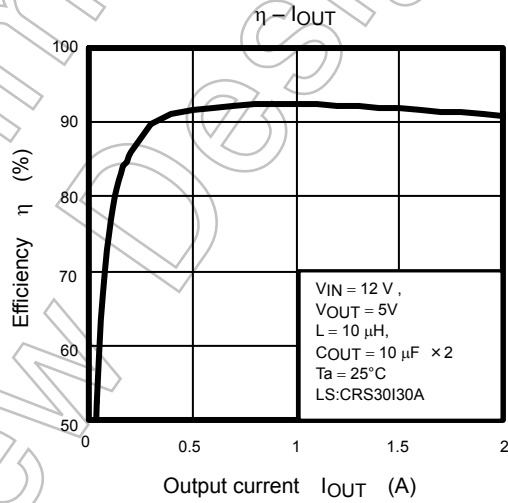
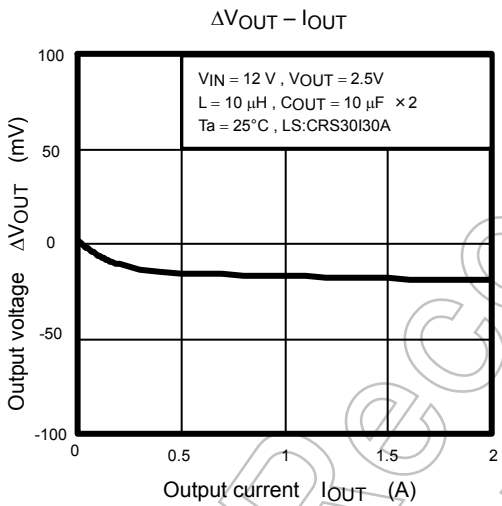
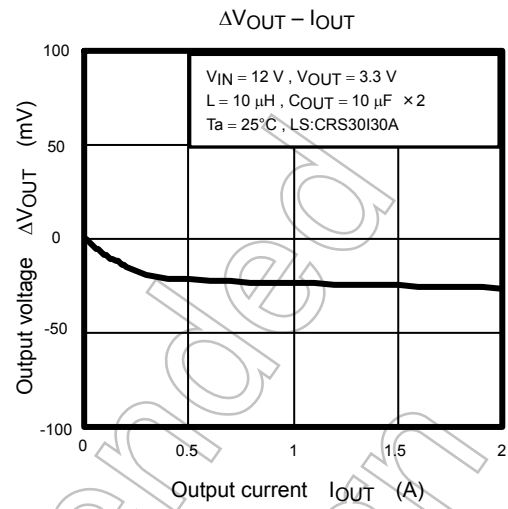
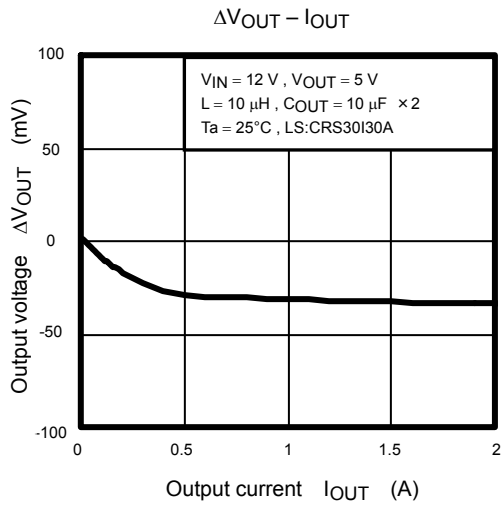


**Typical Performance Characteristics**

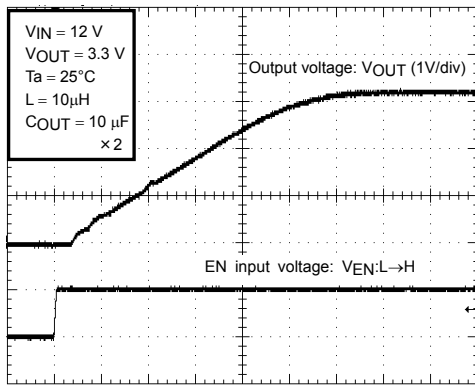






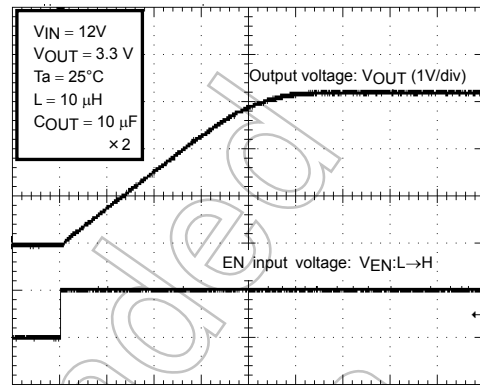


Startup Characteristics  
(Internal Soft-Start Time)



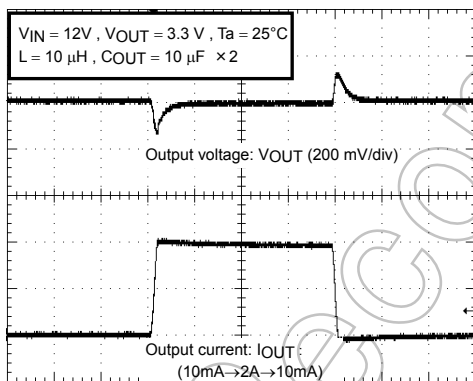
200  $\mu\text{s}/\text{div}$

Startup Characteristics  
( $C_{SS} = 0.1\ \mu\text{F}$ )



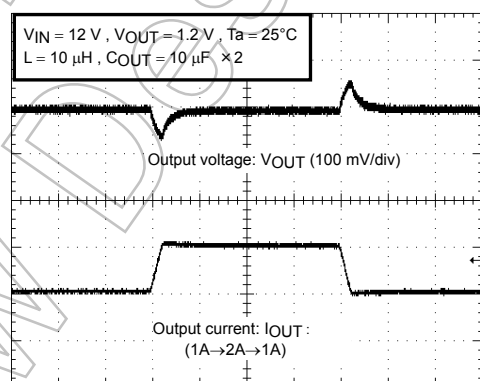
4 ms/div

Load Response Characteristics



200  $\mu\text{s}/\text{div}$

Load Response Characteristics

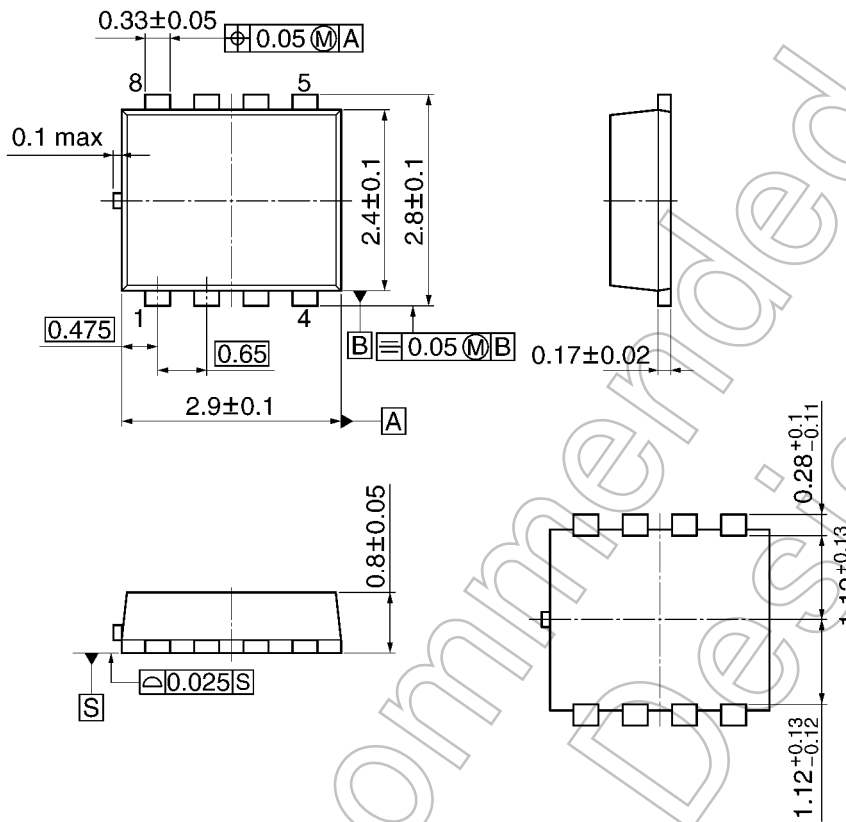


200  $\mu\text{s}/\text{div}$

## Package Dimensions

SON8-P-0303-0.65A

Unit: mm



Weight: 0.017 g (typ.)

Not Recommended for New Design

## RESTRICTIONS ON PRODUCT USE

- Toshiba Corporation, and its subsidiaries and affiliates (collectively "TOSHIBA"), reserve the right to make changes to the information in this document, and related hardware, software and systems (collectively "Product") without notice.
- This document and any information herein may not be reproduced without prior written permission from TOSHIBA. Even with TOSHIBA's written permission, reproduction is permissible only if reproduction is without alteration/omission.
- Though TOSHIBA works continually to improve Product's quality and reliability, Product can malfunction or fail. Customers are responsible for complying with safety standards and for providing adequate designs and safeguards for their hardware, software and systems which minimize risk and avoid situations in which a malfunction or failure of Product could cause loss of human life, bodily injury or damage to property, including data loss or corruption. Before customers use the Product, create designs including the Product, or incorporate the Product into their own applications, customers must also refer to and comply with (a) the latest versions of all relevant TOSHIBA information, including without limitation, this document, the specifications, the data sheets and application notes for Product and the precautions and conditions set forth in the "TOSHIBA Semiconductor Reliability Handbook" and (b) the instructions for the application with which the Product will be used with or for. Customers are solely responsible for all aspects of their own product design or applications, including but not limited to (a) determining the appropriateness of the use of this Product in such design or applications; (b) evaluating and determining the applicability of any information contained in this document, or in charts, diagrams, programs, algorithms, sample application circuits, or any other referenced documents; and (c) validating all operating parameters for such designs and applications. **TOSHIBA ASSUMES NO LIABILITY FOR CUSTOMERS' PRODUCT DESIGN OR APPLICATIONS.**
- **PRODUCT IS NEITHER INTENDED NOR WARRANTED FOR USE IN EQUIPMENTS OR SYSTEMS THAT REQUIRE EXTRAORDINARILY HIGH LEVELS OF QUALITY AND/OR RELIABILITY, AND/OR A MALFUNCTION OR FAILURE OF WHICH MAY CAUSE LOSS OF HUMAN LIFE, BODILY INJURY, SERIOUS PROPERTY DAMAGE AND/OR SERIOUS PUBLIC IMPACT ("UNINTENDED USE").** Except for specific applications as expressly stated in this document, Unintended Use includes, without limitation, equipment used in nuclear facilities, equipment used in the aerospace industry, medical equipment, equipment used for automobiles, trains, ships and other transportation, traffic signaling equipment, equipment used to control combustions or explosions, safety devices, elevators and escalators, devices related to electric power, and equipment used in finance-related fields. **IF YOU USE PRODUCT FOR UNINTENDED USE, TOSHIBA ASSUMES NO LIABILITY FOR PRODUCT.** For details, please contact your TOSHIBA sales representative.
- Do not disassemble, analyze, reverse-engineer, alter, modify, translate or copy Product, whether in whole or in part.
- Product shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable laws or regulations.
- The information contained herein is presented only as guidance for Product use. No responsibility is assumed by TOSHIBA for any infringement of patents or any other intellectual property rights of third parties that may result from the use of Product. No license to any intellectual property right is granted by this document, whether express or implied, by estoppel or otherwise.
- **ABSENT A WRITTEN SIGNED AGREEMENT, EXCEPT AS PROVIDED IN THE RELEVANT TERMS AND CONDITIONS OF SALE FOR PRODUCT, AND TO THE MAXIMUM EXTENT ALLOWABLE BY LAW, TOSHIBA (1) ASSUMES NO LIABILITY WHATSOEVER, INCLUDING WITHOUT LIMITATION, INDIRECT, CONSEQUENTIAL, SPECIAL, OR INCIDENTAL DAMAGES OR LOSS, INCLUDING WITHOUT LIMITATION, LOSS OF PROFITS, LOSS OF OPPORTUNITIES, BUSINESS INTERRUPTION AND LOSS OF DATA, AND (2) DISCLAIMS ANY AND ALL EXPRESS OR IMPLIED WARRANTIES AND CONDITIONS RELATED TO SALE, USE OF PRODUCT, OR INFORMATION, INCLUDING WARRANTIES OR CONDITIONS OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, ACCURACY OF INFORMATION, OR NONINFRINGEMENT.**
- Do not use or otherwise make available Product or related software or technology for any military purposes, including without limitation, for the design, development, use, stockpiling or manufacturing of nuclear, chemical, or biological weapons or missile technology products (mass destruction weapons). Product and related software and technology may be controlled under the applicable export laws and regulations including, without limitation, the Japanese Foreign Exchange and Foreign Trade Law and the U.S. Export Administration Regulations. Export and re-export of Product or related software or technology are strictly prohibited except in compliance with all applicable export laws and regulations.
- Please contact your TOSHIBA sales representative for details as to environmental matters such as the RoHS compatibility of Product. Please use Product in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. **TOSHIBA ASSUMES NO LIABILITY FOR DAMAGES OR LOSSES OCCURRING AS A RESULT OF NONCOMPLIANCE WITH APPLICABLE LAWS AND REGULATIONS.**