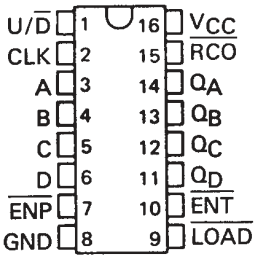
SYNCHRONOUS 4-BIT UP/DOWN BINARY COUNTERS

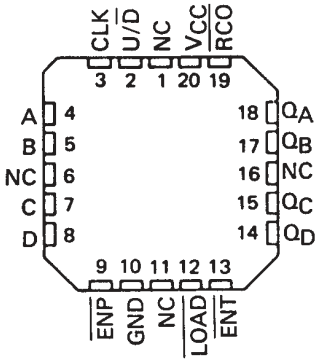
SDLS134 – OCTOBER 1976 – REVISED MARCH 1988

- **Programmable Look-Ahead Up/Down Binary Counters**
- **Fully Synchronous Operation for Counting and Programming**
- **Internal Look-Ahead for Fast Counting**
- **Carry Output for n-Bit Cascading**
- **Fully Independent Clock Circuit**

SN54LS169B, SN54S169 . . . J OR W PACKAGE
SN74LS169B, SN74S169 . . . D OR N PACKAGE
(TOP VIEW)



SN54LS169B, SN54S169 . . . FK PACKAGE
(TOP VIEW)



NC-No internal connection

description

These synchronous presettable counters feature an internal carry look-ahead for cascading in high speed counting applications. The 'LS169B and 'S169 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation helps eliminate the output counting spikes that are normally associated with asynchronous (ripple-clock) counters. A buffered clock input triggers the four master-slave flip-flops on the rising (positive-going) edge of the clock waveform.

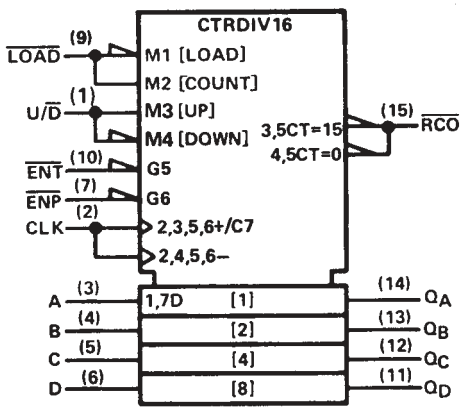
These counters are fully programmable; that is the outputs may each be preset to either level. The load input circuitry allows loading with the carry-enable output of cascaded counters. As loading is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the data inputs after the next clock pulse.

TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY		TYPICAL POWER DISSIPATION
	COUNTING UP	COUNTING DOWN	
'LS169B	35MHz	35MHz	100mW
'S169	70MHz	55MHz	500mW

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a carry output. Both count enable inputs ($\overline{ENP}$, $\overline{ENT}$) must be low to count. The direction of the count is determined by the level of the up/down input. When the input is high, the counter counts up; when low, it counts down. Input $\overline{ENT}$ is fed forward to enable the carry output. The carry output thus enabled will produce a low-level output pulse with a duration approximately equal to the high portion of the Q_A output when counting up and approximately equal to the low portion of the Q_A output when counting down. This low-level overflow carry pulse can be used to enable successive cascaded stages. Transitions at the $\overline{ENP}$ or $\overline{ENT}$ inputs are allowed regardless of the level of the clock input. All inputs are diode-clamped to minimize transmission-line effects, thereby simplifying system design.

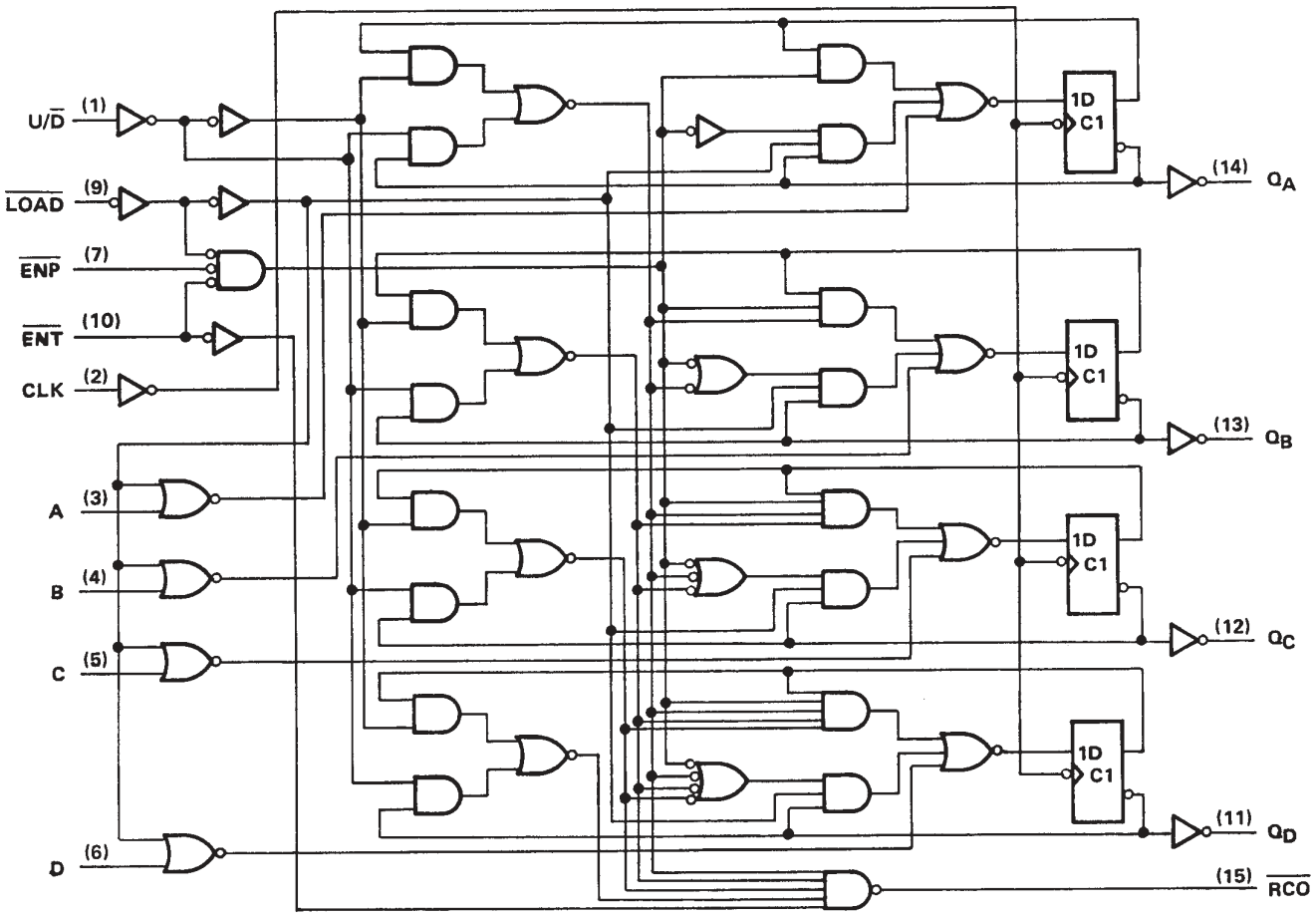
These counters feature a fully independent clock circuit. Changes at control inputs ($\overline{ENP}$, $\overline{ENT}$, $\overline{LOAD}$, $U/\overline{D}$) that will modify the operating mode have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

logic symbol†



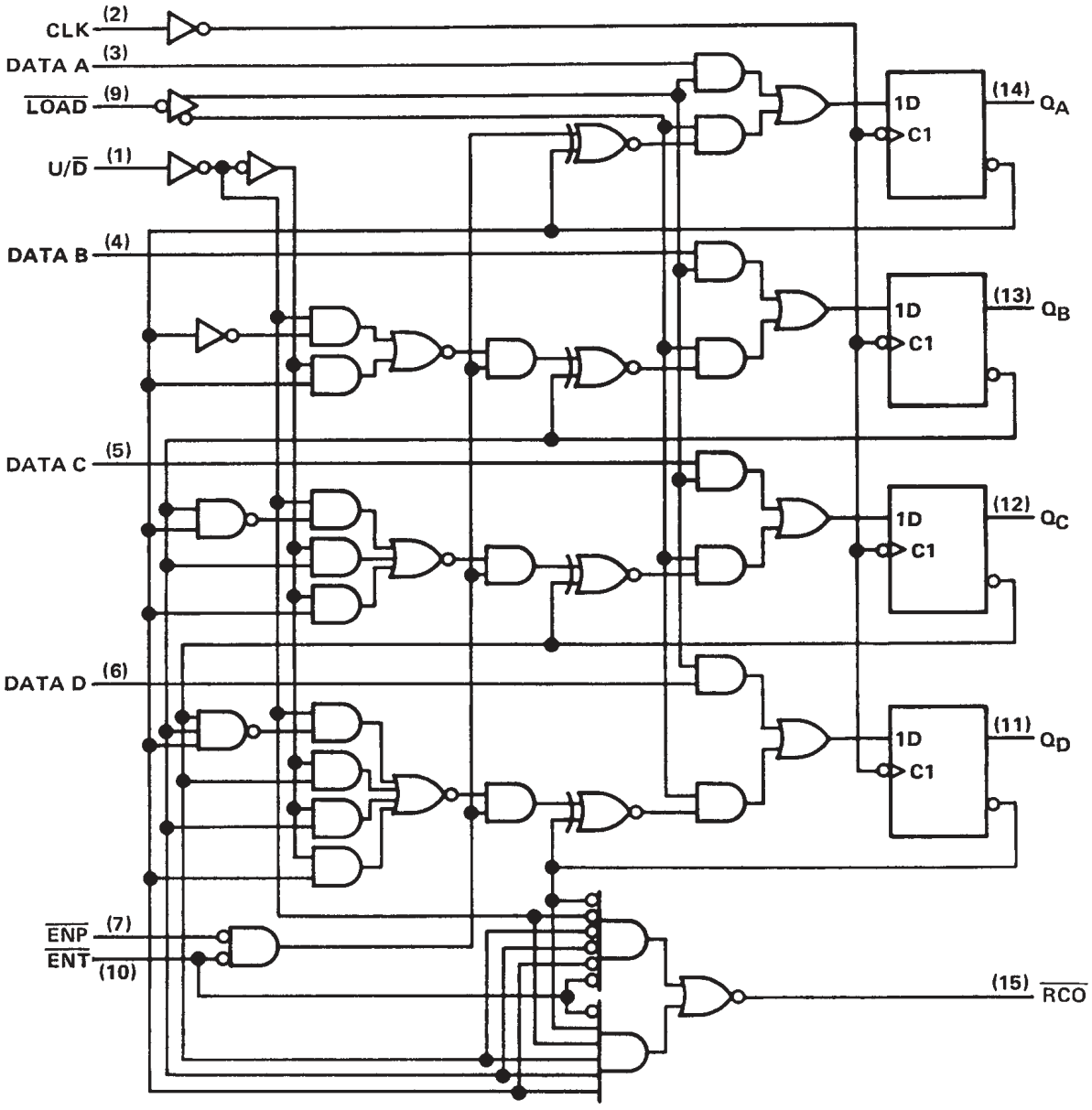
†This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, N, and W packages.

logic diagram (positive logic)



Pin numbers shown are for D, J, N, and W packages.

logic diagram (positive logic)

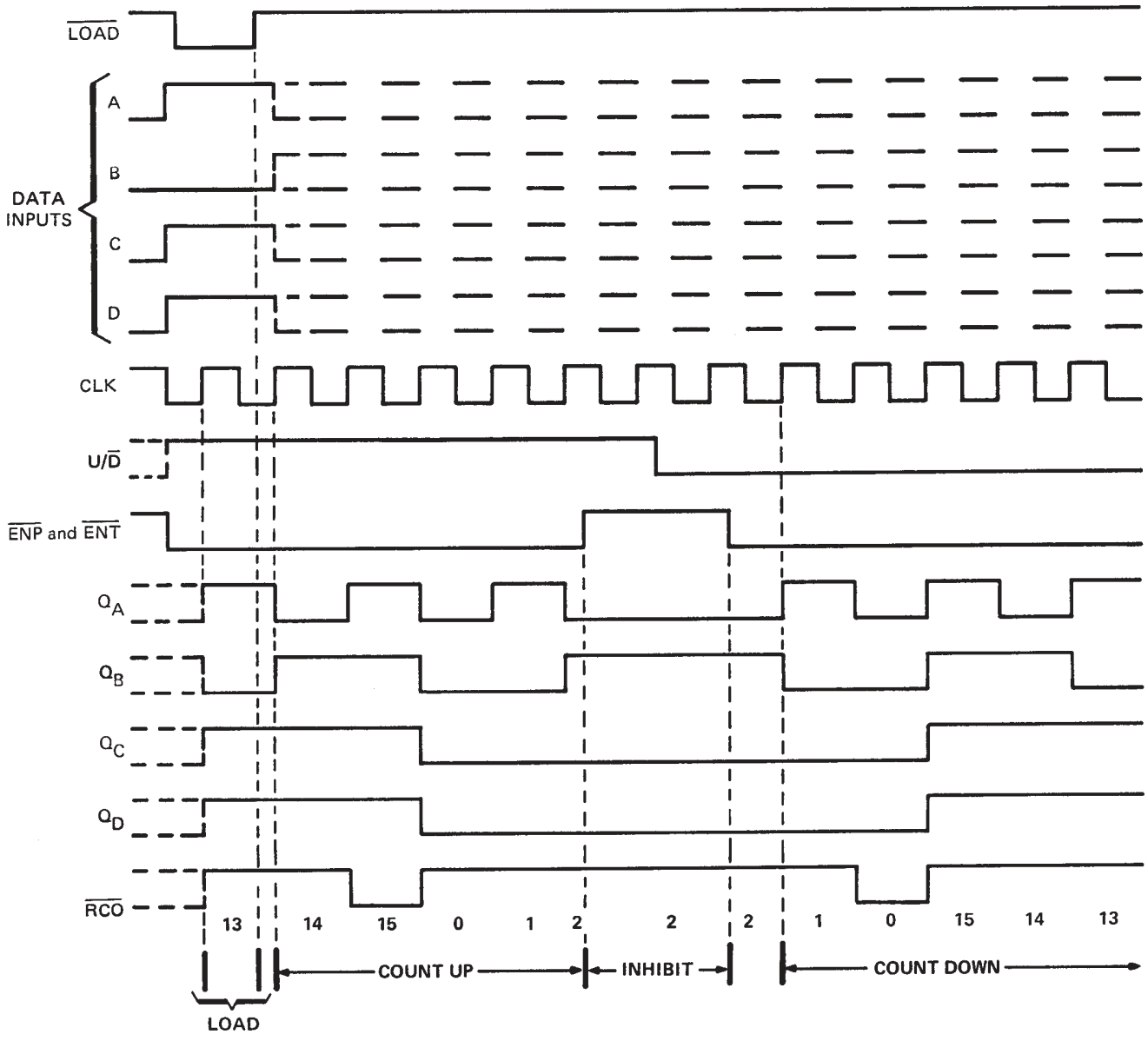


Pin numbers shown are for D, J, N, and W packages.

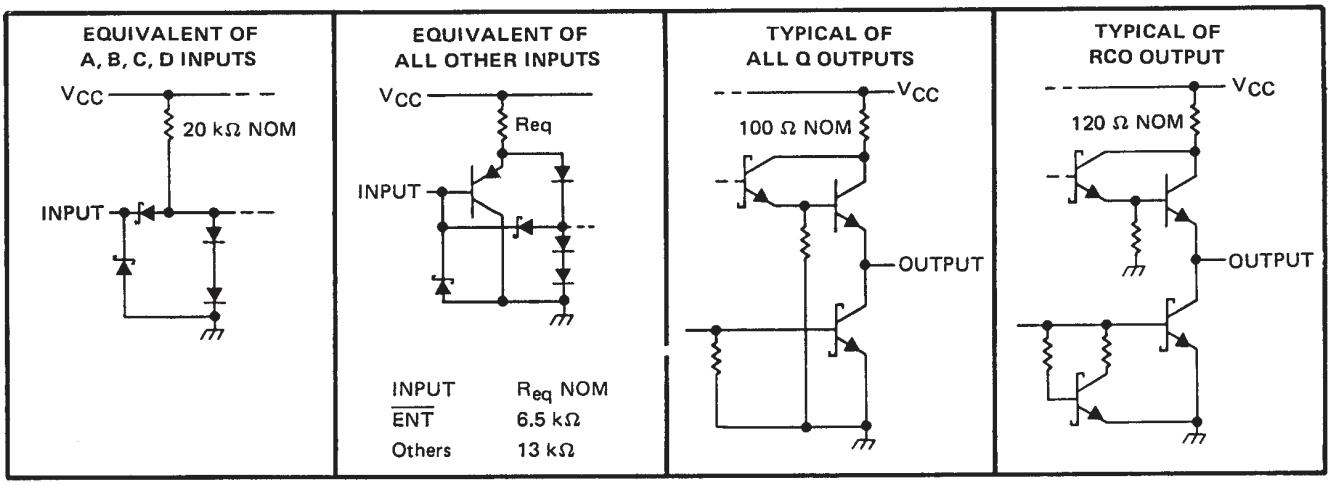
typical load, count, and inhibit sequences

Illustrated below is the following sequence:

1. Load (preset) to binary thirteen.
2. Count up to fourteen, fifteen (maximum), zero, one, and two.
3. Inhibit
4. Count down to one, zero (minimum), fifteen, fourteen, and thirteen



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54LS169B . . . . . −55°C to 125°C
SN74LS169B . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

			SN54LS169B			SN74LS169B			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level-input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
I_{OH}	High-level output current	$\overline{RCO}$			−0.4			−0.4	mA
		Any Q			−1.2			−1.2	mA
I_{OL}	Low-level output current	$\overline{RCO}$			4			8	mA
		Any Q			12			24	mA
f_{clock}	Clock frequency		0		20	0		20	MHz
$t_{w(clock)}$	Width of clock pulse (high or low) (see Figure 1)		25			25			ns
t_{su}	Setup time, (see Figure 1)	Data inputs A, B, C, D	30			30			ns
		$\overline{ENP}$ or $\overline{ENT}$	30			30			
		$\overline{Load}$	35			35			
		$U/\overline{D}$	35			35			
t_h	Hold time at any input with respect to clock (see Figure 1)		0			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†			SN54LS169B			SN74LS169B			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN, I_I = – 18 mA					– 1.5			– 1.5	V
V_{OH}	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = MAX	$\overline{RCO}$	I_{OH} = – 0.4 mA	2.5	3.4		2.7	3.4		V
		Any Q	I_{OH} = – 1.2 mA	2.4	3.2		2.4	3.2		
V_{OL}	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = MAX	$\overline{RCO}$	I_{OH} = 4 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 8 mA					0.35	0.5	
		Any Q	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	
			I_{OL} = 24 mA					0.35	0.5	
I_I	V_{CC} = MAX, V_I = 7 V					0.1			0.1	mA
I_{IH}	V_{CC} = MAX, V_I = 2.7 V					20			20	μA
I_{IL}	V_{CC} = MAX, V_I = 0.4 V	U/$\overline{D}$, $\overline{LOAD}$, $\overline{ENP}$, CLK				– 0.2			– 0.2	mA
		All other inputs				– 0.4			– 0.4	
I_{OS}§	V_{CC} = MAX, V_O = 0 V	$\overline{RCO}$		– 20		– 100	– 20		– 100	mA
		Any Q		– 30		– 130	– 30		– 130	
I_{CC}	V_{CC} = MAX, See Note 2				28	45		28	45	mA

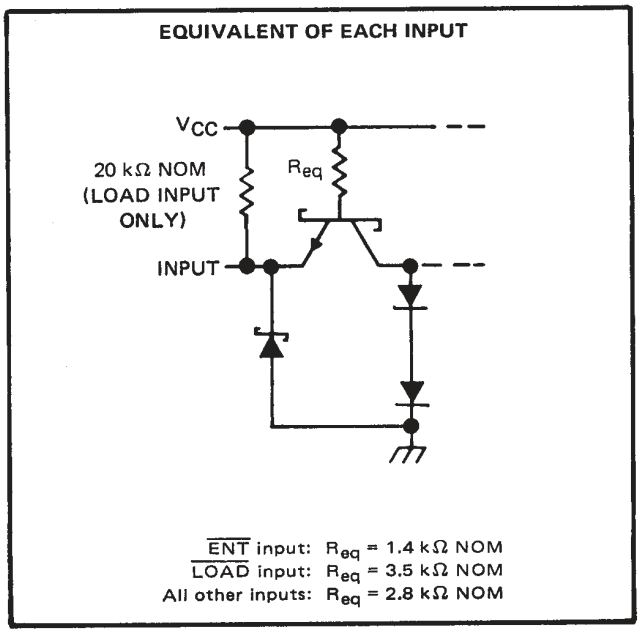
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
NOTE 2: I_{CC} is measured after applying a momentary 4.5 V, then ground, to the clock input with all other inputs grounded and the outputs open.

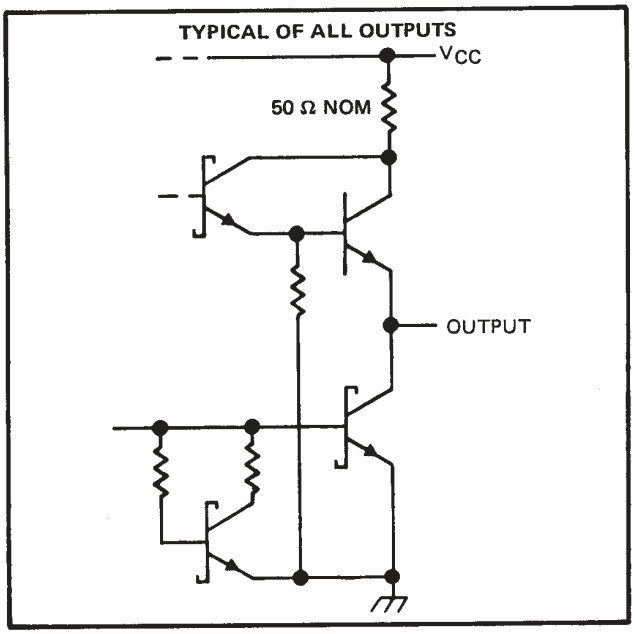
switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS169B			UNIT
				MIN	TYP	MAX	
f_{max}				20	35		MHz
t_{PLH}	CLK	$\overline{RCO}$	R_L = 2 kΩ, C_L = 15 pF		26	40	ns
t_{PHL}					17	25	
t_{PLH}	$\overline{ENT}$	$\overline{RCO}$			15	25	ns
t_{PHL}					11	20	
t_{PLH}	U/$\overline{D}$	$\overline{RCO}$			23	35	ns
t_{PHL}					15	25	
t_{PLH}	CLK	Any Q	R_L = 667 Ω, C_L = 45 pF		16	25	ns
t_{PHL}					17	25	

¶ Propagation delay time from up/down to ripple carry must be measured with the counter at either a minimum or a maximum count. As the logic level of the up/down input is changed, the ripple carry output will follow. If the count is minimum (0), the ripple carry output transition will be in phase. If the count is maximum (15), the ripple carry output will be out of phase.
NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

schematics of inputs and outputs





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (See Note 4) . . . . . 7 V
Input voltage . . . . . 5.5 V
Interemitter voltage (see Note 5) . . . . . 5.5 V
Operating free-air temperature range: SN54S169 (see Note 6) . . . . . −55°C to 125°C
SN74S169 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54S169			SN74S169			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−1			−1	mA
Low-level output current, I_{OL}				20			20	mA
Clock frequency, f_{clock}		0		40	0		40	MHz
Width of clock pulse, $t_{w(clock)}$ (high or low) (see Figure 1)		10			10			ns
Setup time, t_{su} (see Figure 1)	Data inputs A, B, C, D	4			4			ns
	$\overline{ENP}$ or $\overline{ENT}$	14			14			
	Load	9			6			
	U/$\overline{D}$	20			20			
Hold time at any input with respect to clock, t_w (see Figure 1)		1			1			ns
Operating free-air temperature, T_A (see Note 6)		−55		125	0		70	°C

NOTES: 4. Voltage values, except interemitter voltage, are with respect to network ground terminal.
5. This is the voltage between two emitters of a multiple-emitter transistor. For these circuits, this rating applies between the count enable inputs $\overline{ENP}$ and $\overline{ENT}$.
6. A SN54S169 in the W package operating at free-air temperatures above 91°C requires a heat sink that provides a thermal resistance from case to free-air, $R_{\theta CA}$, of not more than 26°C/W.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54S169			SN74S169			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage			2			2			V
V_{IL} Low-level input voltage					0.8			0.8	V
V_{IK} Input clamp voltage		V_{CC} = MIN, I_I = −18 mA			−1.2			−1.2	V
V_{OH} High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −1 mA	2.5	3.4		2.7	3.4		V
V_{OL} Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 20 mA			0.5			0.5	V
I_I Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH} High-level input current	$\overline{ENT}$	V_{CC} = MAX, V_I = 2.7 V			100			100	μA
	$\overline{Load}$		−10		−200	−10		−200	
	Other inputs				50			50	
I_{IL} Low-level input current	$\overline{ENT}$	V_{CC} = MAX, V_I = 0.5 V			−4			−4	mA
	Other inputs				−2			−2	
I_{OS} Short-circuit output current§		V_{CC} = MAX,	−40		−100	−40		−100	mA
I_{CC} Supply current		V_{CC} = MAX, See Note 2		100	160		100	160	mA

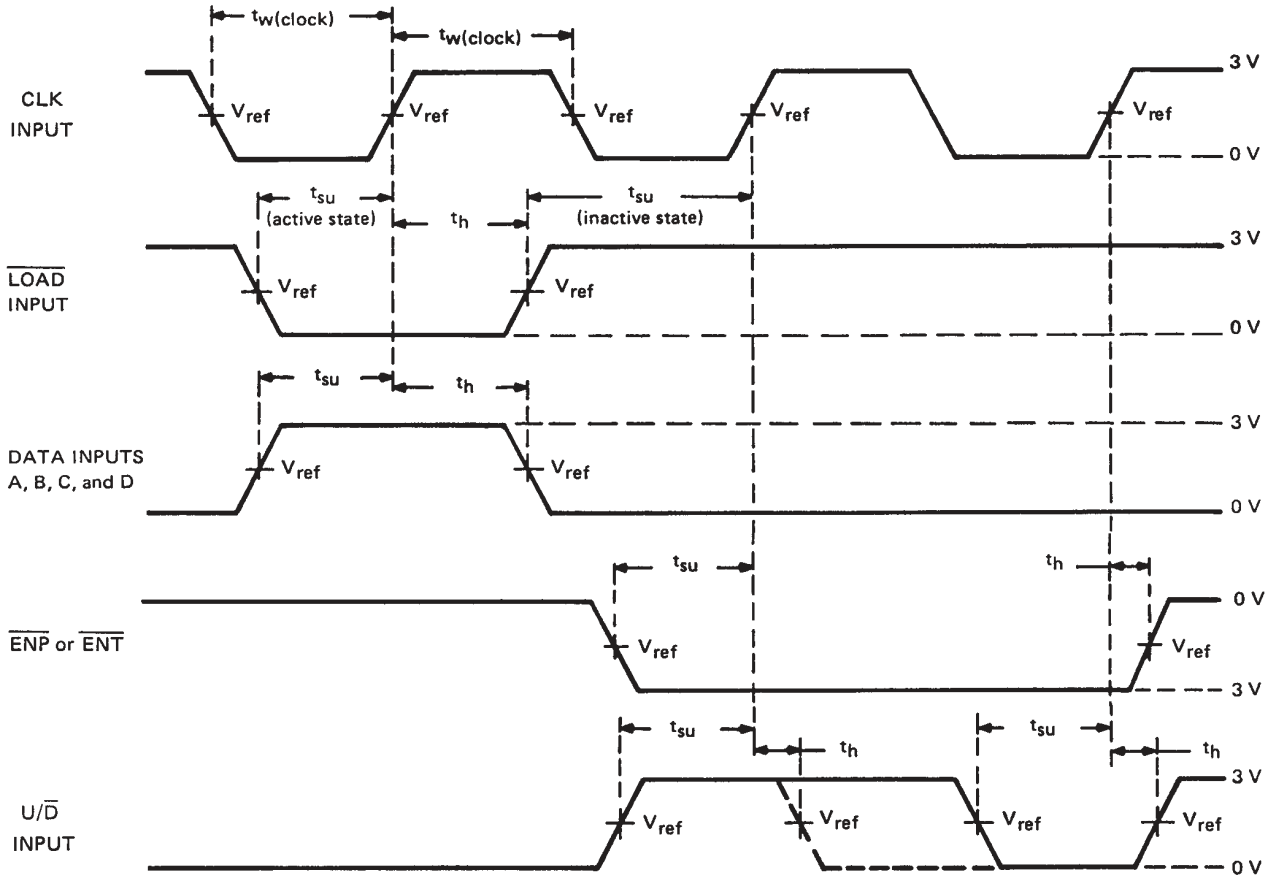
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
NOTE 2: I_{CC} is measured after applying a momentary 4.5 V, then ground, to the clock input with all other inputs grounded and the outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	U/$\overline{D}$ = HIGH			U/$\overline{D}$ = LOW			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}			C_L = 15 pF, R_L = 280 Ω, See Figures 2 and 3 and Note 3	40	70		40	55		MHz
t_{PLH}	CLK	$\overline{RCO}$			14	21		14	21	ns
t_{PHL}					20	28		20	28	
t_{PLH}	CLK	Any Q			8	15		8	15	ns
t_{PHL}					11	15		11	15	
t_{PLH}	$\overline{ENT}$	$\overline{RCO}$			7.5	11		6	12	ns
t_{PHL}					15	22		15	25	
t_{PLH}◇	U/$\overline{D}$	$\overline{RCO}$			9	15		8	15	ns
t_{PHL}◇					10	15		16	22	

¶ t_{max} = maximum clock frequency
t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output
Propagation delay time from up/down to ripple carry must be measured with the counter at either a minimum or a maximum count. As the logic level of the up/down input is changed, the ripple carry output will follow. If the count is minimum (0), the ripple carry output transition will be in phase. If the count is maximum (15 for 'S169), the ripple carry output will be out of phase.
NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

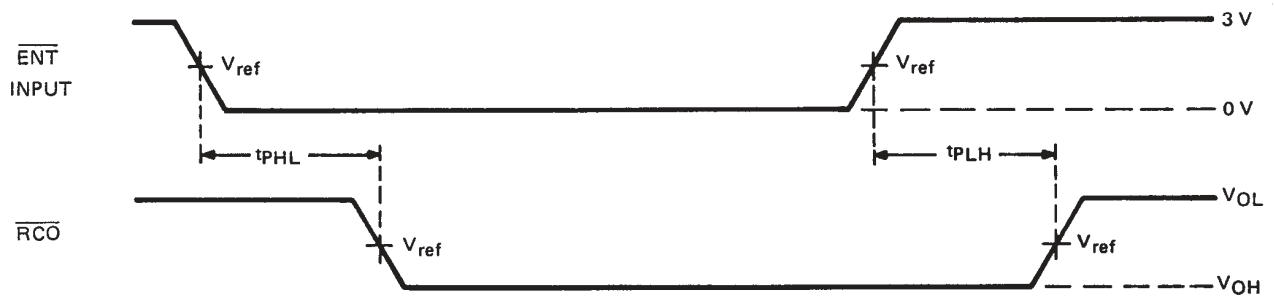
PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS

NOTES: A. The input pulses are supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, Z_{out} ≈ 50 Ω; for 'LS169B, t_r ≤ 15 ns; t_f ≤ 6 ns, and for 'S169, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
B. For 'LS169B, V_{ref} = 1.3 V; for 'S168 and 'S169, V_{ref} = 1.5 V.

FIGURE 1–PULSE WIDTHS, SETUP TIMES, HOLD TIMES

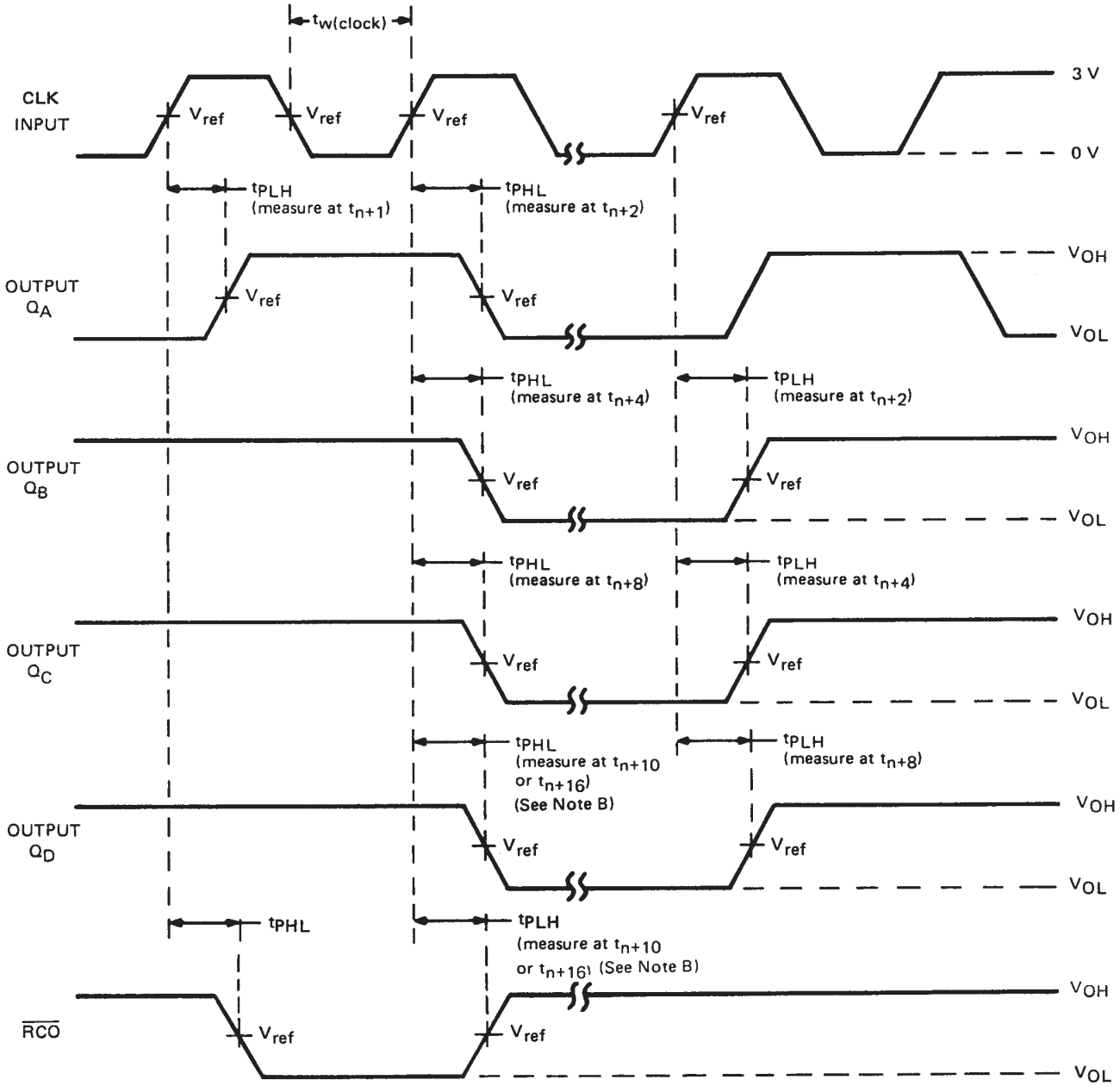


VOLTAGE WAVEFORMS

NOTES: A. The input pulses are supplied by a generator having the following characteristics: PRR ≤ MHz, duty cycle ≤ 50%, Z_{out} ≈ 50 Ω; for 'LS169B, t_r ≤ 15 ns, t_f ≤ 5 ns; and for 'S169, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
B. t_{PLH} and t_{PHL} from enable T input to ripple carry output assume that the counter is at the maximum count, all Q outputs high.
C. For 'LS169B, V_{ref} = 1.3 V; for 'S169, V_{ref} = 1.5 V.
D. Propagation delay time from up/down to ripple carry must be measured with the counter at either a minimum or a maximum count. As the logic level of the up/down input is changed, the ripple carry output will follow. If the count is minimum (0) the ripple carry output transition will be in phase. If the count is maximum (15), the ripple carry output will be out of phase.

FIGURE 2–PROPAGATION DELAY TIMES TO CARRY OUTPUT

PARAMETER MEASUREMENT INFORMATION



UP-COUNT VOLTAGE WAVEFORMS

NOTES: A. The input pulses are supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤50%, $Z_{out} \approx 50\ \Omega$; for 'LS169B, $t_r \leq 15$ ns; $t_f \leq 6$ ns, and 'S169, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns. Vary PRR to measure f_{max}.
B. Outputs Q_D and carry are tested at t_{n+16}, where t_n is the bit-time when all outputs are low.
C. For 'LS169B, $V_{ref} = 1.3$ V; for 'S169, $V_{ref} = 1.5$ V.

FIGURE 3–PROPAGATION DELAY TIMES FROM CLOCK

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
80018022A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	80018022A SNJ54LS 169BFK	Samples
8001802EA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	8001802EA SNJ54LS169BJ	Samples
8001802EA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	8001802EA SNJ54LS169BJ	Samples
8001802FA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	8001802FA SNJ54LS169BW	Samples
8001802FA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	8001802FA SNJ54LS169BW	Samples
SN54LS169BJ	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54LS169BJ	Samples
SN54LS169BJ	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54LS169BJ	Samples
SN54S169J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54S169J	Samples
SN54S169J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54S169J	Samples
SN74LS169BD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS169B	Samples
SN74LS169BD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS169B	Samples
SN74LS169BN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS169BN	Samples
SN74LS169BN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS169BN	Samples
SN74LS169BNE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS169BN	Samples
SN74LS169BNE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS169BN	Samples
SN74S169J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI	0 to 70		
SN74S169J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI	0 to 70		
SN74S169N	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI	0 to 70		
SN74S169N	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI	0 to 70		

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74S169N3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI	0 to 70		
SN74S169N3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI	0 to 70		
SNJ54LS169BFK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	80018022A SNJ54LS 169BFK	Samples
SNJ54LS169BFK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	80018022A SNJ54LS 169BFK	Samples
SNJ54LS169BJ	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	8001802EA SNJ54LS169BJ	Samples
SNJ54LS169BJ	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	8001802EA SNJ54LS169BJ	Samples
SNJ54LS169BW	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	8001802FA SNJ54LS169BW	Samples
SNJ54LS169BW	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	8001802FA SNJ54LS169BW	Samples
SNJ54S169J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ54S169J	Samples
SNJ54S169J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ54S169J	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF SN54LS169B, SN54S169, SN74LS169B, SN74S169 :

- Catalog: SN74LS169B, SN74S169
- Military: SN54LS169B, SN54S169

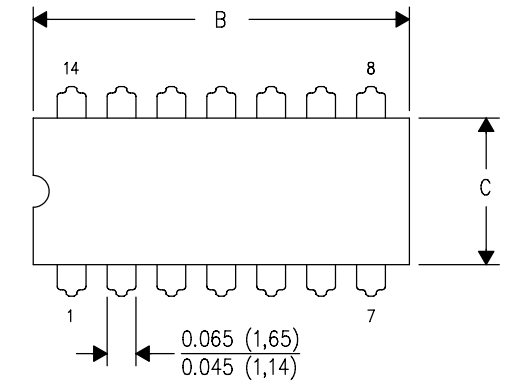
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

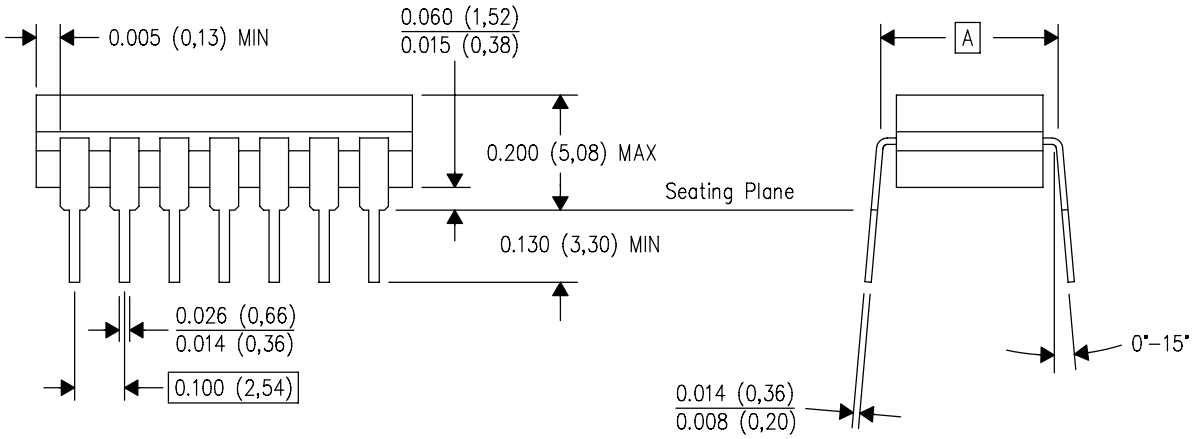
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



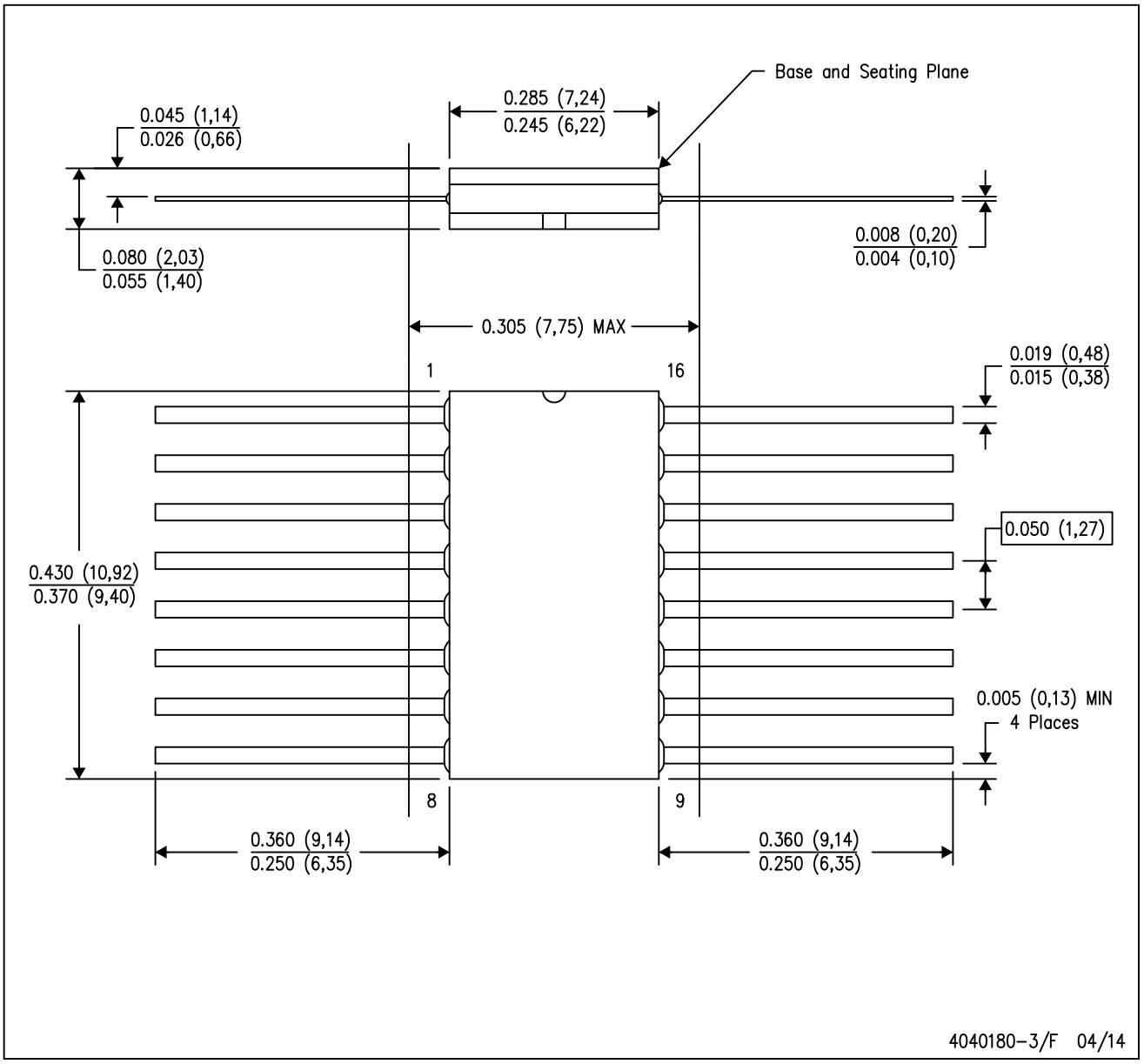
DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

W (R–GDFP–F16) CERAMIC DUAL FLATPACK

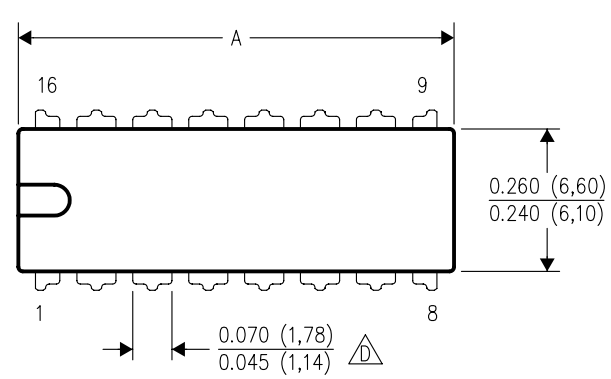


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP2–F16

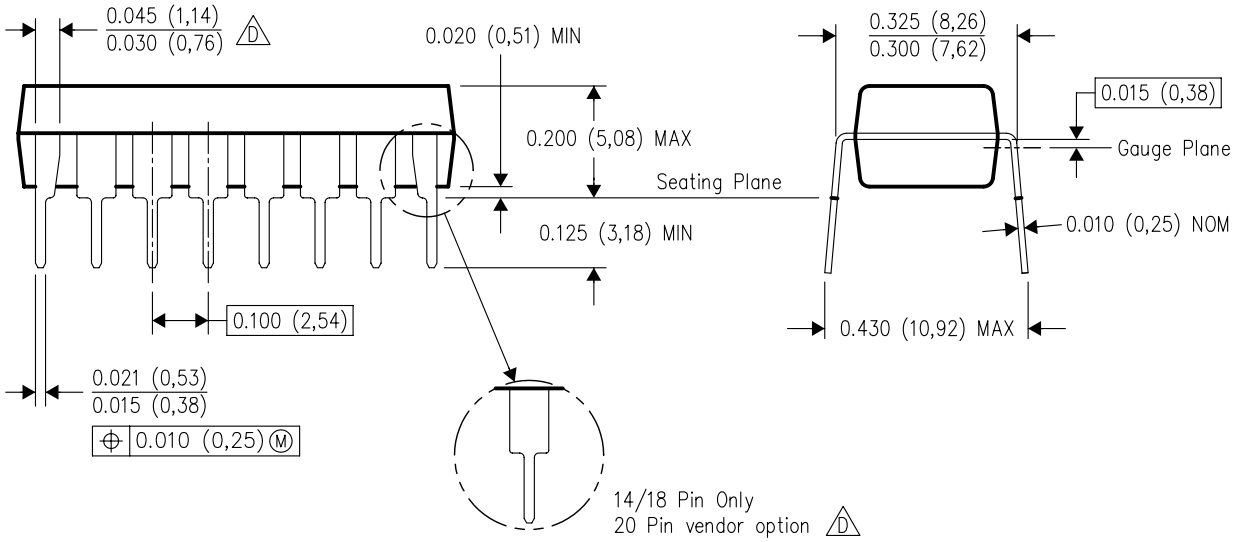
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD

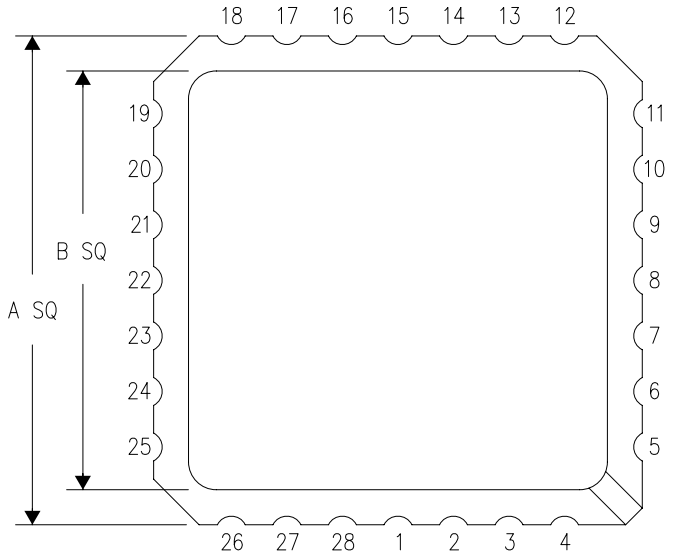


4040049/E 12/2002

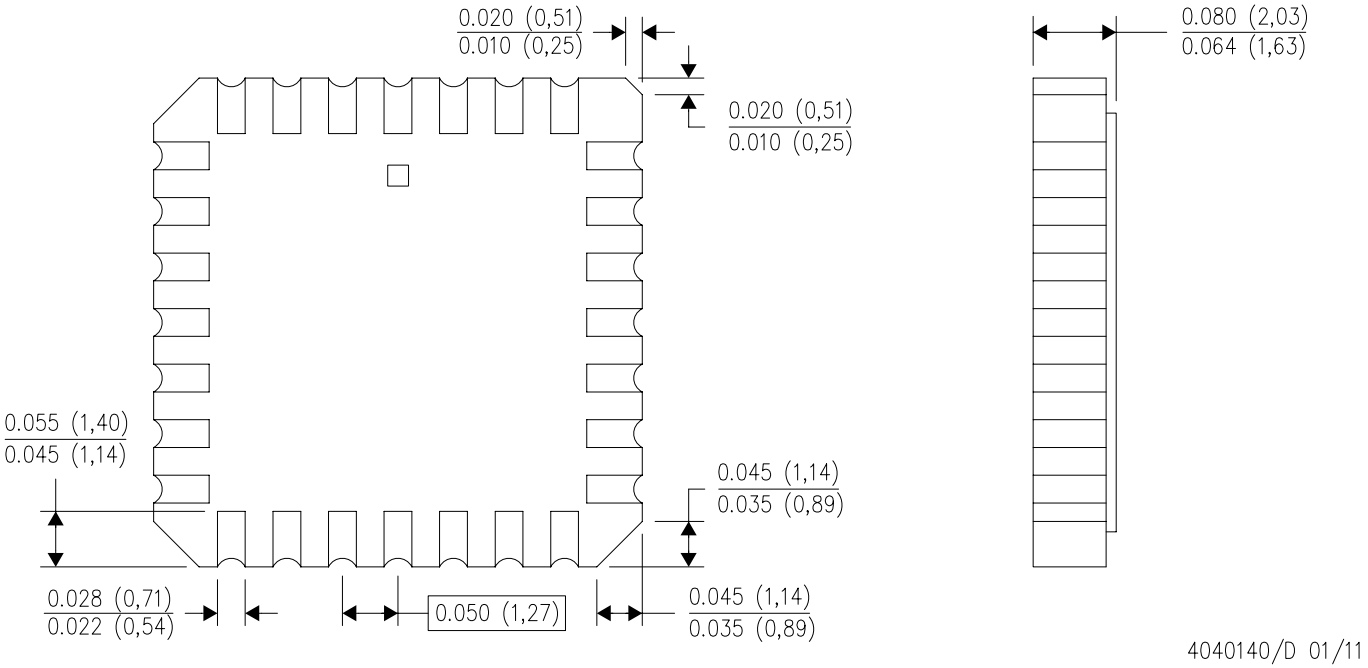
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

FK (S–CQCC–N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



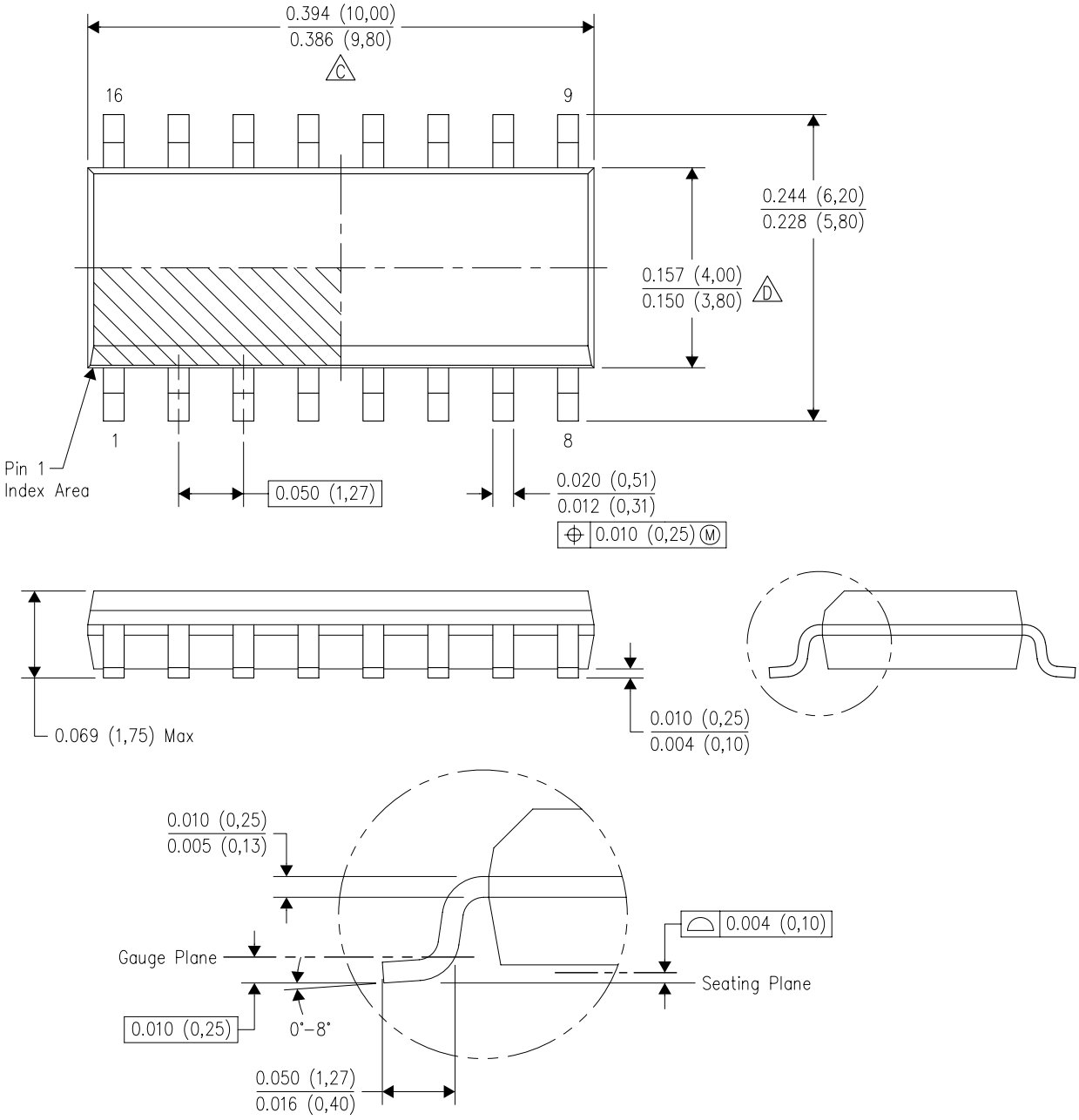
NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

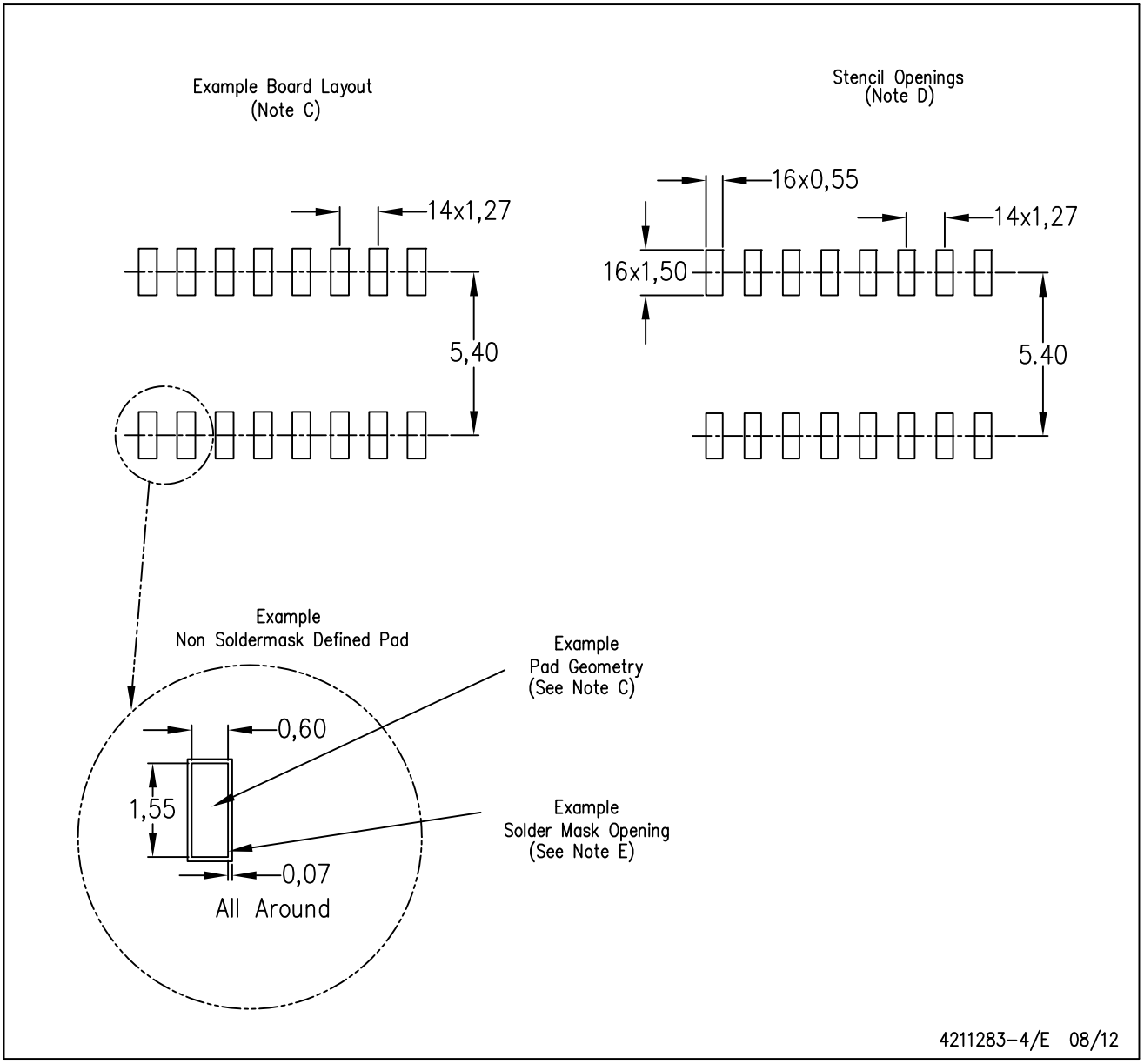
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. Falls within JEDEC MS–004

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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