EVL3435-L-00A

19A, 22V, Fixed-Frequency, High-Efficiency, Fully Integrated, Synchronous Boost Converter Evaluation Board

DESCRIPTION

The EVL3435-L-00A is an evaluation board designed to demonstrate the capabilities of the MP3435, a 600kHz, fixed-frequency, high-efficiency, fully integrated synchronous boost converter with 22V of output voltage across a wide input supply range (3V to 20V). The MP3435 features input disconnect to provide additional protection during an output short or shutdown by isolating the input from the output. For battery-operated applications, the input disconnect also prevents battery depletion.

The MP3435 features a 10mΩ low-side MOSFET (LS-FET) and a 15mΩ synchronous high-side MOSFET (HS-FET) for high efficiency and low cost. The MP3435's fault protections include under-voltage lockout (UVLO), current limiting, and thermal shutdown (TSD).

The MP3435 is available in a low-profile QFN-20 (3mmx4mm) package.

ELECTRICAL SPECIFICATIONS

Parameter	Symbol	Value	Units
Input voltage	V_{IN}	3 to 10	V
Output voltage	V_{OUT}	12	V
Output current	I_{OUT}	0 to OCP (1)	A

Note:

1) The maximum output current depends on the current limit, permitted temperature rising, and input voltage.

FEATURES

- Wide 3V to 20V Operating Input Range
- Up to 22V Output Voltage
- Integrated 10mΩ LS-FET and 15mΩ Synchronous HS-FET
- 19A Internal Switch Current Limit or External Configurable Input Current Limit
- Input Disconnect and Output Short-Circuit Protection (SCP)
- External Soft Start (SS) and Compensation
- Configurable UVLO and Hysteresis
- <1μA Shutdown Current
- Thermal Shutdown (TSD) at 150°C
- Available in a QFN-20 (3mmx4mm) Package

MPL Optimized Performance with MPS Inductor MPL-AY1050 Series

APPLICATIONS

- Thunderbolt Interfaces
- Notebooks and Tablets
- Bluetooth Audio
- Power Banks
- Fuel Cells
- Point-of-Sale (POS) Systems
- Other Electronic Accessories

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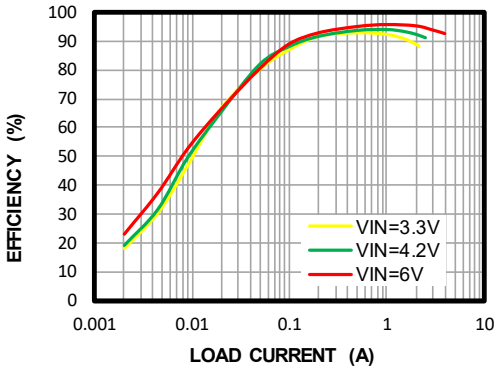
EVL3435-L-00A EVALUATION BOARD

LxWxH (6.4cmx6.4cmx0.6cm)

Board Number	MPS IC Number	MPS Inductor
EVL3435-L-00A	MP3435GL	MPL-AY1050-1R5

Efficiency

Input MOSFET, V_{OUT} = 12V



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QUICK START GUIDE

The output voltage (V_{OUT}) of the evaluation board is 12V. The board layout accommodates most commonly used components.

1. Preset the power supply between 3V and 10V.
2. Turn off the power supply.
3. Connect the power supply terminals to:
   a. Positive (+): VIN
   b. Negative (-): GND
4. Connect the load terminals to:
   a. Positive (+): VOUT
   b. Negative (-): GND
5. After making the connections, turn on the power supply.
6. Once the input voltage (V_{IN}) is applied, the MP3435 is enabled on the evaluation board.
7. V_{OUT} can be changed by modifying the R2 resistor's value. The new V_{OUT} can be calculated with Equation (1):

$$V_{OUT} = V_{FB} \times (1 + \frac{R1}{R2}) \quad (1)$$

   Where V_{FB} is 1.225V, and R1 is 300kΩ.
8. The default configuration of the evaluation board uses an external sense resistor. To use the internal sense resistor, follow steps 9 through 11 to modify the evaluation board.
9. Connect the GATE pin to GND via a 0Ω resistor (R7).
10. Set the external sense resistor ($R4_A$, $R4_B$, $R4_C$, and $R4_D$) to 0Ω.
11. Short the input MOSFET (Q1) drain to source.
12. After modifying the evaluation board, follow steps 1 through 5. The MP3435 should automatically use the internal sense resistor.

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EVALUATION BOARD SCHEMATIC

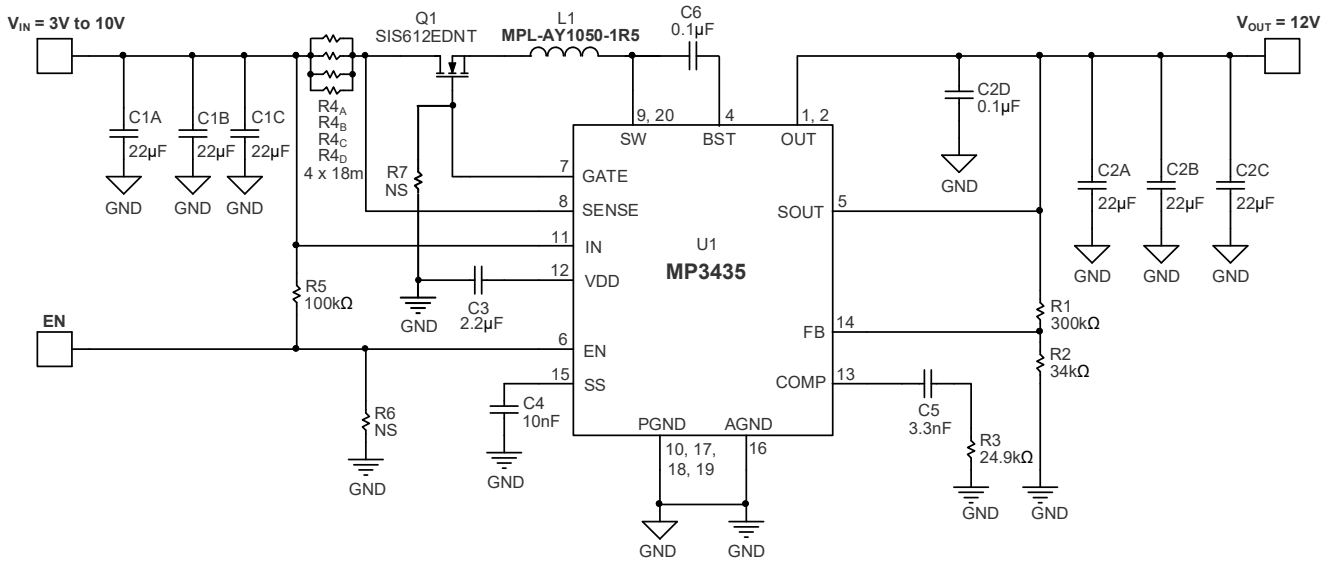

Figure 1: Evaluation Board Schematic

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EVL3435-L-00A BILL OF MATERIALS

Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer P/N
1	L1	1.5µH	3.4mΩ, 17A inductor	SMD (11mmx10mm)	MPS	MPL-AY1050-1R5
6	C1A, C1B, C1C, C2A, C2B, C2C	22µF	Ceramic capacitor, 25V, X5R	1210	Murata	GRM32R71E226KL
2	C2D, C6	0.1µF	Ceramic capacitor, 25V, X5R	0603	Murata	GRM188R71E104KA9
1	C3	2.2µF	Ceramic capacitor, 10V, X5R	0805	Murata	GRM21AR71A225KL
1	C4	10nF	Ceramic capacitor, 50V, X5R	0603	Murata	GRM188R71H103KL
1	C5	3.3nF	Ceramic capacitor, 50V, X5R	0603	Murata	GRM188R71H332KL
1	Q1	20V	20V, 3.2mΩ, 19A N-channel MOSFET	PowerPAK 1212-8	Vishay	SiS612EDNT-T1-GE3
1	R1	300kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-07300KL
1	R2	34kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-0734KL
1	R3	24.9kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-0724K9L
4	$R4_A$, $R4_B$, $R4_C$, $R4_D$	18mΩ	Low-resistance film resistor, 1%	0805	Yageo	PR0805FKF070R018L
1	R5	100kΩ	Film resistor, 1%	0603	Yageo	RC0603JR-07100KL
0	R6, R7	NS				
1	U1	MP3435	22V, 19A boost converter	QFN-20 (3mmx4mm)	MPS	MP3435GL

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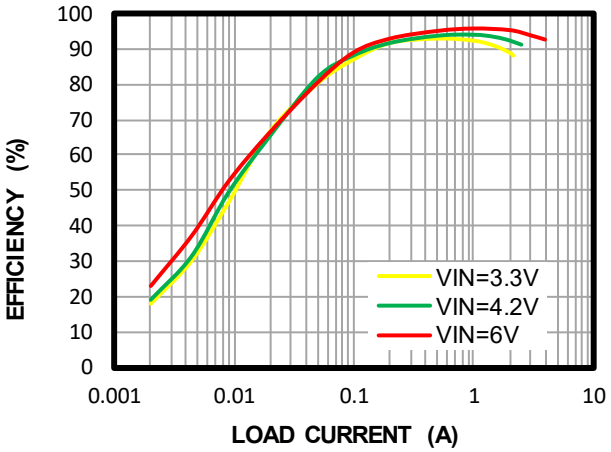
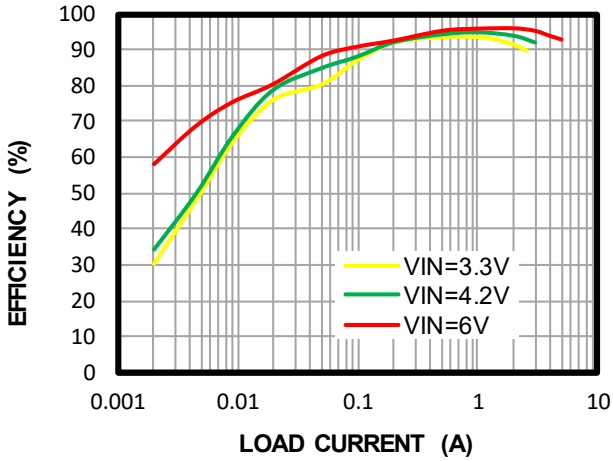
EVB TEST RESULTS

V_{IN} = 3.3V, V_{OUT} = 12V, L = 1.5µH, I_{OUT} = 2A, T_A = 25°C, unless otherwise noted.

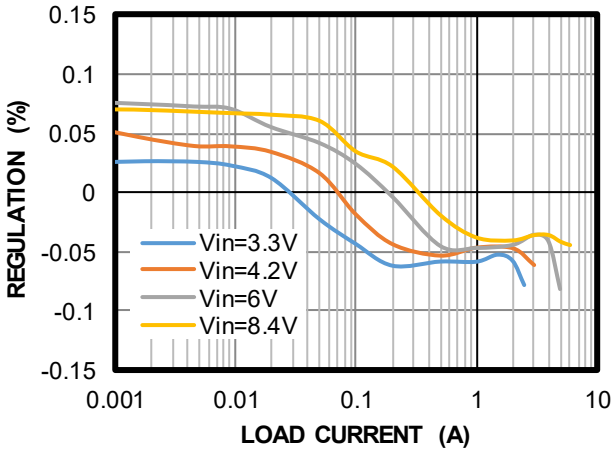
Efficiency vs. Load Current
Input MOSFET



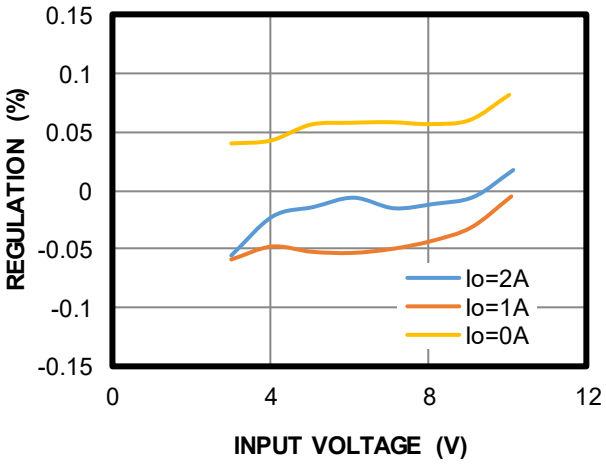
Efficiency vs. Load Current
No input MOSFET, GATE = GND



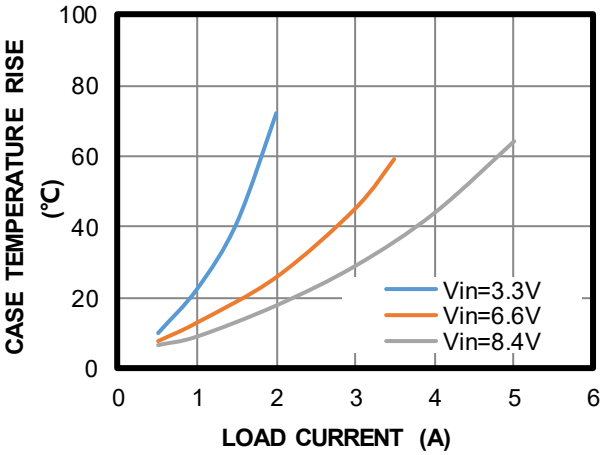
Load Regulation



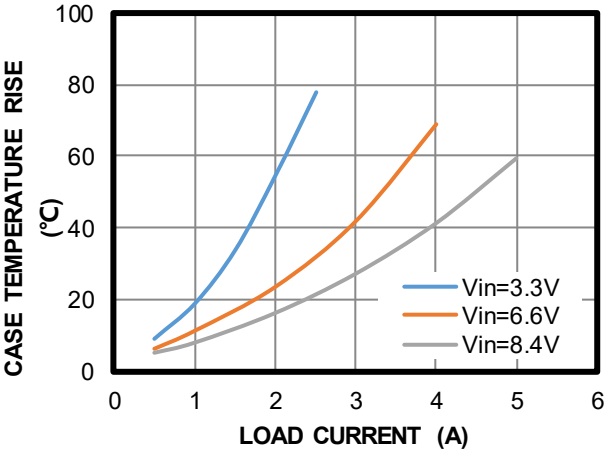
Line Regulation



Case Temperature Rise
Input MOSFET



Case Temperature Rise
No input MOSFET, GATE = GND



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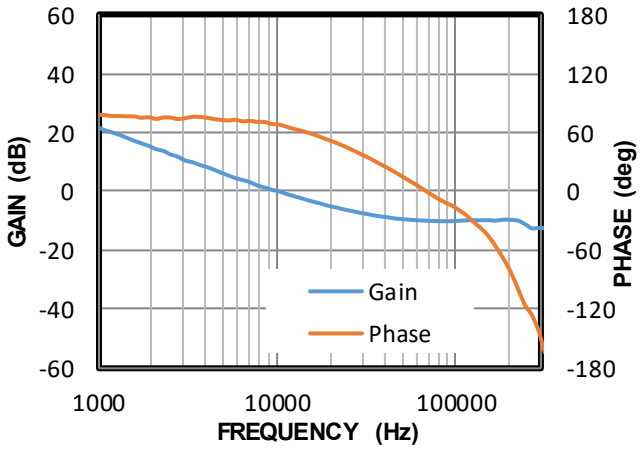
EVB TEST RESULTS *(continued)*

V_{IN} = 3.3V, V_{OUT} = 12V, L = 1.5µH, I_{OUT} = 2A, T_A = 25°C, unless otherwise noted.

Bode Plot



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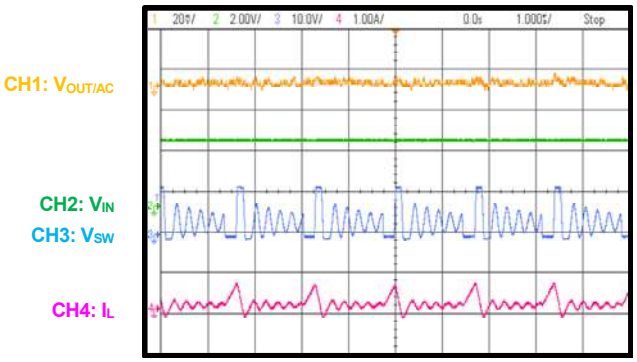
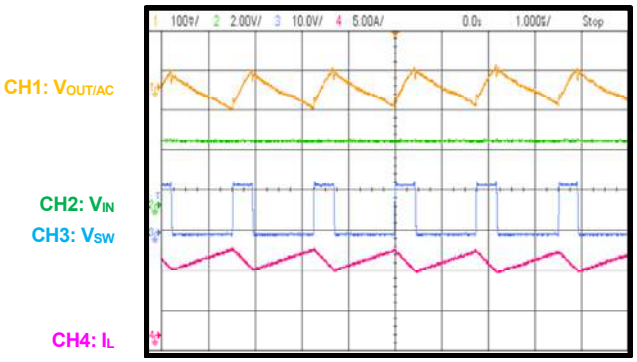
EVB TEST RESULTS *(continued)*

V_{IN} = 3.3V, V_{OUT} = 12V, L = 1.5µH, I_{OUT} = 2A, T_A = 25°C, unless otherwise noted.

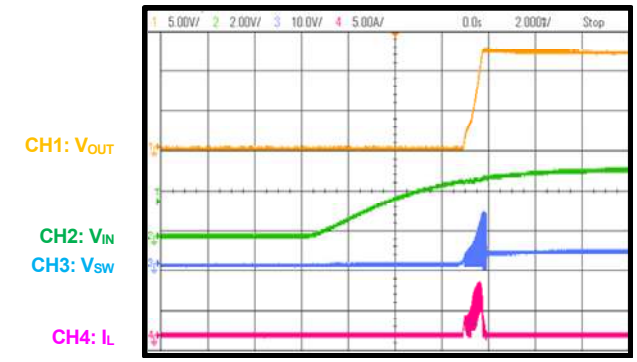
Steady State
I_{OUT} = 0A



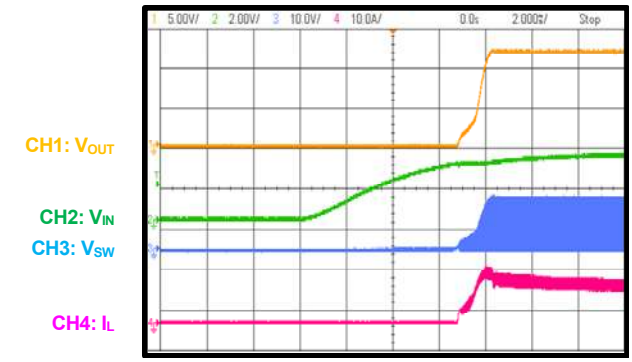
Steady State
I_{OUT} = 2A



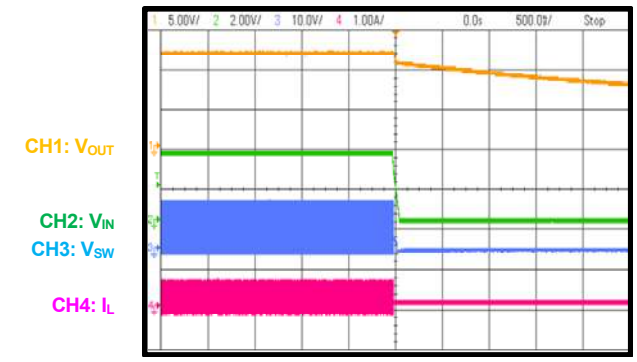
Start-Up through VIN
I_{OUT} = 0A



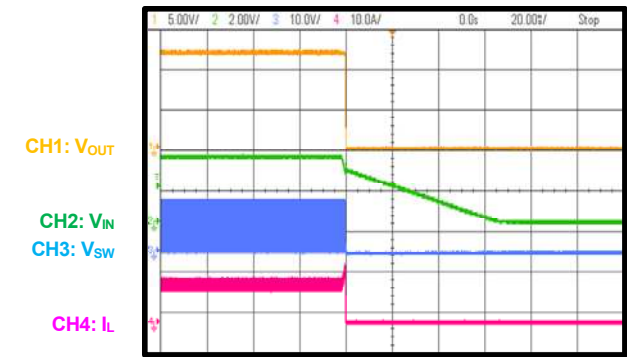
Start-Up through VIN
I_{OUT} = 2A



Shutdown through VIN
I_{OUT} = 0A



Shutdown through VIN
I_{OUT} = 2A



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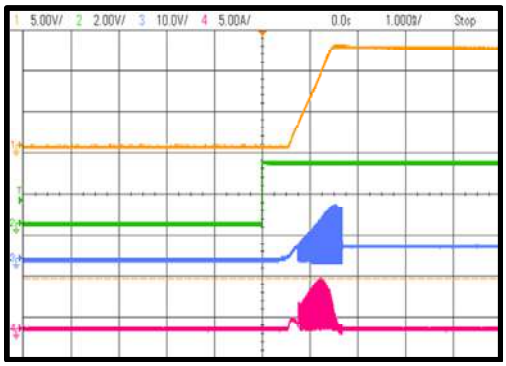
EVB TEST RESULTS *(continued)*

V_{IN} = 3.3V, V_{OUT} = 12V, L = 1.5µH, I_{OUT} = 2A, T_A = 25°C, unless otherwise noted.

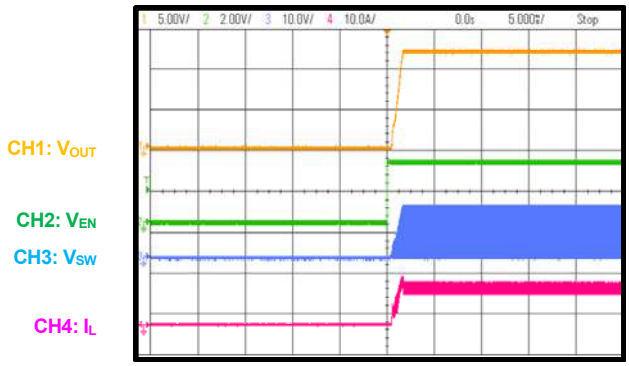
Start-Up through EN

I_{OUT} = 0A



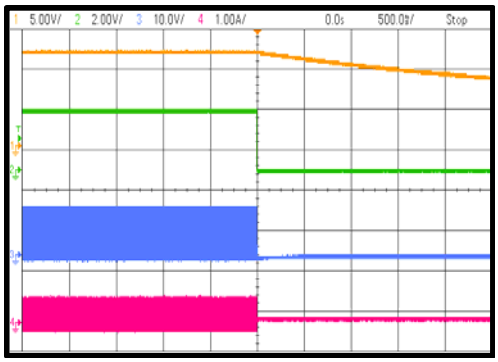
Start-Up through EN

I_{OUT} = 2A



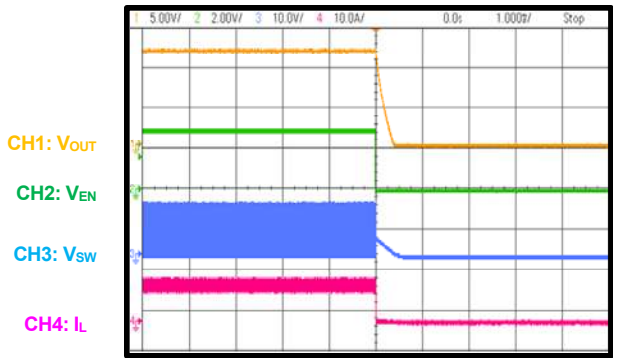
Shutdown through EN

I_{OUT} = 0A



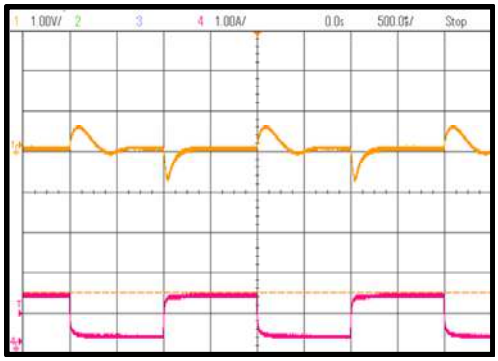
Shutdown through EN

I_{OUT} = 2A



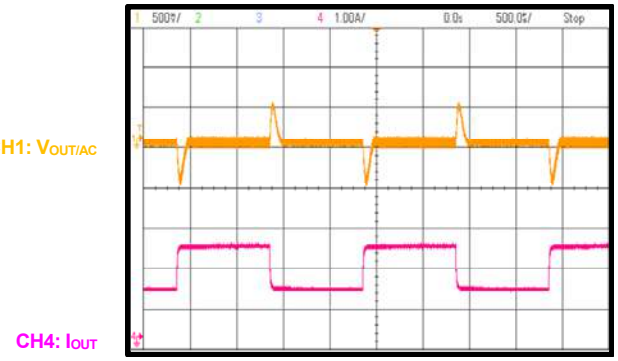
Load Transient

I_{OUT} = 0A to 1A, I_{RAMP} = 25mA/µs



Load Transient

I_{OUT} = 1A to 2A, I_{RAMP} = 25mA/µs



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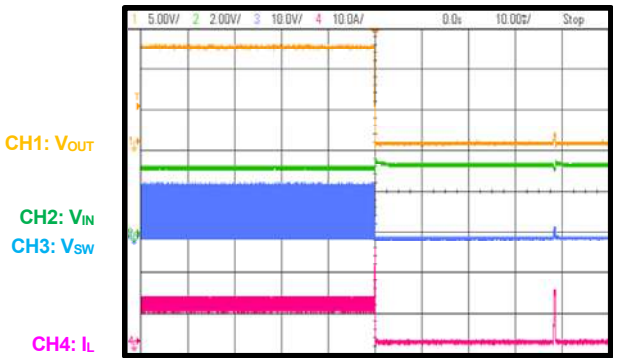
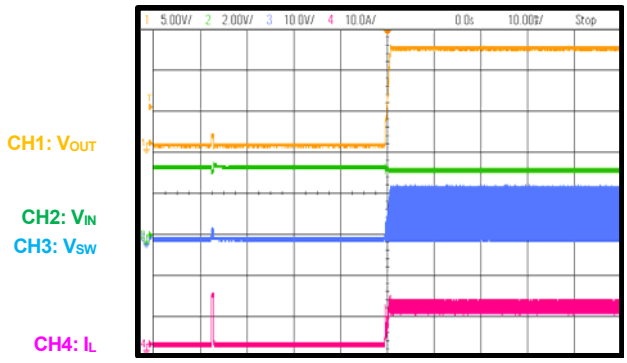
EVB TEST RESULTS *(continued)*

V_{IN} = 3.3V, V_{OUT} = 12V, L = 1.5µH, I_{OUT} = 2A, T_A = 25°C, unless otherwise noted.

SCP Entry



SCP Recovery



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PCB LAYOUT

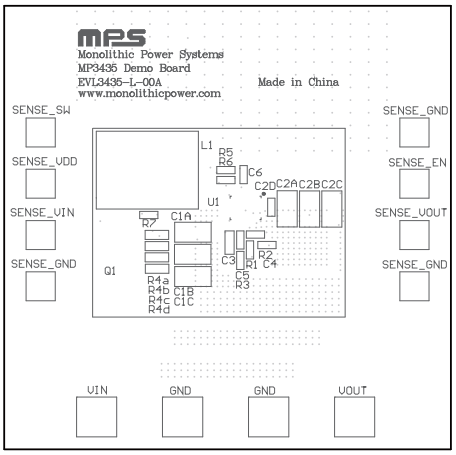

Figure 1: Top Silk

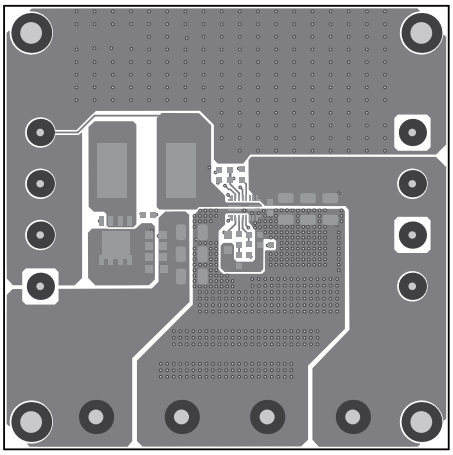

Figure 2: Top Layer

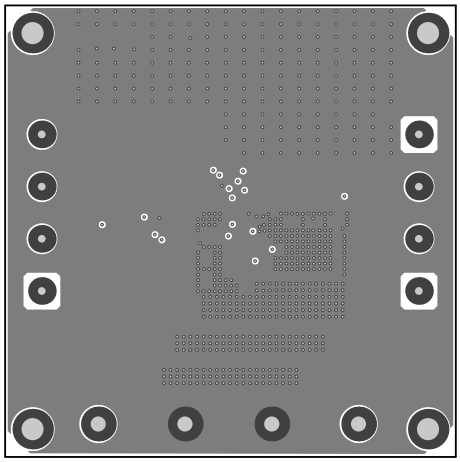

Figure 3: Mid-Layer 1

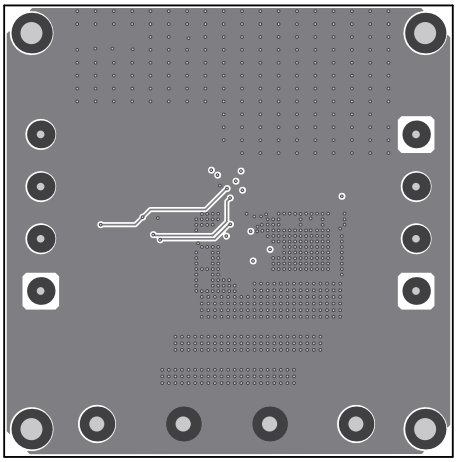

Figure 4: Mid-Layer 2

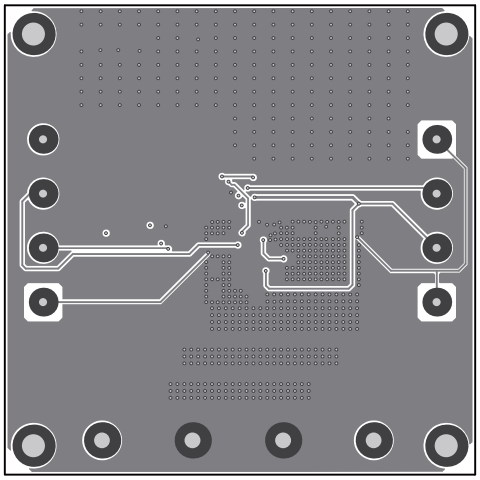

Figure 5: Bottom Layer

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	2/4/2021	Initial Release	-

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