

N-Channel NexFET™ Power MOSFET

 Check for Samples: [CSD13303W1015](#)

FEATURES

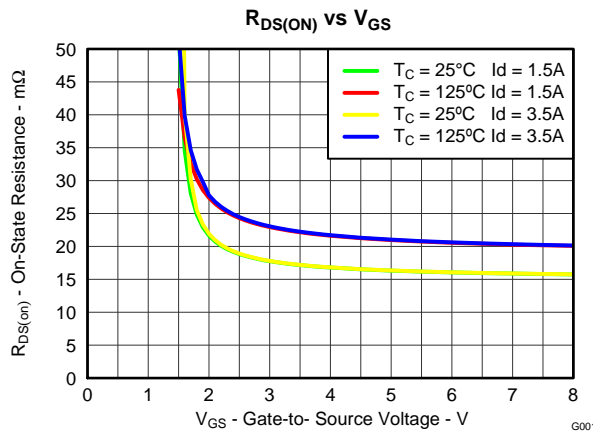
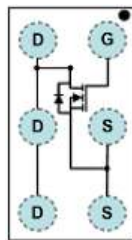
- Ultra Low on Resistance
- Ultra Low Qg and Qgd
- Small Footprint
- Low Profile 0.62 mm Height
- Pb Free
- RoHS Compliant
- Halogen Free
- CSP 1 × 1.5 mm Wafer Level Package

APPLICATIONS

- Battery Management
- Load Switch
- Battery Protection

DESCRIPTION

The device has been designed to deliver the lowest on resistance and gate charge in the smallest outline possible with excellent thermal characteristics in an ultra low profile.

Top View


PRODUCT SUMMARY

T _A = 25°C unless otherwise stated		TYPICAL VALUE		UNIT
V _{DS}	Drain to Source Voltage	12		V
Q _g	Gate Charge Total (4.5V)	3.9		nC
Q _{gd}	Gate Charge Gate to Drain	0.4		nC
R _{DS(on)}	Drain to Source On Resistance	V _{GS} = 2.5V	18	mΩ
		V _{GS} = 4.5V	16	mΩ
V _{GS(th)}	Voltage Threshold	0.85		V

ORDERING INFORMATION

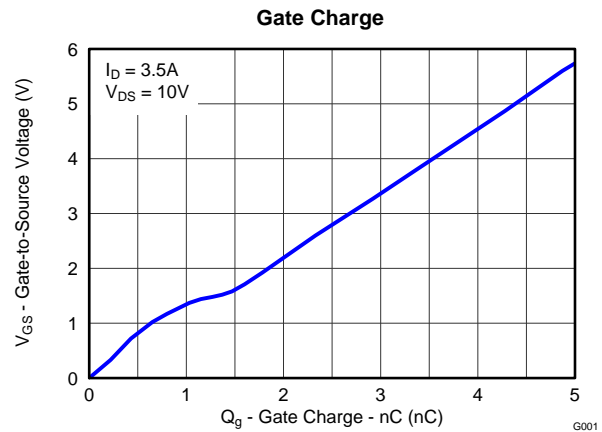
Device	Package	Media	Qty	Ship
CSD13303W1015	1 × 1.5 Wafer Level Package	7-inch reel	3000	Tape and Reel

ABSOLUTE MAXIMUM RATINGS

T _A = 25°C unless otherwise stated		VALUE	UNIT
V _{DS}	Drain to Source Voltage	12	V
V _{GS}	Gate to Source Voltage	±8	V
I _D	Continuous Drain Current, T _C = 25°C ⁽¹⁾	3.5	A
I _{DM}	Pulsed Drain Current, T _A = 25°C ⁽²⁾	31	A
P _D	Power Dissipation ⁽¹⁾	1.65	W
T _{STG}	Storage Temperature Range	-55 to 150	°C
T _J	Operating Junction Temperature Range		

(1) Typical R_{θJA} = 75.7°C/W on 1in² Cu (2 oz.) on 0.060" thick FR4 PCB.

(2) Pulse width ≤1ms, duty cycle ≤2%



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ELECTRICAL CHARACTERISTICS

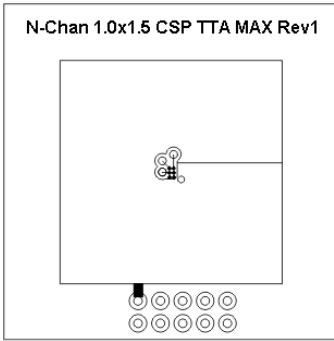
($T_A = 25^\circ\text{C}$ unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Static Characteristics						
BV_{DSS}	Drain to Source Voltage	$V_{GS} = 0V, I_D = 250\mu A$	12			V
I_{DSS}	Drain to Source Leakage Current	$V_{GS} = 0V, V_{DS} = 9.6V$			1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{DS} = 0V, V_{GS} = +8V$			100	nA
$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	0.65	0.85	1.2	V
$R_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = 2.5V, I_D = 1.5A$		18	23	$m\Omega$
		$V_{GS} = 4.5V, I_D = 1.5A$		16	20	$m\Omega$
g_{fs}	Transconductance	$V_{DS} = 6V, I_D = 1.5A$		14		S
Dynamic Characteristics						
C_{ISS}	Input Capacitance	$V_{GS} = 0V, V_{DS} = 6V, f = 1MHz$		550	715	pF
C_{OSS}	Output Capacitance			400	480	pF
C_{RSS}	Reverse Transfer Capacitance			29	36	pF
R_g	Gate Charge Total (4.5V)	$V_{DS} = 6V, I_D = 1.5A$		3	4.6	Ω
Q_g	Gate Charge Total (4.5V)			3.9	4.7	nC
Q_{gd}	Gate Charge Gate to Drain			0.4		nC
Q_{gs}	Gate Charge Gate to Source			1		nC
$Q_{g(th)}$	Gate Charge at V_{th}			0.6		nC
Q_{OSS}	Output Charge	$V_{DS} = 6V, V_{GS} = 0V$		4.9		nC
$t_{d(on)}$	Turn On Delay Time	$V_{DS} = 6V, V_{GS} = 4.5V, I_D = 1.5A$ $R_G = 4\Omega$		4.6		ns
t_r	Rise Time			10		ns
$t_{d(off)}$	Turn Off Delay Time			14.7		ns
t_f	Fall Time			3.2		ns
Diode Characteristics						
V_{SD}	Diode Forward Voltage	$I_S = 1.5A, V_{GS} = 0V$		0.7	1	V
Q_{rr}	Reverse Recovery Charge	$V_{DS} = 6V, I_F = 1.5A, di/dt = 200A/\mu s$		14		nC
t_{rr}	Reverse Recovery Time			38.7		ns

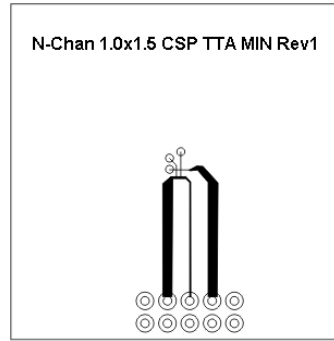
THERMAL CHARACTERISTICS

($T_A = 25^\circ\text{C}$ unless otherwise stated)

PARAMETER		MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Thermal Resistance Junction to Ambient (Minimum Cu area)			295.5	$^\circ\text{C/W}$
	Thermal Resistance Junction to Ambient (1 in ² Cu area)			94.6	$^\circ\text{C/W}$



Max $R_{\theta JA} = 94.6^{\circ}\text{C/W}$
when mounted on 1
 inch^2 of 2 oz. Cu.



Max $R_{\theta JA} = 295.5^{\circ}\text{C/W}$
when mounted on
minimum pad area of 2
oz. Cu.

TYPICAL MOSFET CHARACTERISTICS

($T_A = 25^{\circ}\text{C}$ unless otherwise stated)

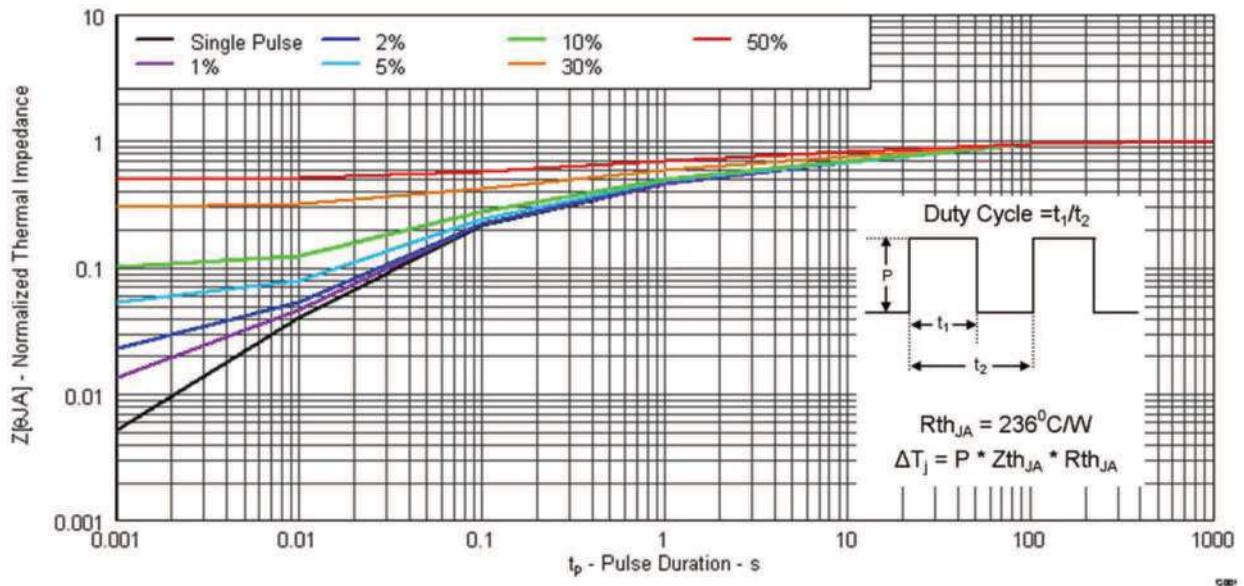


Figure 1. Transient Thermal Impedance

TYPICAL MOSFET CHARACTERISTICS (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

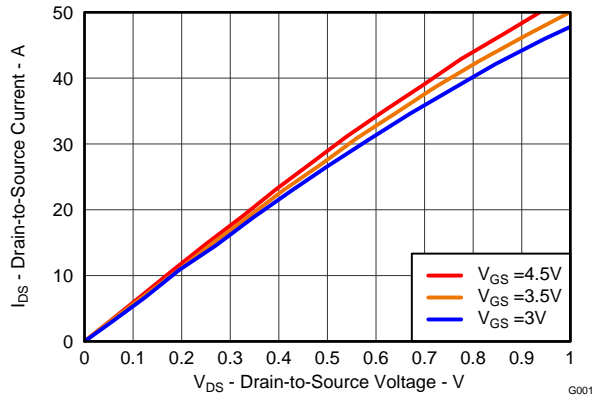


Figure 2. Saturation Characteristics

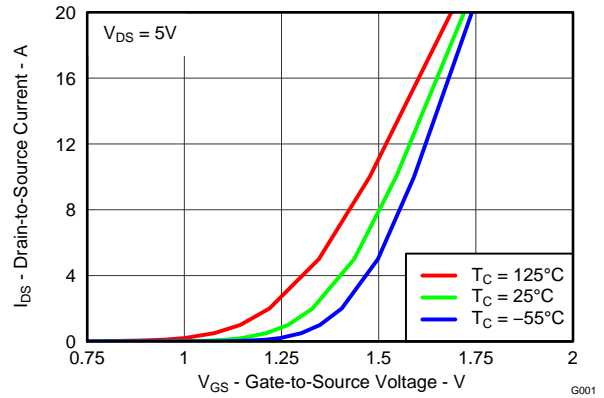


Figure 3. Transfer Characteristics

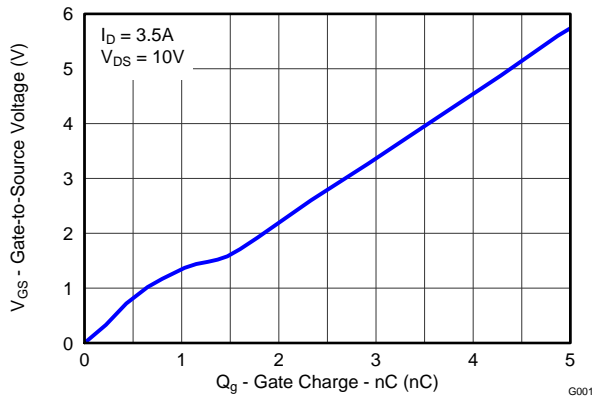


Figure 4. Gate Charge

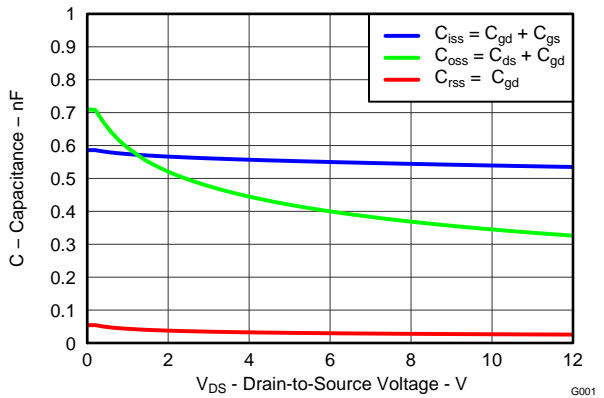


Figure 5. Capacitance

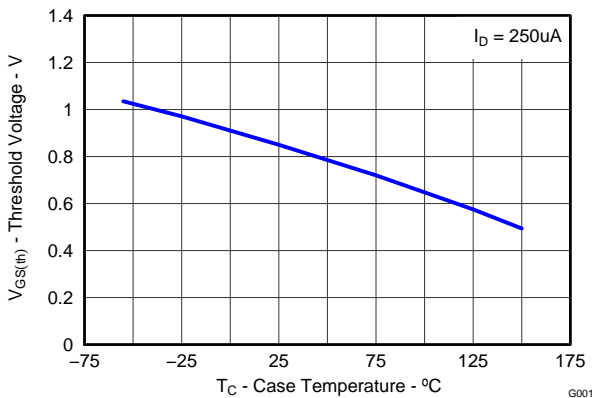


Figure 6. Threshold Voltage vs. Temperature

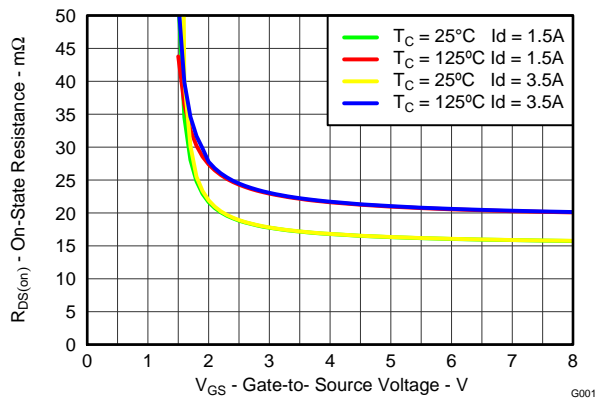


Figure 7. On Resistance vs. Gate Voltage

TYPICAL MOSFET CHARACTERISTICS (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

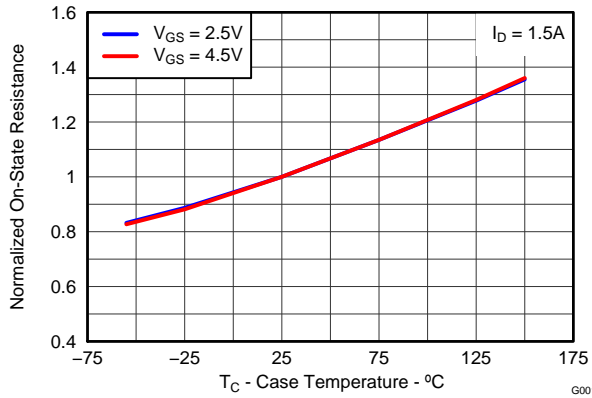


Figure 8. Normalized On Resistance vs. Temperature

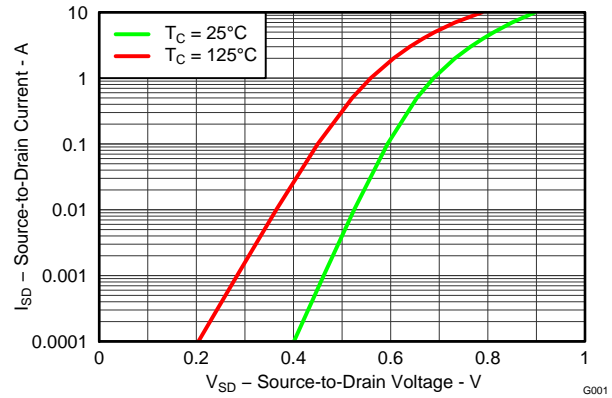


Figure 9. Typical Diode Forward Voltage

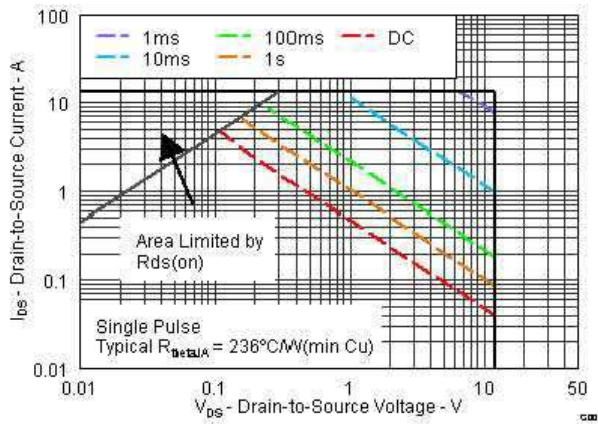


Figure 10. Maximum Safe Operating Area

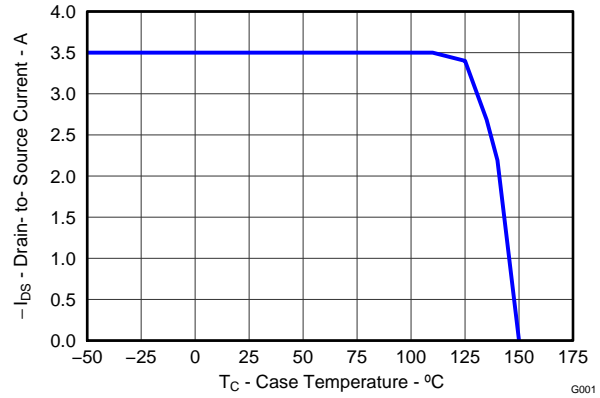


Figure 11. Maximum Drain Current vs. Temperature

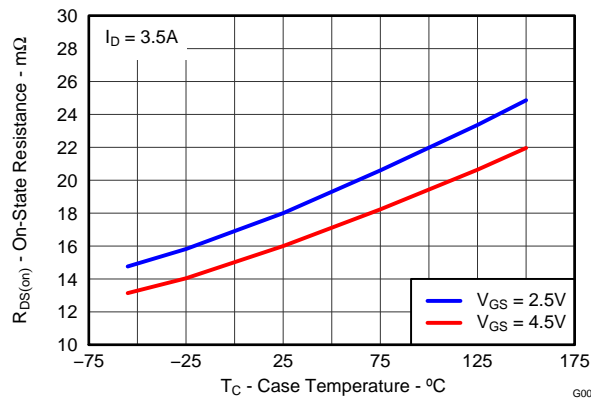
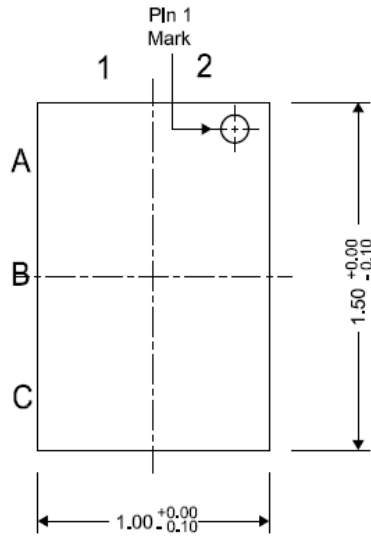


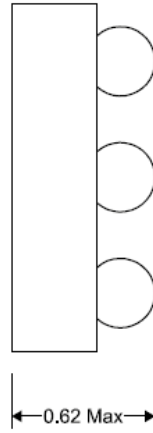
Figure 12. On Resistance vs. Temperature

MECHANICAL DATA

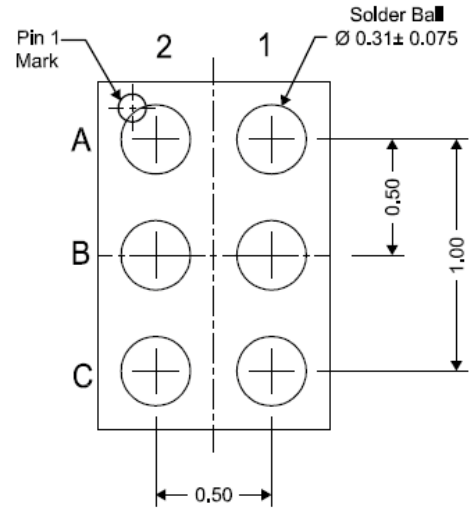
CSD13303W1015 Package Dimensions



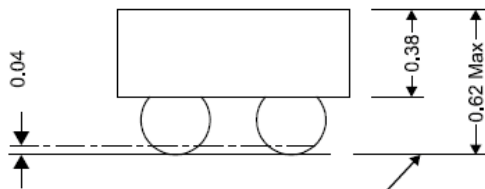
Top View



Side View



Bottom View



Seating Plane

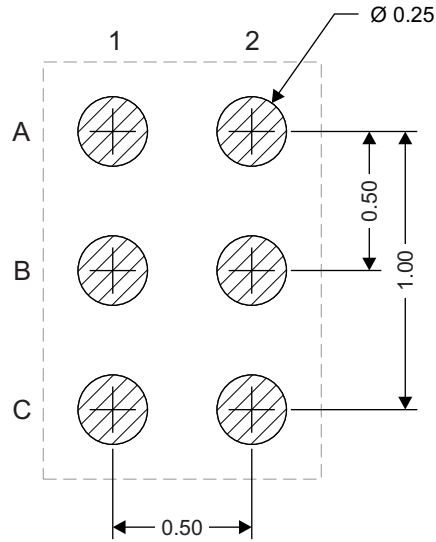
Front View

NOTE: All dimensions are in mm (unless otherwise specified)

Pinout

POSITION	DESIGNATION
C2, B2	Source
A2	Gate
A1, B1, C1	Drain

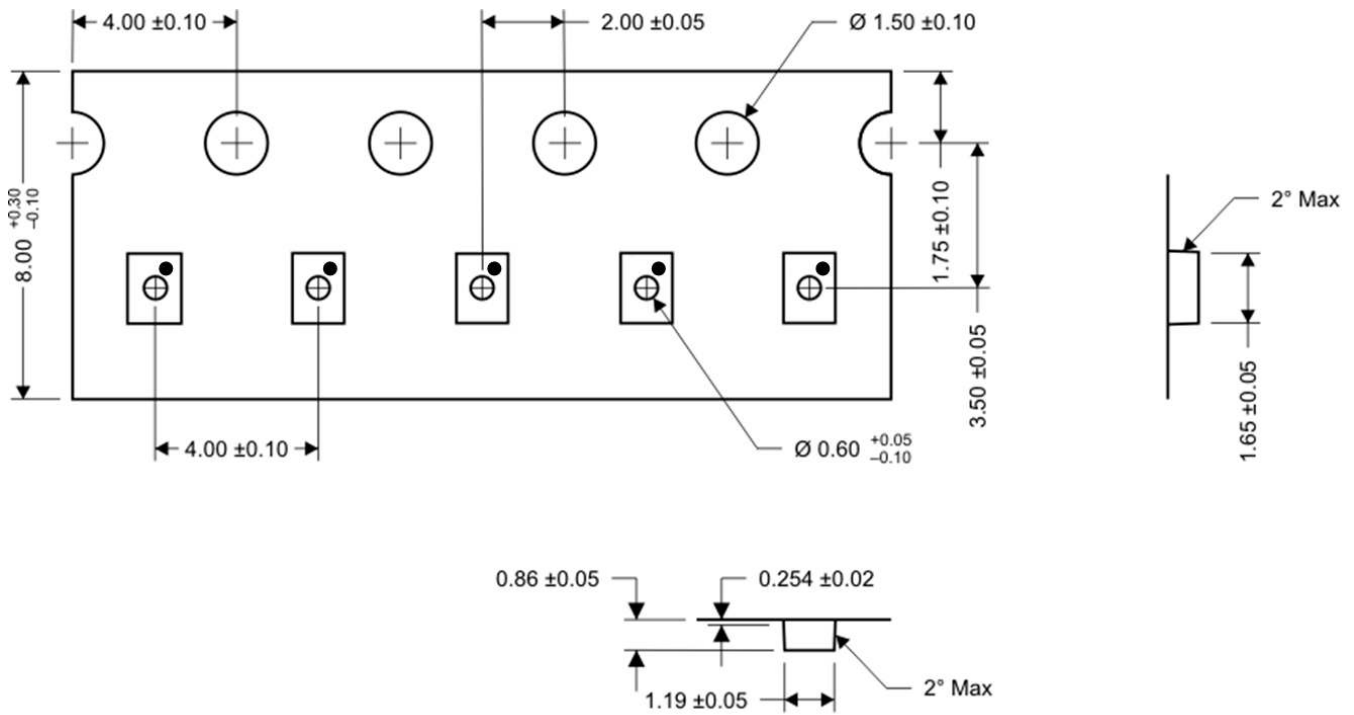
Land Pattern Recommendation



M0158-01

NOTE: All dimensions are in mm (unless otherwise specified)

Tape and Reel Information



M0159-01

NOTE: All dimensions are in mm (unless otherwise specified)

REVISION HISTORY

Changes from Original (May 2012) to Revision A	Page
• Changed the Tape and Reel Information section	7

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD13303W1015	ACTIVE	DSBGA	YZC	6	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-55 to 150	13303	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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