HAGIWARA Solutions

DDR4 SDRAM SO-DIMM
(PC4-25600 8GB ECC)
GN25N008GE-M625DC0

Rev. 1.00

Features

- JEDEC Standard 260-pin Small-Outline Dual In-Line Memory Module
- Inputs and Outputs are SSTL-12compatible
- VDD=VDDQ= 1.2Volt (TYP)
- VPP=2.5Volt (TYP)
- VDDSPD=2.2-3.6V
- Low-Power auto self-refresh (LPASR)
- Normal and Dynamic On-Die Termination for data, strobe and mask signals.
- Data bus inversion (DBI) for data bus
- Fixed burst chop (BC) of 4 and burst length (BL) of 8 via the MRS
- Selectable BC4 or BL8 on-the fly (OTF)
- Golden Connector (Au:30u")
- Chamfer
- Fly-By topology
- Terminated control, command and address bus
- Programmable /CAS Latency: 15, 17, 19, 21, 22
- Operation temperature – (0℃~85℃)
- On-die VREFDQ generation and Calibration
- On-Board EEPROM
- ECC function support
- RoHs and Halogen free

Part Number	GN25N008GE-M625DC0
Density	8GB
Module speed	PC4-25600 (DDR4-3200)
Function	ECC
Operating Temp	0 to +85℃
Organization	1Gx72
Component Composition	1024Mx8 Micron *9
Number of Rank	1
Height	30mm
Golden Connector	Au: 30u"
Chamfer	Yes

Key Parameter

Part Number	Module speed	tRCD (ns)	tRP (ns)	tRC (ns)	CL-tRCD-tRP
GN25N008GE-M625DC0	PC4-25600 (DDR4-3200)	13.75	13.75	45.75	22-22-22

Emvironmental Req.

Symbol	Parameter	Rating	Units	Notes
TOPR	Operating Temperature (ambient)	0 to +85	°C	1,2
		+85 to +95	°C	1,2
TSTG	Storage Temperature	-50 to +100	°C	-
HOPR	Operating Humidity (relative)	10 to 90	%	-
HSTG	Storage Humidity (without condensation)	5 to 95	%	-

1. The component maximum case temperature (Tcase) shall not exceed the value specified in the DDR DRAM component specification.
2. Average Refresh Period 7.8us at lower then TCASE 85°C, 3.9us at 85°C < TCASE ≦ 95°C

Absolute Max DC Rating

Symbol	Parameter	Rating	Units	Notes
V_{IN}, V_{OUT}	Voltage on any pins relative to Vss	-0.3 to +1.5	V	1
V_{DD}	Voltage on V_{DD} supply relative to Vss	-0.3 to +1.5	V	1,2
V_{DDQ}	Voltage on V_{DDQ} supply relative to Vss	-0.3 to +1.5	V	1,2
V_{PP}	Voltage on V_{PP} supply relative to Vss	-0.3 to +3.0	V	-

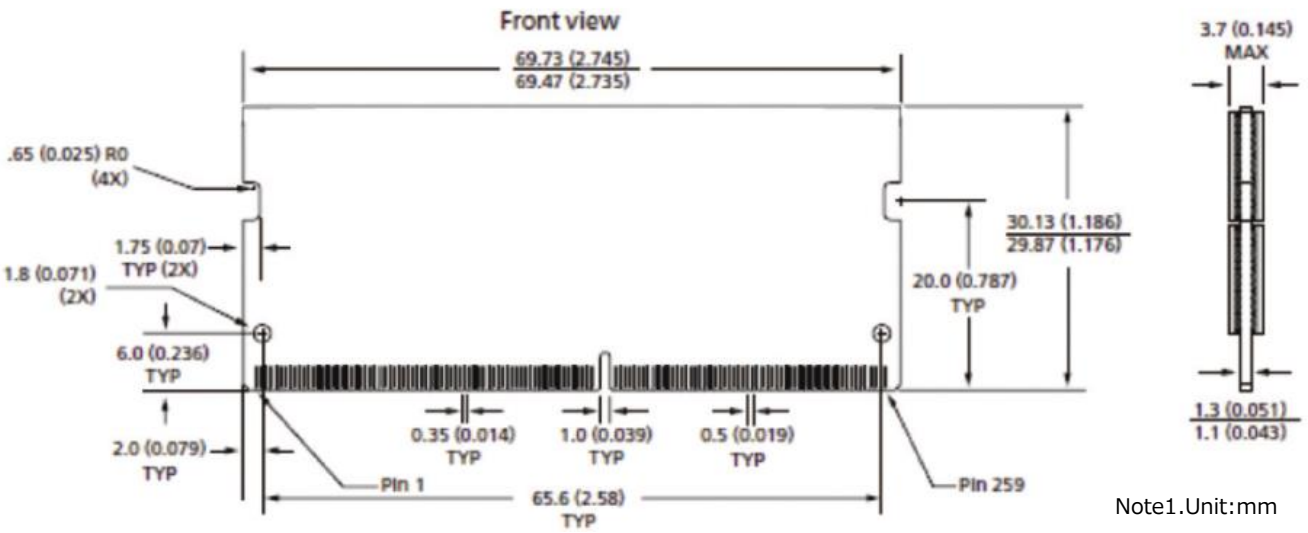
1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. VDD and VDDQ must be within 300 mV of each other at all times;and VREF must be not greater than 0.6 x VDDQ, When VDD and VDDQ are less than 500 mV; VREF may be equal to or less than 300 mV

Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units	Notes
V_{DD}	V_{DD} supply voltage	1.14	1.2	1.26	V	1
V_{PP}	DRAM activating power supply	2.375	2.5	2.75	V	2
$V_{REFCA(DC)}$	Input reference voltage command/ address bus	0.49 × V_{DD}	0.5 × V_{DD}	0.51 × V_{DD}	V	3
V_{TT}	Termination reference voltage (DC) – command/address bus	0.49 × V_{DD} - 20mV	0.5 × V_{DD}	0.51 × V_{DD} + 20mV	V	4

1. VDDQ tracks with VDD; VDDQ and VDD are tied together.
2. VPP must be greater than or equal to VDD at all times.
3. VREFCA must not be greater than 0.6 x VDD. When VDD is less than 500mV, VREF may be less than or equal to 300mV.
4. VTT termination voltages in excess of the specification limit adversely affect the voltage margins of command and address signals and reduce timing margins.

Dimensions



Note1.Unit:mm

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