



CY74FCT163827 CY74FCT163LD827

20-Bit Buffer

Features

- Low power, pin-compatible replacement for LCX, LPT, LVC, LVCH & LVT families
- 5V tolerant inputs and outputs*
- 24 mA & 6 mA balanced drive outputs
- Power-off disable outputs permits live insertion
- Edge-rate control circuitry for reduced noise
- FCT-C speed at 4.1 ns
- Latch-up performance exceeds JEDEC standard no. 17
- Typical output skew < 250 ps
- Industrial temperature range of -40°C to $+85^{\circ}\text{C}$
- TSSOP (19.6-mil pitch) or SSOP (25-mil pitch)
- Typical V_{Olp} (ground bounce) performance exceeds Mil Std 883D
- $V_{CC} = 2.7\text{V}$ to 3.6V
- ESD (HBM) > 2000V

CY74FCT163LD244

- Lite Drive™ option for low noise applications

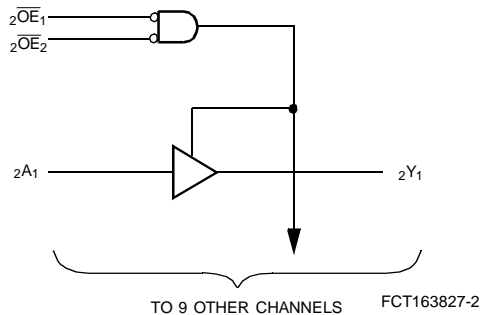
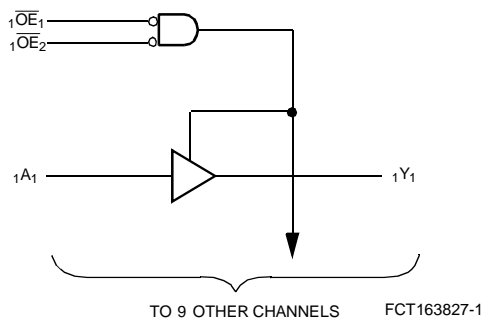
- 6 mA balanced drive outputs
- FCT-A speed at 4.8ns
- $V_{CC} = 3.0\text{V}$ to 3.6V
- ESD (HBM) > 1100V

Functional Description

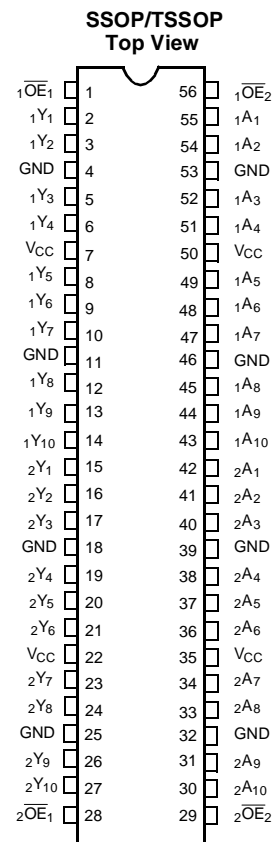
The CY74FCT163827 is a 20-bit buffer/line driver that provides high-performance bus interface buffering for wide data/address paths or buses carrying parity. It can be used as a single 20-bit buffer or two 10-bit buffers. Each 10-bit buffer has a pair of NANDed OE for increased flexibility.

The CY74FCT163827 has 24-mA balanced output drivers with current limiting resistors in the outputs. This reduces the need for external terminating resistors and provides for minimal undershoot and reduced ground bounce. The inputs and outputs were designed to be capable of being driven by 5.0V buses, allowing them to be used in mixed voltage systems as translators. The outputs are also designed with a power-off disable feature enabling them to be used in applications requiring live insertion.

Logic Block Diagrams CY74FCT163827, CY74FCT163LD827



Pin Configuration



Lite Drive is a trademark of Cypress Semiconductor Corporation.

Pin Description

Name	Description
OE	Output Enable Inputs (Active LOW)
A	Data Inputs
Y	Three-State Outputs

Function Table^[1]

Inputs			Outputs
\overline{OE}_1	\overline{OE}_2	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

Maximum Ratings^[2, 3]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -55°C to +125°C

Ambient Temperature with Power Applied..... -55°C to +125°C

Supply Voltage Range0.5V to +4.6V

DC Input Voltage-0.5V to +7.0V

DC Output Voltage-0.5V to +7.0V

DC Output Current (Maximum Sink Current/Pin) -60 to +120 mA

Power Dissipation 1.0W

Operating Range

Range	Ambient Temperature	V _{CC}
Commercial	-40°C to +85°C	2.7V to 3.6V

Electrical Characteristics Over the Operating Range V_{CC}=2.7V to 3.6V

Parameter	Description	Test Conditions	Min.	Typ. ^[4]	Max.	Unit
V _{IH}	Input HIGH Voltage	All Inputs	2.0		5.5	V
V _{IL}	Input LOW Voltage				0.8	V
V _H	Input Hysteresis ^[5]			100		mV
V _{IK}	Input Clamp Diode Voltage	V _{CC} =Min., I _{IN} =-18 mA		-0.7	-1.2	V
I _{IH}	Input HIGH Current	V _{CC} =Max., V _I =5.5			±1	µA
I _{IL}	Input LOW Current	V _{CC} =Max., V _I =GND			±1	µA
I _{OZH}	High Impedance Output Current (Three-State Output pins)	V _{CC} =Max., V _{OUT} =5.5V			±1	µA
I _{OZL}	High Impedance Output Current (Three-State Output pins)	V _{CC} =Max., V _{OUT} =GND			±1	µA
I _{OS}	Short Circuit Current ^[6]	V _{CC} =Max., V _{OUT} =GND	-60	-135	-240	mA
I _{OFF}	Power-Off Disable	V _{CC} =0V, V _{OUT} ≤4.5V			±100	µA
I _{CC}	Quiescent Power Supply Current	V _{IN} ≤0.2V, V _{IN} ≥V _{CC} -0.2V, V _{CC} =Max.		0.1	10	µA
ΔI _{CC}	Quiescent Power Supply Current (TTL inputs HIGH)	V _{IN} =V _{CC} -0.6V ^[7] , V _{CC} =Max.		2.0	30	µA

Note:

- H = HIGH Voltage Level, L = LOW Voltage Level, X = Don't Care, Z = HIGH Impedance.
- Operation beyond the limits set forth may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
- Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
- Typical values are at V_{CC}=3.3V, T_A = +25°C ambient.
- This parameter is guaranteed but not tested.
- Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
- Per TTL driven input; all other inputs at V_{CC} or GND.

Electrical Characteristics For Balanced Drive Devices Over the Operating Range $V_{CC}=2.7V$ to $3.6V$

Parameter	Description	Test Conditions	Min.	Typ. ^[4]	Max.	Unit
I_{ODL}	Output LOW Dynamic Current ^[6]	$V_{CC}=3.3V, V_{IN}=V_{IH}$ or $V_{IL}, V_{OUT}=1.5V$	45		180	mA
I_{ODH}	Output HIGH Dynamic Current ^[6]	$V_{CC}=3.3V, V_{IN}=V_{IH}$ or $V_{IL}, V_{OUT}=1.5V$	-45		-180	mA
V_{OH}	Output HIGH Voltage	$V_{CC}=\text{Min.}, I_{OH} = -0.1 \text{ mA}$	$V_{CC}-0.2$			V
		$V_{CC}=\text{Min.}, I_{OH} = -8 \text{ mA}$	2.4 ^[8]	3.0		V
		$V_{CC}=3.0V, I_{OH} = -24 \text{ mA}$	2.0	3.0		V
V_{OL}	Output LOW Voltage	$V_{CC}=\text{Min.}, I_{OL} = 0.1\text{mA}$			0.2	V
		$V_{CC}=\text{Min.}, I_{OL} = 24 \text{ mA}$		0.3	0.55	

Electrical Characteristics For Lite Drive Devices Over the Operating Range $V_{CC}=3.0V$ to $3.6V$

Parameter	Description	Test Conditions	Min.	Typ. ^[4]	Max.	Unit
I_{ODL}	Output LOW Dynamic Current ^[6]	$V_{CC}=3.3V, V_{IN}=V_{IH}$ or $V_{IL}, V_{OUT}=1.5V$	15.0		45	mA
I_{ODH}	Output HIGH Dynamic Current ^[6]	$V_{CC}=3.3V, V_{IN}=V_{IH}$ or $V_{IL}, V_{OUT}=1.5V$	-15.0		-45	mA
V_{OH}	Output HIGH Voltage	$V_{CC}=3.0 \text{ V}, I_{OH} = -6 \text{ mA}$	2.4	3.0		V
V_{OL}	Output LOW Voltage	$V_{CC}=3.0 \text{ V}, I_{OL} = 6 \text{ mA}$			0.55	V

Capacitance^[5] ($T_A = +25^\circ\text{C}, f = 1.0 \text{ MHz}$)

Parameter	Description	Test Conditions	Typ. ^[4]	Max.	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0V$	4.5	6.0	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	5.5	8.0	pF

Note:

8. $V_{OH}=V_{CC}-0.6V$ at rated current.



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Power Supply Characteristics

Parameter	Description	Test Conditions	Typ. ^[4]	Max.	Unit	
I _{CCD}	Dynamic Power Supply Current ^[9]	V _{CC} =Max., One Input Toggling, 50% Duty Cycle, Outputs Open, \overline{OE} =GND	V _{IN} =V _{CC} or V _{IN} =GND	50	75	μA/MHz
I _C	Total Power Supply Current ^[10]	V _{CC} =Max., f ₁ =10 MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling, \overline{OE} =GND	V _{IN} =V _{CC} or V _{IN} =GND	0.5	0.8	mA
			V _{IN} =V _{CC} -0.6V or V _{IN} =GND	0.5	0.8	mA
		V _{CC} =Max., f ₁ =2.5 MHz, 50% Duty Cycle, Outputs Open, Sixteen Bits Toggling, \overline{OE} =GND	V _{IN} =V _{CC} or V _{IN} =GND	2.0	3.0 ^[11]	mA
			V _{IN} =V _{CC} -0.6V or V _{IN} =GND	2.0	3.3 ^[11]	mA

Switching Characteristics Over the Operating Range V_{CC}=3.0V to 3.6V^[12,13]

Parameter	Description	CY74FCT163827A		CY74FCT163827C		Unit	Fig. No. ^[14]
		Min.	Max.	Min.	Max.		
t _{PLH} t _{PHL}	Propagation Delay Data to Output	1.5	4.8	1.5	4.1	ns	1, 3
t _{PZH} t _{PZL}	Output Enable Time	1.5	6.2	1.5	5.8	ns	1, 7, 8
t _{PHZ} t _{PLZ}	Output Disable Time	1.5	5.6	1.5	5.2	ns	1, 7, 8
t _{SK(O)}	Output Skew ^[15]		0.5		0.5	ns	—

Switching Characteristics Over the Operating Range V_{CC}=3.0V to 3.6V^[12,13]

Parameter	Description	CY74FCT163LD827 ^[16]		CY74FCT163827A ^[16]		Unit	Fig. No. ^[14]
		Min.	Max.	Min.	Max.		
t _{PLH} t _{PHL}	Propagation Delay Data to Output	1.5	6.5	1.5	4.8	ns	1, 3
t _{PZH} t _{PZL}	Output Enable Time	1.5	8.0	1.5	6.2	ns	1, 7, 8
t _{PHZ} t _{PLZ}	Output Disable Time	1.5	7.0	1.5	5.6	ns	1, 7, 8
t _{SK(O)}	Output Skew ^[15]		0.5		0.5	ns	—

Notes:

9. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
10. $I_C = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$
 $I_C = I_{\text{CC}} + \Delta I_{\text{CC}} D_H N_T + I_{\text{CCD}} (f_0/2 + f_1 N_1)$
 I_{CC} = Quiescent Current with CMOS input levels
 ΔI_{CC} = Power Supply Current for a TTL HIGH input (V_{IN}=3.4V)
 D_H = Duty Cycle for TTL inputs HIGH
 N_T = Number of TTL inputs at D_H
 I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
 f_0 = Clock frequency for registered devices, otherwise zero
 f_1 = Input signal frequency
 N_1 = Number of inputs changing at f₁
 All currents are in milliamps and all frequencies are in megahertz.
11. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
12. Minimum limits are guaranteed but not tested on Propagation Delays.
13. For V_{CC}=2.7, propagation delay, output enable and output disable times should be degraded by 20%.
14. See "Parameter Measurement Information" in the General Information section.
15. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.
16. The load capacitance is 30 pF for Lite Drive devices. For all others it is 50 pF.



Ordering Information CY74FCT163827

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.1	CY74FCT163827CPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT163827CPVC	O56	56-Lead (300-Mil) SSOP	
4.8	CY74FCT163827APAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT163827APVC	O56	56-Lead (300-Mil) SSOP	

Ordering Information CY74FCT163LD827

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.8	CY74FCT163LD827APAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT163LD827APVC	O56	56-Lead (300-Mil) SSOP	
6.5	CY74FCT163LD827PAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT163LD827PVC	O56	56-Lead (300-Mil) SSOP	

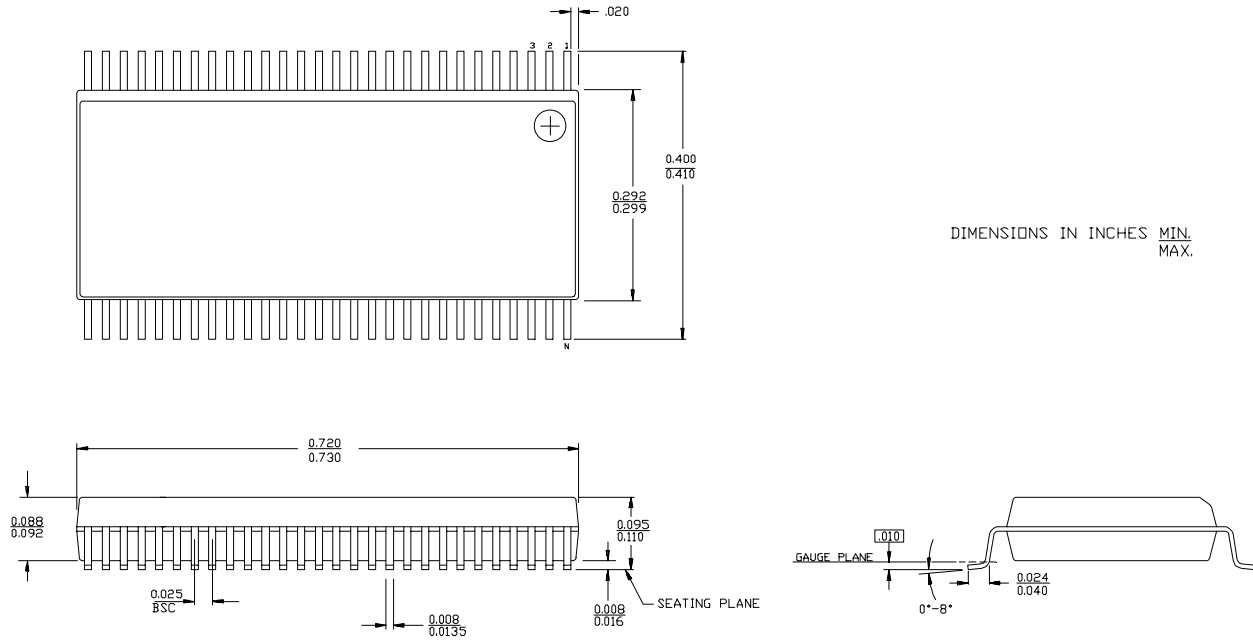
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Package Diagrams

56-Lead Shrunk Small Outline Package O56



56-Lead Thin Shrunk Small Outline Package Z56

